FAIRCHILD SEMICONDUCTOR™

April 2001
Revised June 2002

74LCX32500
Low Voltage 36-Bit Universal Bus Transceivers with 5V Tolerant Inputs and Outputs

General Description

These 36-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock ($\overline{CLKAB}$ and $\overline{CLKBA}$) inputs.

The LCX32500 is designed for low voltage (2.5V or 3.3V) V_{CC} applications with the capability of interfacing to a 5V signal environment.

The LCX32500 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power.

Features

- 5V tolerant inputs and outputs
- 2.3V–3.6V V_{CC} specifications provided
- 6.0 ns t_{PD} max (V_{CC} = 3.3V), 20 µA I_{CC} max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- ±24 mA output drive (V_{CC} = 3.0V)
- Uses patented noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA
- ESD performance:
  - Human body model > 2000V
  - Machine model > 200V
- Packaged in plastic Fine-Pitch Ball Grid Array (FBGA)

Note 1: To ensure the high-impedance state during power up or down, $\overline{OE}$ should be tied to V_{CC} and OE tied to GND through a resistor: the minimum value or the resistor is determined by the current-sourcing capability of the driver.

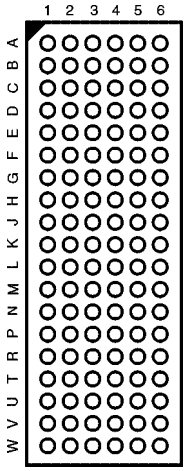
Ordering Code:

Order Number	Package Number	Package Description
74LCX32500G (Note 2)(Note 3)	BGA114A	114-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide

Note 2: Ordering code "G" indicates Trays.

Note 3: Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



(Top Thru View)

Truth Table (Note 4)

Inputs				Output
$OEAB_n$	$LEAB_n$	$\overline{CLKAB}_n$	A_n	B_n
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	B_0 (Note 5)
H	L	L	X	B_0 (Note 6)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial (HIGH or LOW, inputs may not float)
Z = High Impedance

Note 4: A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, and $\overline{CLKBA}$.

Note 5: Output level before the indicated steady-state input conditions were established.

Note 6: Output level before the indicated steady-state input conditions were established, provided that $\overline{CLKAB}$ was LOW before LEAB went LOW.

Pin Descriptions

Pin Names	Description
$1A_1$ - $1A_{18}$ $2A_1$ - $2A_{18}$	Data Register A Inputs/3-STATE Outputs
$1B_1$ - $1B_{18}$ $2B_1$ - $2B_{18}$	Data Register B Inputs/3-STATE Outputs
$\overline{CLKAB}_1$, $\overline{CLKBA}_1$ $\overline{CLKAB}_2$, $\overline{CLKBA}_2$	Clock Pulse Inputs
$LEAB_1$, $LEBA_1$ $LEAB_2$, $LEBA_2$	Latch Enable Inputs
$OEAB_1$, $\overline{OEBA}_1$ $OEAB_2$, $\overline{OEBA}_2$	Output Enable Inputs

FBGA Pin Assignments

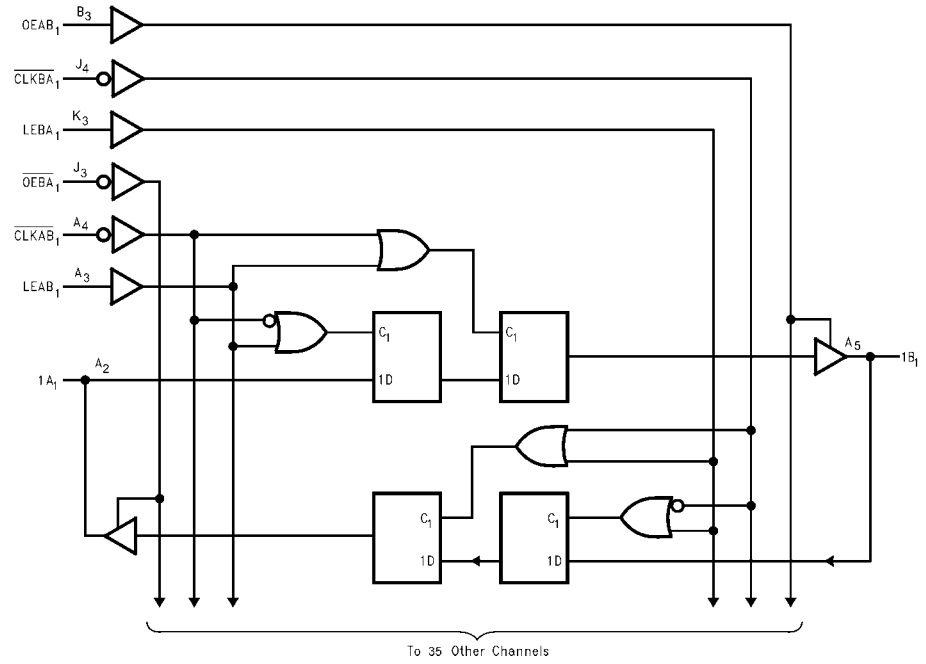
	1	2	3	4	5	6
A	$1A_2$	$1A_1$	$LEAB_1$	$\overline{CLKAB}_1$	$1B_1$	$1B_2$
B	$1A_4$	$1A_3$	$OEAB_1$	GND	$1B_3$	$1B_4$
C	$1A_6$	$1A_5$	GND	GND	$1B_5$	$1B_6$
D	$1A_8$	$1A_7$	V_{CC}	V_{CC}	$1B_7$	$1B_8$
E	$1A_{10}$	$1A_9$	GND	GND	$1B_9$	$1B_{10}$
F	$1A_{12}$	$1A_{11}$	GND	GND	$1B_{11}$	$1B_{12}$
G	$1A_{14}$	$1A_{13}$	V_{CC}	V_{CC}	$1B_{13}$	$1B_{14}$
H	$1A_{15}$	$1A_{16}$	GND	GND	$1B_{16}$	$1B_{15}$
J	$1A_{17}$	$1A_{18}$	$\overline{OEBA}_1$	$\overline{CLKBA}_1$	$1B_{18}$	$1B_{17}$
K	NC	$LEAB_2$	$LEBA_1$	GND	$\overline{CLKAB}_2$	NC
L	$2A_2$	$2A_1$	$OEAB_2$	GND	$2B_1$	$2B_2$
M	$2A_4$	$2A_3$	GND	GND	$2B_3$	$2B_4$
N	$2A_6$	$2A_5$	V_{CC}	V_{CC}	$2B_5$	$2B_6$
P	$2A_8$	$2A_7$	GND	GND	$2B_7$	$2B_8$
R	$2A_{10}$	$2A_9$	GND	GND	$2B_9$	$2B_{10}$
T	$2A_{12}$	$2A_{11}$	V_{CC}	V_{CC}	$2B_{11}$	$2B_{12}$
U	$2A_{14}$	$2A_{13}$	GND	GND	$2B_{13}$	$2B_{14}$
V	$2A_{15}$	$2A_{16}$	$\overline{OEBA}_2$	$\overline{CLKBA}_2$	$2B_{16}$	$2B_{15}$
W	$2A_{17}$	$2A_{18}$	$LEBA_2$	GND	$2B_{18}$	$2B_{17}$

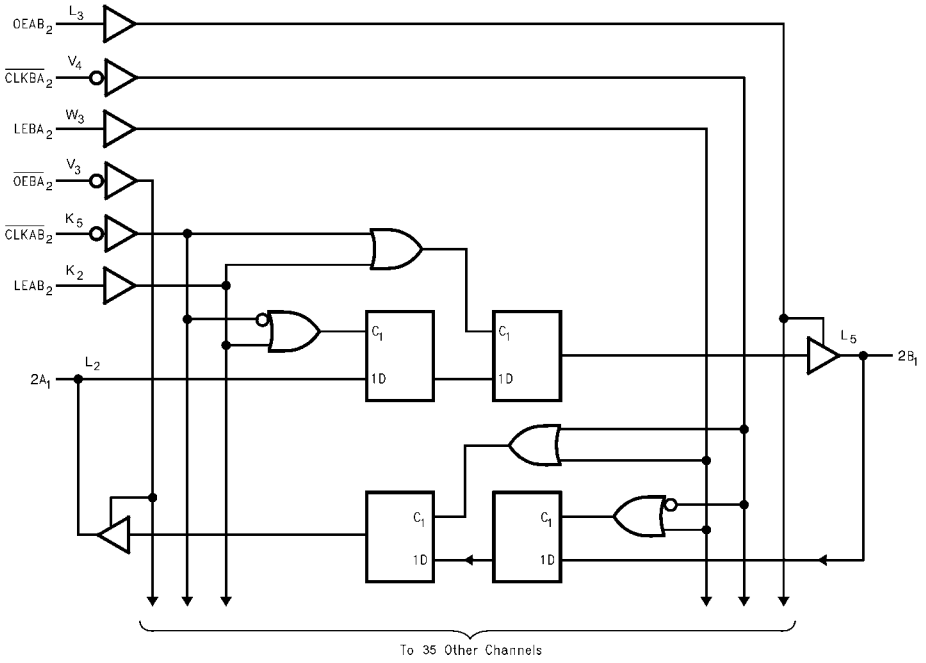
Functional Description

For A-to-B data flow, the LCX32500 operates in the transparent mode when LEAB is HIGH. When LEAB is LOW, the A data is latched if $\overline{CLKAB}$ is held at a HIGH or LOW logic level. If LEAB is LOW, the A bus data is stored in the latch/flip-flop on the HIGH-to-LOW transition of $\overline{CLKAB}$. Output-enable OEAB is active-HIGH. When OEAB is HIGH, the outputs are active. When OEAB is LOW, the outputs are in the high impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, LEBA, and $\overline{CLKBA}$. The output enables are complementary (OEAB is active HIGH and $\overline{OEBA}$ is active LOW).

Logic Diagrams





Absolute Maximum Ratings(Note 7)

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in 3-STATE	V
		−0.5 to V_{CC} + 0.5	Output in HIGH or LOW State (Note 8)	
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50	V_O < GND	mA
		+50	V_O > V_{CC}	
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Recommended Operating Conditions (Note 9)

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
		3-STATE	0	5.5	
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V – 3.6V		±24	mA
		V_{CC} = 2.7V – 3.0V		±12	
		V_{CC} = 2.3V – 2.7V		±8	
T_A	Free-Air Operating Temperature		–40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

Note 7: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 8: I_O Absolute Maximum Rating must be observed.

Note 9: Unused (inputs or I/O's) must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.3 – 2.7	1.7		V
			2.7 – 3.6	2.0		
V_{IL}	LOW Level Input Voltage		2.3 – 2.7		0.7	V
			2.7 – 3.6		0.8	
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 µA	2.3 – 3.6	V_{CC} – 0.2		V
		I_{OH} = −8 mA	2.3	1.8		
		I_{OH} = −12 mA	2.7	2.2		
		I_{OH} = −18 mA	3.0	2.4		
		I_{OH} = −24 mA	3.0	2.2		
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 µA	2.3 – 3.6		0.2	V
		I_{OL} = 8 mA	2.3		0.6	
		I_{OL} = 12 mA	2.7		0.4	
		I_{OL} = 16 mA	3.0		0.4	
		I_{OL} = 24 mA	3.0		0.55	
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.3 – 3.6		±5.0	µA
I_{OZ}	3-STATE I/O Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.3 – 3.6		±5.0	µA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	µA

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = -40°C$ to $+85°C$		Units
				Min	Max	
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.3 – 3.6		20	µA
		$3.6V \le V_I$, $V_O \le 5.5V$ (Note 10)	2.3 – 3.6		±20	
ΔI_{CC}	Increase in I_{CC} per Input	$V_{IH} = V_{CC} - 0.6V$	2.3 – 3.6		500	µA

Note 10: Outputs disabled or 3-STATE only.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $R_L = 500\ \Omega$						Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		$V_{CC} = 2.5V \pm 0.2V$		
		$C_L = 50$ pF		$C_L = 50$ pF		$C_L = 30$ pF		
		Min	Max	Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	170						MHz
t_{PHL}	Propagation Delay	1.5	6.0	1.5	7.0	1.5	7.2	ns
t_{PLH}	Bus to Bus	1.5	6.0	1.5	7.0	1.5	7.2	
t_{PHL}	Propagation Delay	1.5	6.7	1.5	8.0	1.5	8.4	ns
t_{PLH}	Clock to Bus	1.5	6.7	1.5	8.0	1.5	8.4	
t_{PHL}	Propagation Delay	1.5	7.0	1.5	8.0	1.5	8.4	ns
t_{PLH}	LE to Bus	1.5	7.0	1.5	8.0	1.5	8.4	
t_{PZL}	Output Enable Time	1.5	7.2	1.5	8.2	1.5	9.4	ns
t_{PZH}		1.5	7.2	1.5	8.2	1.5	9.4	
t_{PLZ}	Output Disable Time	1.5	7.0	1.5	8.0	1.5	8.4	ns
t_{PHZ}		1.5	7.0	1.5	8.0	1.5	8.4	
t_S	Setup Time	2.5		2.5		3.0		ns
t_H	Hold Time	1.5		1.5		2.0		ns
t_W	Pulse Width	3.0		3.0		3.5		ns

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$ Typical	Units
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
		$C_L = 30$ pF, $V_{IH} = 2.5V$, $V_{IL} = 0V$	2.5	0.6	
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	–0.8	V
		$C_L = 30$ pF, $V_{IH} = 2.5V$, $V_{IL} = 0V$	2.5	–0.6	

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
$C_{I/O}$	Input/Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, f = 10 MHz	20	pF

AC LOADING and WAVEFORMS Generic for LCX Family

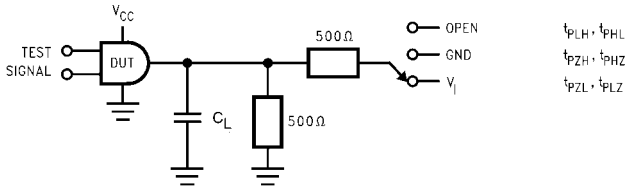
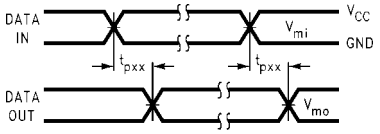
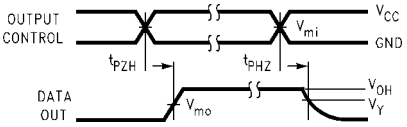


FIGURE 1. AC Test Circuit (C_L includes probe and jig capacitance)

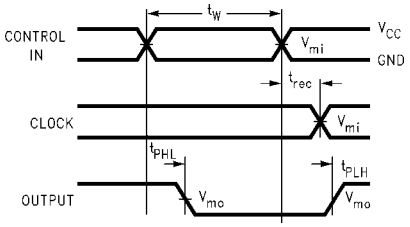
Test	Switch
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at V_{CC} = 3.3 ± 0.3V, and 2.7V V_{CC} x 2 at V_{CC} = 2.5 ± 0.2V
t_{PZH},t_{PHZ}	GND



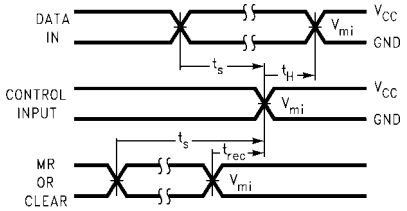
Waveform for Inverting and Non-Inverting Functions



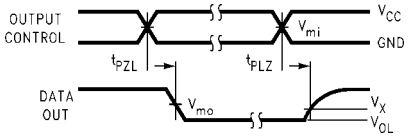
3-STATE Output High Enable and Disable Times for Logic



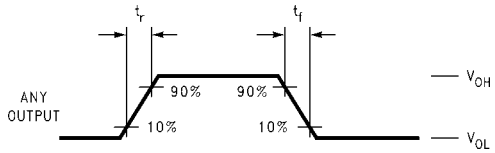
Propagation Delay. Pulse Width and t_{rec} Waveforms



Setup Time, Hold Time and Recovery Time for Logic



3-STATE Output Low Enable and Disable Times for Logic

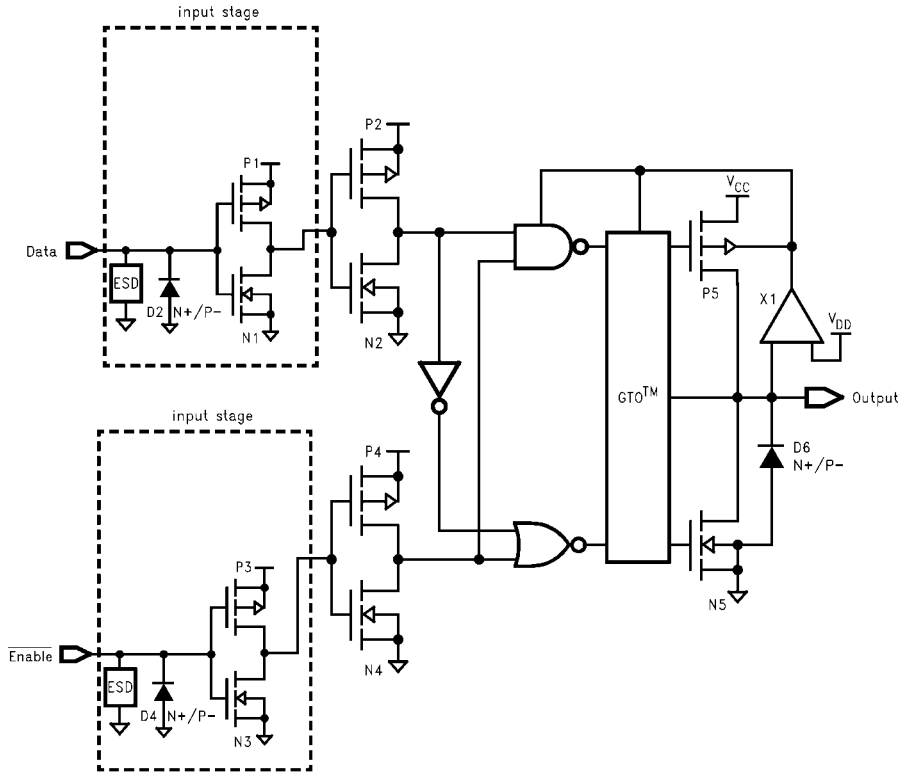


t_{rise} and t_{fall}

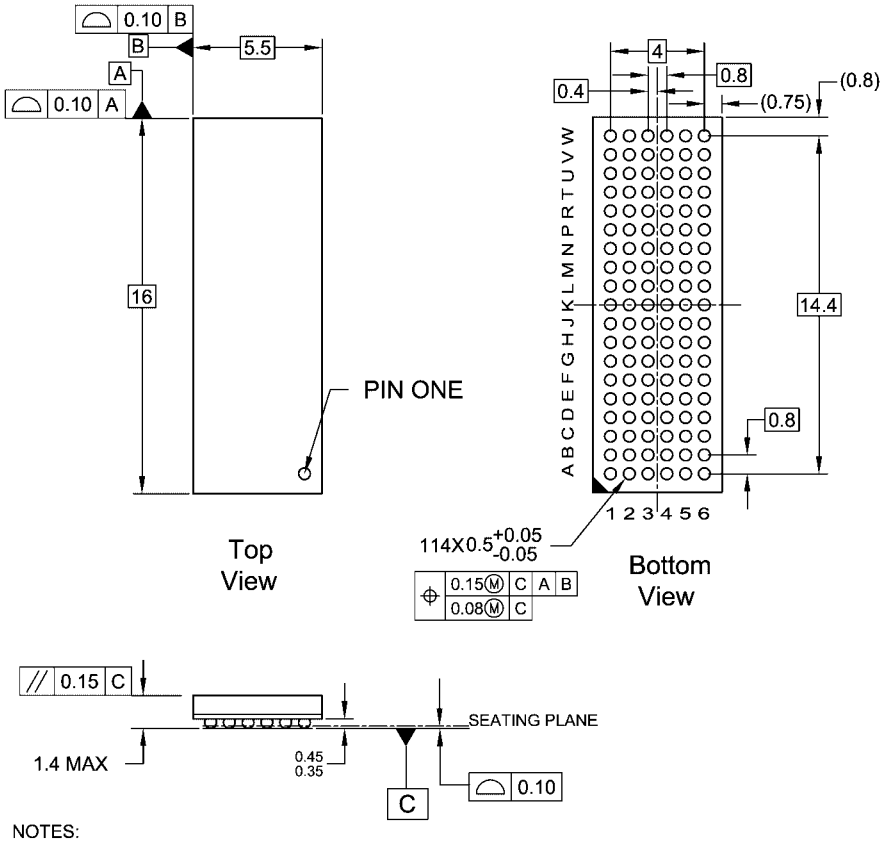
FIGURE 2. Waveforms
(Input Characteristics; f =1MHz, t_r = t_f = 3ns)

Symbol	V_{CC}		
	3.3V ± 0.3V	**2.7V**	**2.5V ± 0.2V**
V_{mi}	1.5V	1.5V	V_{CC}/2
V_{mo}	1.5V	1.5V	V_{CC}/2
V_x	V_{OL} + 0.3V	V_{OL} + 0.3V	V_{OL} + 0.15V
V_y	V_{OH} − 0.3V	V_{OH} − 0.3V	V_{OH} − 0.15V

Schematic Diagram Generic for LCX Family



Physical Dimensions inches (millimeters) unless otherwise noted



NOTES:

A. THIS PACKAGE CONFORMS TO JEDEC M0-205
B. ALL DIMENSIONS IN MILLIMETERS
C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA114ArevE

114-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
Package Number BGA114A

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com