FAIRCHILD

SEMICONDUCTOR TM

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74LCX760
Low Voltage Buffer/Line Driver
with 5V Tolerant Inputs and Open Drain Outputs

General Description

The LCX760 is the Open Drain version of the LCX244. The LCX760 contains eight non-inverting buffers with 3-STATE outputs. The device may be employed as a memory address driver, clock driver and bus-oriented transmitter/receiver. The LCX760 is designed for low voltage (2.5V or 3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX760 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- Open drain version of the LCX244
- 5V tolerant inputs and outputs
- 2.3V–3.6V V_{CC} specifications provided
- 8.0 ns t_{PD} max (V_{CC} = 3.3V), 10 μA I_{CC} max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- 24 mA output drive (V_{CC} = 3.0V)
- Implements patented noise/EMI reduction circuitry
- Latch-up conforms to JEDEC JED78
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

Note 1: To ensure the high-impedance state during power up or down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor: the minimum value or the resistor is determined by the current-sourcing capability of the driver.

Ordering Code:

Order Number	Package Number	Package Description
74LCX760WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74LCX760SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 4.4mm Wide
74LCX760MSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
74LCX760MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol
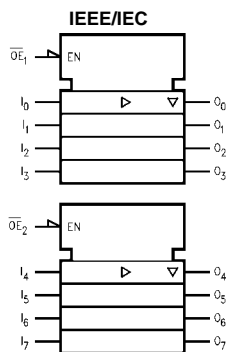
Connection Diagram
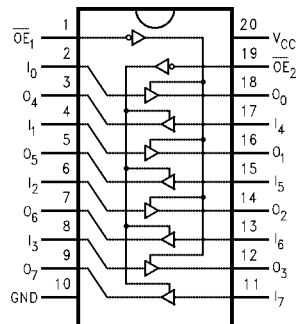
Pin Descriptions

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	3-STATE Output Enable Inputs
I_0–I_7	Inputs
O_0–O_7	Outputs

Truth Tables

Inputs		Outputs
$\overline{OE}_1$	I_n	(Pins 12, 14, 16, 18)
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_2$	I_n	(Pins 3, 5, 7, 9)
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

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Absolute Maximum Ratings(Note 2)

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in HIGH or LOW State (Note 3)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50	V_O < GND	mA
		+50	V_O > V_{CC}	
I_O	DC Output Sink Current	50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Recommended Operating Conditions (Note 4)

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage		0	5.5	V
I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V		24	mA
		V_{CC} = 2.7V − 3.0V		12	
		V_{CC} = 2.3V − 2.7V		8	
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

Note 2: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 3: I_O Absolute Maximum Rating must be observed.

Note 4: Unused inputs or I/Os must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C Min	Max	Units
V_{IH}	HIGH Level Input Voltage		2.3 – 2.7	1.7		V
			2.7 – 3.6	2.0		
V_{IL}	LOW Level Input Voltage		2.3 – 2.7		0.7	V
			2.7 – 3.6		0.8	
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.3 – 3.6		0.2	V
		I_{OL} = 8 mA	2.3		0.6	
		I_{OL} = 12 mA	2.7		0.4	
		I_{OL} = 16 mA	3.0		0.4	
		I_{OL} = 24 mA	3.0		0.55	
I_I	Input Leakage Current	$0 \leq V_I \leq 5.5V$	2.3 – 3.6		±5.0	μA
I_{OZ}	3-STATE Output Leakage	$0 \leq V_O \leq 5.5V$	2.3 – 3.6		±5.0	μA
		V_I = V_{IH} or V_{IL}				
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.3 – 3.6		10	μA
		$3.6V \leq V_I$, $V_O \leq 5.5V$ (Note 5)	2.3 – 3.6		±10	
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.3 – 3.6		500	μA
I_{OHZ}	Off State Current	V_O = 5.5	2 - 3.6		10	μA

Note 5: Outputs disabled or 3-STATE only.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $R_L = 500\Omega$						Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		$V_{CC} = 2.5V \pm 0.2$		
		$C_L = 50$ pF		$C_L = 50$ pF		$C_L = 30$ pF		
		Min	Max	Min	Max	Min	Max	
t_{PZL}	Propagation Delay	0.5	8.0	0.5	9.0	0.5	10.0	ns
t_{PLZ}	Data to Output	0.5	7.0	0.5	8.0	0.5	8.4	
t_{PZL}	Output Enable Time $\overline{OE}_n$ to Out	0.5	8.0	0.5	9.0	0.5	10.0	ns
t_{PLZ}	Output Disable Time $\overline{OE}_n$ to Out	0.5	7.0	0.5	8.0	0.5	8.4	ns
t_{OSHL}	Output to Output Skew		1.0					ns
t_{OSLH}	(Note 6)		1.0					

Note 6: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$ Typical	Units
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
		$C_L = 30$ pF, $V_{IH} = 2.5V$, $V_{IL} = 0V$	2.5	0.6	
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	−0.8	V
		$C_L = 30$ pF, $V_{IH} = 2.5V$, $V_{IL} = 0V$	2.5	−0.6	

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, V_I = 0V or V_{CC}	7	pF
C_{OUT}	Output Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}, f = 10 MHz	10	pF

AC LOADING and WAVEFORMS
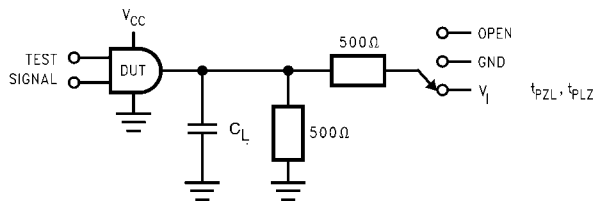
FIGURE 1. AC Test Circuit (C_L includes probe and jig capacitance)

Test	Switch
t_{PZL}, t_{PLZ}	6V at $V_{CC} = 3.3 \pm 0.3V$ V_{CC} x 2 at $V_{CC} = 2.5 \pm 0.2V$

3-STATE Output Low Enable and Disable Times for Logic

t_{rise} and t_{fall}
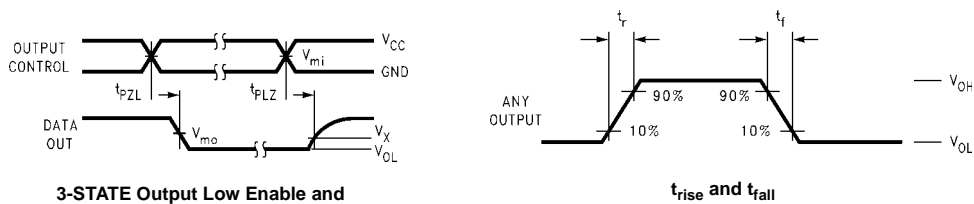
FIGURE 2. Waveforms
(Input Characteristics; f =1MHz, $t_r = t_f = 3ns$)

Symbol	V_{CC}		
	$3.3V \pm 0.3V$	$2.7V$	$2.5V \pm 0.2V$
V_{mi}	1.5V	1.5V	$V_{CC}/2$
V_{mo}	1.5V	1.5V	$V_{CC}/2$
V_x	$V_{OL} + 0.3V$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$
V_y	$V_{OH} - 0.3V$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$

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Schematic Diagram Generic for LCX Family (output pull-up circuitry is not applicable to open drain versions)
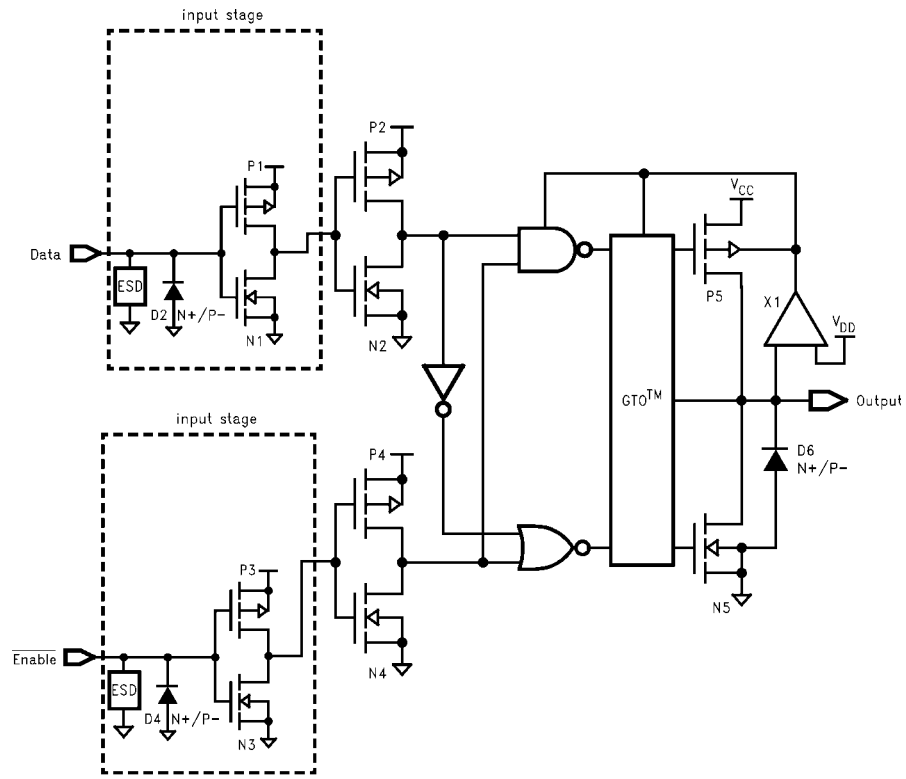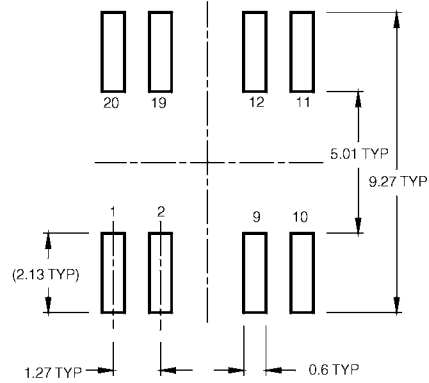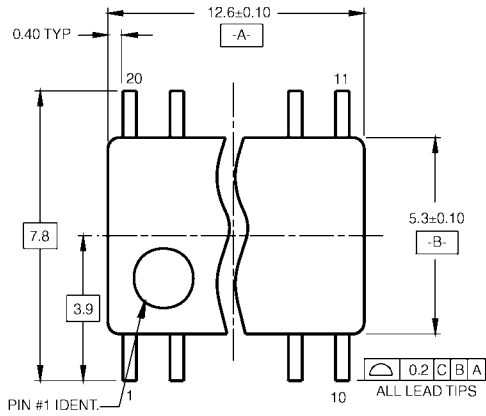

FIGURE 3.

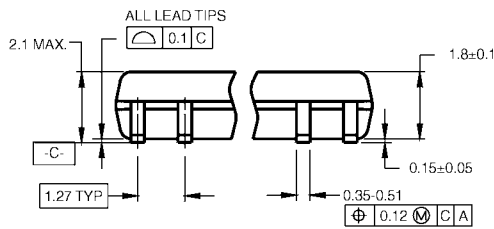# Physical Dimensions inches (millimeters) unless otherwise noted

0.496 − 0.512
(12.598 − 13.005)

20 19 18 17 16 15 14 13 12 11

0.394 − 0.419
(10.008 − 10.643)

LEAD NO. 1
IDENT

1 2 3 4 5 6 7 8 9 10

30° TYP

0.010 MAX
(0.254)

0.291 − 0.299
(7.391 − 7.595)

0.010 − 0.029
(0.254 − 0.737) × 45°

8° MAX TYP
ALL LEADS

0.009 − 0.013
(0.229 − 0.330)
TYP ALL LEADS

0.004
(0.102)
ALL LEAD TIPS

0.016 − 0.050
(0.406 − 1.270)
TYP ALL LEADS

0.093 − 0.104
(2.362 − 2.642)

0.004 − 0.012
(0.102 − 0.305)

SEATING
PLANE

0.014
(0.356)

0.050
(1.270)
TYP

0.008 TYP
(0.203)

0.014 − 0.020 TYP
(0.356 0.508)

M20B (REV F)
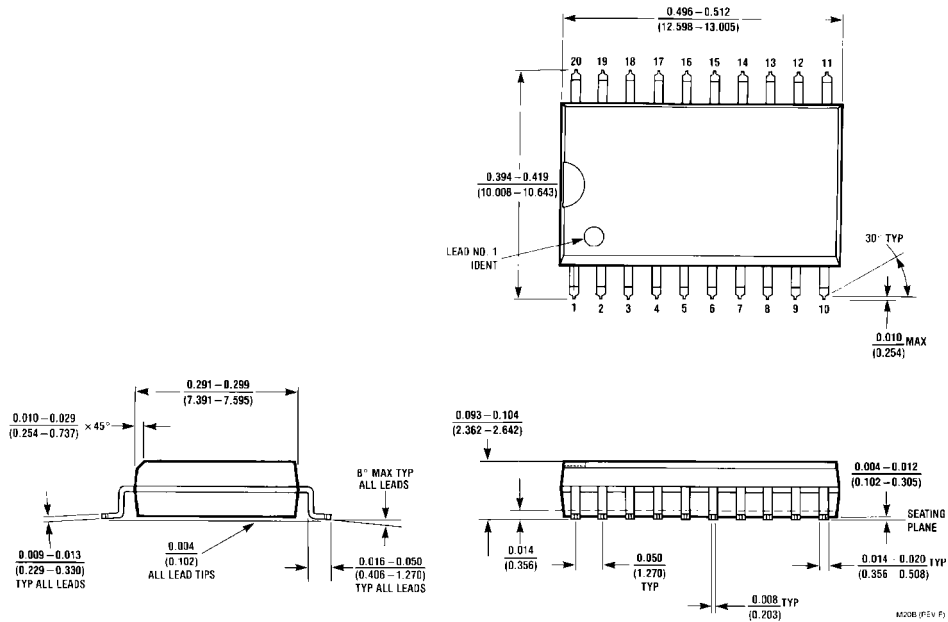
20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

12.6±0.10
-A-
0.40 TYP
20
11
7.8
5.3±0.10
-B-
3.9
0.2 C B A
ALL LEAD TIPS
PIN #1 IDENT.
1
10

LAND PATTERN RECOMMENDATION

20 19   12 11
5.01 TYP
9.27 TYP
1   2   9   10
(2.13 TYP)
1.27 TYP   0.6 TYP

ALL LEAD TIPS
0.1 C
2.1 MAX.
1.8±0.1
-C-
0.15±0.05
1.27 TYP
0.35-0.51
⊕ 0.12 Ⓜ C A

DIMENSIONS ARE IN MILLIMETERS

SEE DETAIL A
0.15-0.25
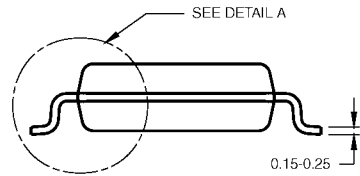
NOTES:
A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
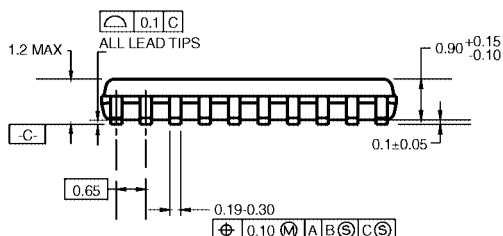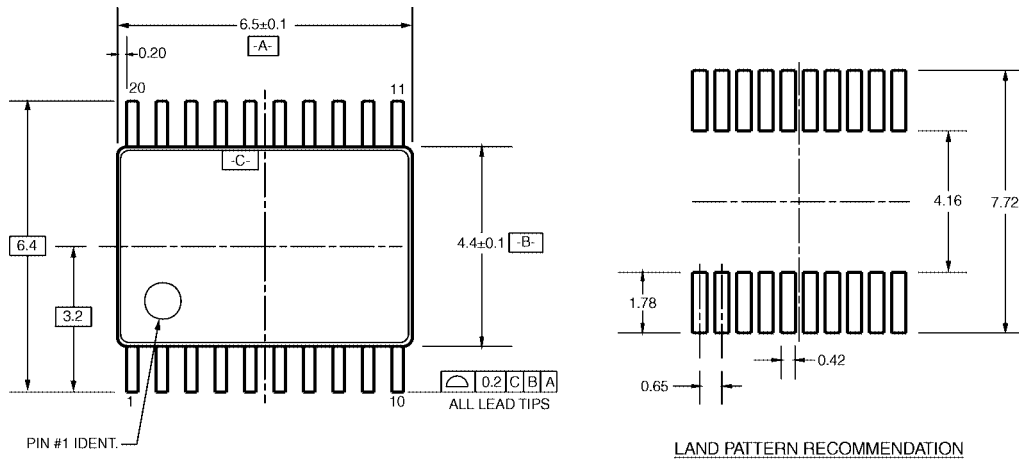
M20DRevB1

7° TYP
GAGE PLANE
0°-8° TYP
0.25
0.60±0.15
1.25
SEATING PLANE

DETAIL A

20-Lead Small Outline Package (SOP), EIAJ TYPE II, 4.4mm Wide
Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)
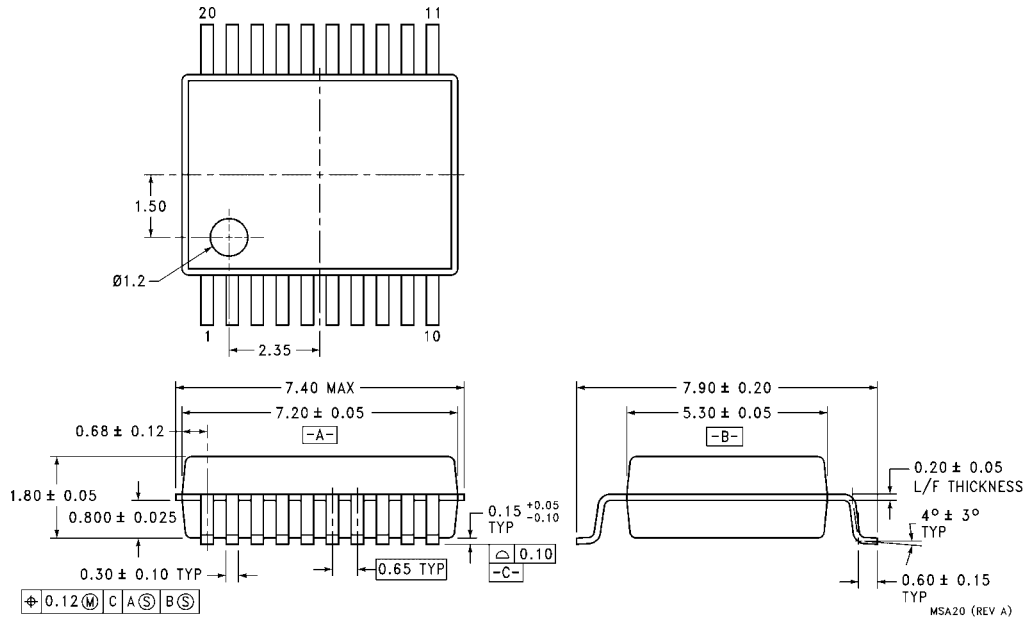
20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
Package Number MSA20

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

6.5±0.1
-A-

0.20

20   11

-C-

6.4   4.4±0.1 -B-

3.2

0.2 C B A
1   10
ALL LEAD TIPS

PIN #1 IDENT.

4.16   7.72

1.78

0.65   0.42

LAND PATTERN RECOMMENDATION

0.1 C
ALL LEAD TIPS
1.2 MAX

0.90 +0.15 -0.10

-C-

0.1±0.05

0.65

0.19-0.30

0.10 M A B S C S
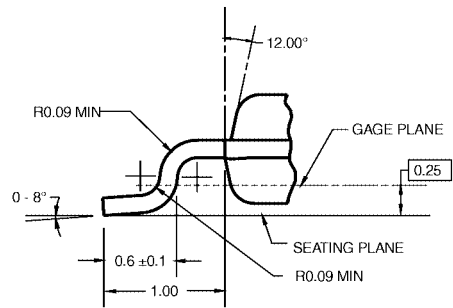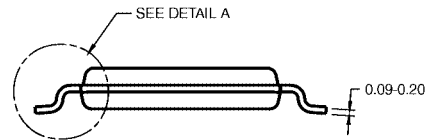
DIMENSIONS ARE IN MILLIMETERS

NOTES:
A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC,
   REF NOTE 6, DATE 7/93.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND
   TIE BAR EXTRUSIONS.
D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20RevD1

SEE DETAIL A

0.09-0.20

12.00°

R0.09 MIN   GAGE PLANE

0.25

0 - 8°

0.6 ±0.1   SEATING PLANE
1.00   R0.09 MIN

DETAIL A

20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20

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