FAIRCHILD SEMICONDUCTOR™

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74LVTH32952
Low Voltage 32-Bit Registered Transceiver with 3-STATE Outputs (Preliminary)

General Description

The LVTH32952 is a 32-bit registered transceiver. Four 8-bit back to back registers store data flowing in both directions between two bidirectional buses. Separate clock, clock enable, and output enable signals are provided for each register.

The LVTH32952 data inputs include bushold, eliminating the need for external pull-up resistors to hold unused inputs.

The registered transceiver is designed for low voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment.

The LVTH32952 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining low power dissipation.

Features

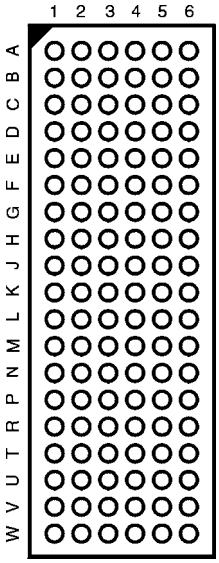
- Input and output interface capability to systems at 5V V_{CC}
- Bushold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink –32 mA/+64 mA
- ESD performance:
  - Human-body model > 2000V
  - Machine model > 200V
  - Charged-device model > 1000V
- Packaged in plastic Fine-Pitch Ball Grid Array (FBGA) (Preliminary)

Ordering Code:

Order Number	Package Number	Package Description
74LVTH32952GX (Note 1)	BGA114A (Preliminary)	114-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide [TAPE and REEL]

Note 1: BGA package available in Tape and Reel only.

Connection Diagram



(Top Thru View)

Truth Table

(Note 2)

Inputs				Internal Register	Output
A	**$CPAB_n$**	**$\overline{CEA}_n$**	**$\overline{OEAB}_n$**	**Value**	**B**
X	X	H	L	NC	B_0
X	X	H	H	NC	Z
L	⌐	L	L	L	L
L	⌐	L	H	L	Z
H	⌐	L	L	H	H
H	⌐	L	H	H	Z
X	L	X	L	NC	B_0
X	H	X	L	NC	B_0
X	L	X	H	NC	Z
X	H	X	H	NC	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = Output High Impedance
⌐ = LOW-to-HIGH Transition.
NC = No Change (state established by last valid CP)
B_0 = State established by last valid CP

Note 2: A to B data flow shown; B to A flow control is the same, but uses $\overline{OEBA}_n$, $CPBA_n$ and $\overline{CEB}_n$.

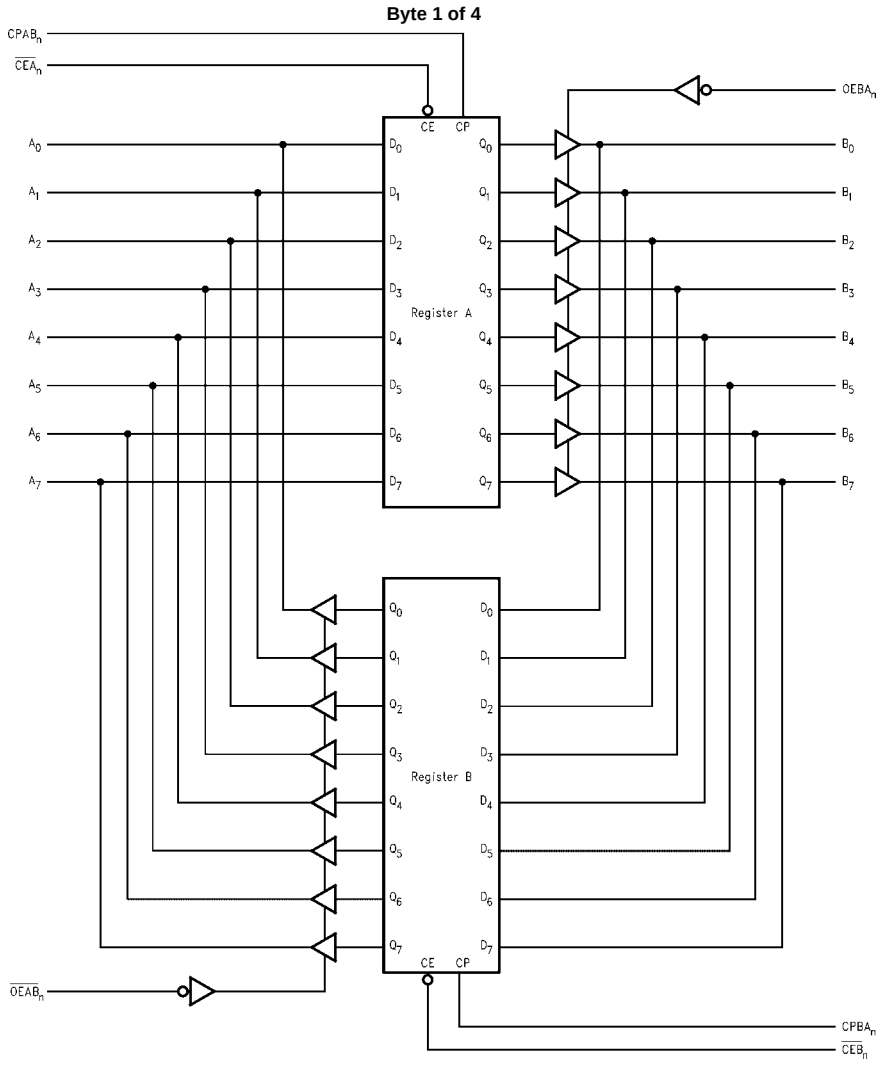
Pin Descriptions

Pin Names	Description
A_0–A_{31}	Data Register A Inputs B-Register 3-STATE Outputs
B_0–B_{31}	Data Register B Inputs A-Register 3-STATE Outputs
$CPAB_n$, $CPBA_n$	Clock Pulse Inputs
$\overline{CEA}_n$, $\overline{CEB}_n$	Clock Enable
$\overline{OEAB}_n$, $\overline{OEBA}_n$	Output Enable Inputs

Pin Assignments for FBGA

	1	2	3	4	5	6
A	A_0	$\overline{CEA}_1$	$CPAB_1$	$CPBA_1$	$\overline{CEB}_1$	B_0
B	A_2	A_1	$\overline{OEAB}_1$	$\overline{OEBA}_1$	B_1	B_2
C	A_4	A_3	GND	GND	B_3	B_4
D	A_6	A_5	V_{CC1}	V_{CC1}	B_5	B_6
E	A_8	A_7	GND	GND	B_7	B_8
F	A_{10}	A_9	GND	GND	B_9	B_{10}
G	A_{12}	A_{11}	V_{CC1}	V_{CC1}	B_{11}	B_{12}
H	A_{13}	A_{14}	GND	GND	B_{14}	B_{13}
J	A_{15}	$\overline{CEA}_2$	$CPAB_2$	$CPBA_2$	$\overline{CEB}_2$	B_{15}
K	NC	$CPAB_3$	$\overline{OEAB}_2$	$\overline{OEBA}_2$	$CPBA_3$	NC
L	A_{16}	$\overline{CEA}_3$	$\overline{OEAB}_3$	$\overline{OEBA}_3$	$\overline{CEB}_3$	B_{16}
M	A_{18}	A_{17}	GND	GND	B_{17}	B_{18}
N	A_{20}	A_{19}	V_{CC2}	V_{CC2}	B_{19}	B_{20}
P	A_{22}	A_{21}	GND	GND	B_{21}	B_{22}
R	A_{24}	A_{23}	GND	GND	B_{23}	B_{24}
T	A_{26}	A_{25}	V_{CC2}	V_{CC2}	B_{25}	B_{26}
U	A_{28}	A_{27}	GND	GND	B_{27}	B_{28}
V	A_{29}	A_{30}	$\overline{CPAB}_4$	$\overline{CPBA}_4$	B_{30}	B_{29}
W	A_{31}	$\overline{CEA}_4$	$\overline{OEAB}_4$	$\overline{OEBA}_4$	$\overline{CEB}_4$	B_{31}

Logic Diagram



n = 1 for Byte 1, n = 2 for Byte 2, etc.

Byte 1: A_0 - A_7, B_0 - B_7

Byte 2: A_8 - A_{15}, B_8 - B_{15}

Byte 3: A_{16} - A_{23}, B_{16} - B_{23}

Byte 4: A_{24} - A_{31}, B_{24} - B_{31}

V_{CC1} is associated with Bytes 1 and 2

V_{CC2} is associated with Bytes 3 and 4

Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 3)

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +4.6		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in 3-STATE	V
		−0.5 to +7.0	Output in HIGH or LOW State (Note 4)	V
I_{IK}	DC Input Diode Current	–50	$V_I < GND$	mA
I_{OK}	DC Output Diode Current	–50	$V_O < GND$	mA
I_O	DC Output Current	64	$V_O > V_{CC}$ Output at HIGH State	mA
		128	$V_O > V_{CC}$ Output at LOW State	
I_{CC}	DC Supply Current per Supply Pin	±64		mA
I_{GND}	DC Ground Current per Ground Pin	±128		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	2.7	3.6	V
V_I	Input Voltage	0	5.5	V
I_{OH}	HIGH Level Output Current		−32	mA
I_{OL}	LOW Level Output Current		64	
T_A	Free-Air Operating Temperature	−40	+85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V	0	10	ns/V

Note 3: Absolute Maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rated conditions is not implied.

Note 4: I_O Absolute Maximum Rating must be observed.

DC Electrical Characteristics

Symbol	Parameter		V_{CC} (V)	T_A = −40°C to +85°C Min	T_A = −40°C to +85°C Max	Units	Conditions
V_{IK}	Input Clamp Diode Voltage		2.7		−1.2	V	I_I = −18 mA
V_{IH}	Input HIGH Voltage		2.7–3.6	2.0		V	$V_O \le 0.1V$ or
V_{IL}	Input LOW Voltage		2.7–3.6		0.8		$V_O \ge V_{CC} - 0.1V$
V_{OH}	Output HIGH Voltage		2.7–3.6	V_{CC} − 0.2		V	I_{OH} = −100 µA
			2.7	2.4		V	I_{OH} = −8 mA
			3.0	2.0		V	I_{OH} = −32 mA
V_{OL}	Output LOW Voltage		2.7		0.2	V	I_{OL} = 100 µA
			2.7		0.5	V	I_{OL} = 24 mA
			3.0		0.4	V	I_{OL} = 16 mA
			3.0		0.5	V	I_{OL} = 32 mA
			3.0		0.55	V	I_{OL} = 64 mA
$I_{I(HOLD)}$	Bushold Input Minimum Drive		3.0	75		µA	V_I = 0.8V
				−75		µA	V_I = 2.0V
$I_{I(OD)}$	Bushold Input Over-Drive		3.0	500		µA	(Note 5)
	Current to Change State			−500		µA	(Note 6)
I_I	Input Current		3.6		10	µA	V_I = 5.5V
		Control Pins	3.6		±1	µA	V_I = 0V or V_{CC}
		Data Pins	3.6		−5	µA	V_I = 0V
					1	µA	$V_I = V_{CC}$
I_{OFF}	Power Off Leakage Current		0		±100	µA	$0V \le V_I$ or $V_O \le 5.5V$
$I_{PU/PD}$	Power Up/Down 3-STATE		0–1.5V		±100	µA	V_O = 0.5V to 3.0V
	Output Current						V_I = GND or V_{CC}
I_{OZL}	3-STATE Output Leakage Current		3.6		−5	µA	V_O = 0.0V
I_{OZH}	3-STATE Output Leakage Current		3.6		5	µA	V_O = 3.6V
I_{OZH+}	3-STATE Output Leakage Current		3.6		10	µA	$V_{CC} < V_O \le 5.5V$

DC Electrical Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	$T_A = -40°C$ to $+85°C$		Units	Conditions
			Min	Max		
I_{CCH}	Power Supply Current V_{CC1} or V_{CC2}	3.6		0.19	mA	Outputs High
I_{CCL}	Power Supply Current V_{CC1} or V_{CC2}	3.6		5	mA	Outputs Low
I_{CCZ}	Power Supply Current V_{CC1} or V_{CC2}	3.6		0.19	mA	Outputs Disabled
$I_{CCZ}+$	Power Supply Current V_{CC1} or V_{CC2}	3.6		0.19	mA	$V_{CC} \le V_O \le 5.5V$, Outputs Disabled
ΔI_{CC}	Increase in Power Supply Current (Note 7) V_{CC1} or V_{CC2}	3.6		0.2	mA	One Input at $V_{CC} - 0.6V$ Other Inputs at V_{CC} or GND

Note 5: An external driver must source at least the specified current to switch from LOW-to-HIGH.

Note 6: An external driver must sink at least the specified current to switch from HIGH-to-LOW.

Note 7: This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

Dynamic Switching Characteristics (Note 8)

Symbol	Parameter	V_{CC} (V)	$T_A = 25°C$			Units	Conditions $C_L = 50$ pF, $R_L = 500\Omega$
			Min	Typ	Max		
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3		0.8		V	(Note 9)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3		−0.8		V	(Note 9)

Note 8: Characterized in SSOP package. Guaranteed parameter, but not tested.

Note 9: Max number of outputs defined as (n). n–1 data inputs are driven 0V to 3V. Output under test held LOW.

AC Electrical Characteristics

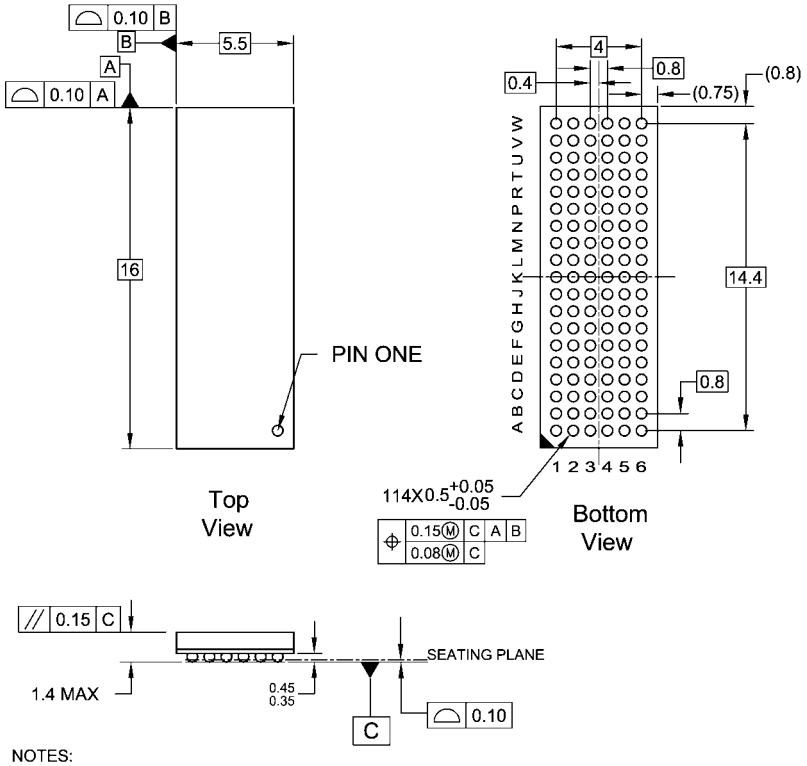
Symbol	Parameter		$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF, $R_L = 500\Omega$				Units
			$V_{CC} = 3.3 \pm 0.3V$		$V_{CC} = 2.7V$		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		150		150		MHz
t_{PLH}	Propagation Delay		1.3	4.4	1.3	4.7	ns
t_{PHL}	CPBA or CPAB to A or B		1.3	4.8	1.3	5.0	
t_{PZH}	Output Enable Time		1.0	4.3	1.0	4.9	ns
t_{PZL}	$\overline{OE}$ to A or B		1.0	4.8	1.0	5.7	
t_{PHZ}	Output Disable Time		2.1	5.7	2.1	6.2	ns
t_{PLZ}	$\overline{OE}$ to A or B		2.1	5.1	2.1	5.3	
t_W	Pulse Width, CPAB or CPBA HIGH or LOW		3.3		3.3		ns
t_S	Setup Time	A or B before CPAB or CPBA	1.7		2.5		ns
		$\overline{CEA}$ or $\overline{CEB}$ before CPAB or CPBA	2.0		2.8		
t_H	Hold Time	A or B after CPAB or CPBA	0.8		0.0		ns
		$\overline{CEA}$ or $\overline{CEB}$ after CPAB or CPBA	0.4		0.0		

Capacitance (Note 10)

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = OPEN, V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	Input/Output Capacitance	V_{CC} = 3.0V, V_O = 0V or V_{CC}	8	pF

Note 10: Capacitance is measured at frequency f = 1 MHz, per MIL-STD-883, Method 3012.

Physical Dimensions inches (millimeters) unless otherwise noted



NOTES:

A. THIS PACKAGE CONFORMS TO JEDEC M0-205
B. ALL DIMENSIONS IN MILLIMETERS
C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA114ArevE

114-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
Package Number BGA114A
Preliminary

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