FAN5038

Dual Voltage Controller for DSP Power

Features

- Provides complete, low-cost core and I/O power in single chip
- I/O power sequencing
- Core voltage adjustable from 1.5V to 3.6V
- Independent adjustable current limits
- Core up to 13A, I/O up to 5A
- Precision trimmed low TC voltage reference
- Constant On-Time oscillator
- Small footprint 16 lead SOIC package

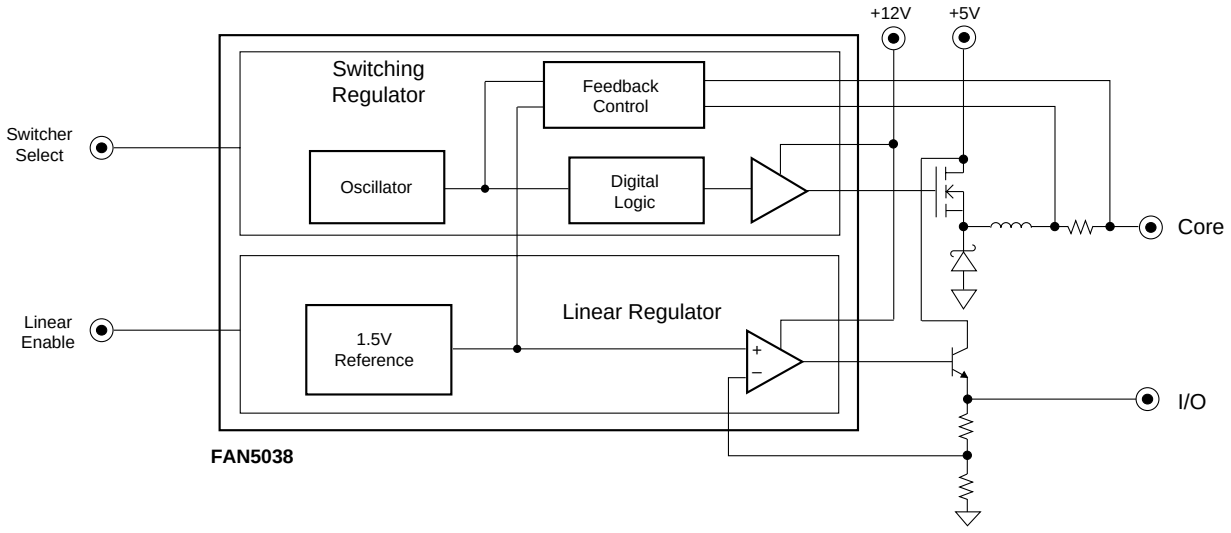
Applications

- High efficiency low-cost power for DSPs
- Power for ASICs and FPGAs
- Programmable dual power supply for high current loads

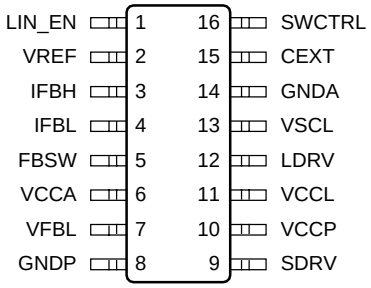
Description

The FAN5038 provides a complete low-cost power system for DSPs and other loads requiring high-performance. The FAN5038 combines an adjustable switch-mode DC-DC converter for core power with a low-dropout linear regulator for I/O power in a space-saving SO-16 package. Simple external circuitry provides power sequencing and independent current limits. An internal precision voltage reference allows the switcher to be adjusted from 1.5V to 3.6V. With the appropriate external components, the FAN5038 can deliver core power up to 13A, and I/O power up to 5A, allowing multiple DSPs to be powered with a single device.

Block Diagram



Pin Assignments



Pin Descriptions

Pin Name	Pin Number	Pin Function Description
LIN_EN	1	**Linear regulator enable input.** Accepts TTL/open collector input levels. A logic level HIGH on this pin disables the output of the linear regulator.
VREF	2	**Voltage reference test point.** This pin provides access to the internal precision 1.5V bandgap reference and should be decoupled to ground using a 0.1µF ceramic capacitor. No load should be connected to this pin.
IFBH	3	**High side current feedback for switching regulator.** Pins 3 and 4 are used as the inputs for the current feedback control loop and as the short circuit current sense points. Careful layout of the traces from these pins to the current sense resistor is critical for optimal performance of the short circuit protection scheme. See Applications Discussion for details.
IFBL	4	**Low side current feedback for switching regulator.** See Applications Discussion for details.
FBSW	5	**Voltage feedback for switching regulator.** This input is active when a logic level LOW is input on pin 16 (SWCTRL). Using two external resistors, it sets the output voltage level for the switching regulator. See Applications Discussion for details.
VCCA	6	**Switching Regulator V_{CC}.** Power supply for switching regulator control circuitry and voltage reference. Connect to system 5V supply and decouple to ground with 0.1µF ceramic capacitor.
VFBL	7	**Voltage feedback for linear regulator.** Using two external resistors, this pin sets the output voltage level for the linear regulator. See Applications Discussion for details.
GNDP	8	**Power Ground.** Return pin for high currents flowing in pins 9, 10 and 12 (SDRV, VCCP and LDRV). Connect to a low impedance ground. See Applications Discussion for details.
SDRV	9	**FET driver output for switching regulator.** Connect this pin to the gate of the N-channel MOSFET Q1 as shown in Figure 1. The trace from this pin to the MOSFET gate should be kept as short as possible (less than 0.5"). See Applications Discussion for details.
VCCP	10	**Switching regulator gate drive V_{CC}.** Power supply for SDRV output driver. Connect to system 12V supply with R-C filter shown in Figure 1. See Applications Discussion for details.
VCCL	11	**Linear Regulator Vcc.** Power supply for LDRV output op-amp. Connect to system 12V supply and decouple to ground with 0.1µF ceramic capacitor.
LDRV	12	**Output driver for linear regulator.** Connect this pin to the base of an NPN transistor. When pin 1 (LIN_EN) is pulled HIGH, the linear regulator is disabled and pin 12 will be pulled low internally.
VSCL	13	**Low side current sense for linear regulator.** Connect this pin between the sense resistor and the collector of the power transistor. The high side current sense is internally connected to pin 6 (VCCA). Layout is critical to optimal performance of the linear regulator short circuit protection scheme. See Applications Discussion for details.

Pin Descriptions (continued)

Pin Name	Pin Number	Pin Function Description
GNDA	14	**Analog ground.** All low power internal circuitry returns to this pin. This pin should be connected to system ground so that ground loops are avoided. See Applications Discussion for details.
CEXT	15	**External capacitor.** A 100pF capacitor is connected to this pin as part of the constant on-time pulse width circuit. Careful layout of this pin is critical to system performance. See Applications Discussion for details.
SWCTRL	16	**Switching regulator control input.** Accepts TTL/open collector input levels. A logic level HIGH on this pin presets the switching regulator output voltage at 3.5V using internal resistors. A logic level LOW on this pin will select the output voltage set by two external resistors and the voltage feedback control pin 5 (VFBSW). See Applications Discussion for details.

Absolute Maximum Ratings

Supply Voltages, VCCA, VCCL, VCCP	13V
Junction Temperature, T_J	+150°C
Storage Temperature, T_S	-65 to +150°C
Lead Soldering Temperature, 10 seconds	300°C
Thermal Resistance Junction-to-Ambient, Θ_{JA}	112°C/W

Note:
1. Functional operation under any of these conditions is not implied. Performance is guaranteed only if Operating Conditions are not exceeded.

Operating Conditions

Parameter	Conditions	Min.	Typ.	Max.	Units
Switching Regulator V_{CC}, VCCA		4.75	5	5.25	V
Linear Regulator V_{CC}, VCCL		11.4	12	12.6	V
Logic Inputs, SWCTRL, LIN_EN	Logic HIGH Logic LOW	2.4		 0.8	V V
Ambient Operating Temperature, T_A		0		70	°C
Drive Gate Supply, V_{CCP}		9.5	12	12.6	V

Electrical Characteristics—Switch-Mode Regulator

(VCCA = 5V, VCCL = 12V, T_A = 25°C using circuit of Figure 1, unless otherwise noted)

The • denotes specifications which apply over the full ambient operating temperature range.

Parameter	Conditions		Min.	Typ.	Max.	Units
Output Voltage, VOSW[1]	SWCTRL = HIGH Set by internal resistors	•		3.5		V
Output Voltage, VOSW[1]	SWCTRL = LOW Set by external resistors	•	1.5		3.6	V
Setpoint Accuracy[2]	I_{SW} = 4A		-1.2		+1.2	%Vo
Output Temperature Drift	T_A = 0°C–70°C	•		40		ppm
Line Regulation	VCCA = 4.75 to 5.25V I_{SW} = 4A			0.10	0.15	%Vo
Load Regulation	I_{SW} = 0 to 4A			±0.9	±1.3	%Vo
Output Ripple, peak-peak	20MHz BW, I_{SW} = 4A			15		mV
Cumulative DC Accuracy[3]		•		±55	±100	mV
Efficiency	I_{SW} = 4A			80		%
Output Driver Current	Open Loop	•	0.5			A
Short Circuit Threshold Voltage		•	70	90	100	mV
On Time Pulse Width[4]	C_{EXT} = 100pF			2		µs

Notes:

1. When the SWCTRL pin is HIGH or left open, the switch-mode regulator output will be preset at 3.5V using internal precision resistors. When the SWCTRL pin is LOW, the output voltage may be programmed with external resistors. Please refer to the Applications Section for output voltage selection information.
2. Setpoint accuracy is the initial output voltage variability under the specified conditions. When SWCTRL is LOW, the matching of the external resistors will have a major influence on this parameter.
3. Cumulative DC accuracy includes setpoint accuracy, temperature drift, line and load regulation, and output ripple.
4. The on-time pulse width of the oscillator is preset using external capacitor C_{EXT}. See Typical Operating Characteristics curves.

Electrical Characteristics—Linear Regulator

(VCCA = 5V, VCCL = 12V, T_A = 25°C using circuit in Figure 1, unless otherwise noted)

The • denotes specifications which apply over the full ambient operating temperature range.

Parameter	Conditions		Min	Typ	Max	Units
Output Voltage, VOL[1]	Set by external resistors	•	1.5		3.6	V
Setpoint Accuracy[2]	I_L=0.5A, using 0.1% resistors		-1.5		+1.5	%
Output Temperature Drift		•		40		ppm
Line Regulation	VCCL = 11.4V to 12.6V, I_L = 0.5A			0.1	0.15	%Vo
Load Regulation	I_L = 0 to 5A			±0.7	±1	%Vo
Output Noise	0.1 to 20KHz			1		mV
Cumulative DC Accuracy[3]		•		±1.7	±3	%
Crosstalk[4]	I_{SW} = 4A			35		mVpp
Short Circuit Comparator Threshold		•	40	50	60	mV
Op-amp Output Current	Open Loop		50	70		mA

Notes:

1. When the LIN_EN pin is LOW, the linear regulator output is set with external resistors. When the LIN_EN pin is HIGH, the linear regulator is disabled and will exhibit no output voltage. Please refer to the Application Section for output voltage selection information.
2. Setpoint accuracy is the initial output voltage variability under the specified conditions. The matching of the external resistors will have a major influence on this parameter.
3. Cumulative DC accuracy includes setpoint accuracy, temperature drift, line and load regulation.
4. Crosstalk is defined as the amount of switching noise from the switch-mode regulator that appears on the output of the linear regulator when both outputs are in a static load condition.

Electrical Characteristics—Common

(VCCA = 5V, VCCL = 12V, T_A = 25°C using circuit of Figure 1, unless otherwise noted)

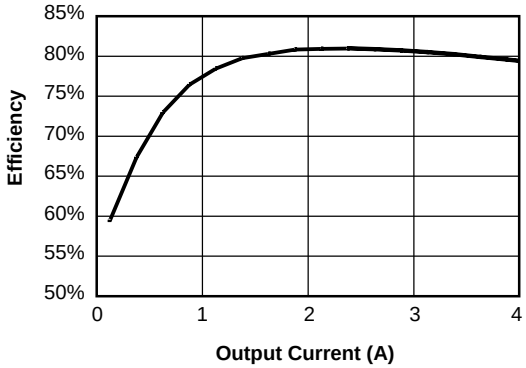
The • denotes specifications which apply over the full ambient operating temperature range.

Parameter	Conditions		Min	Typ	Max	Units
Reference Voltage, VREF			1.485	1.5	1.515	V
VREF PSRR			60			dB
VCCA Supply Current	Independent of load	•		5	15	mA
VCCP Supply Current	I_{SW} = 4A	•		20	25	mA
VCCL Supply Current	I_L = 2A	•		5		mA

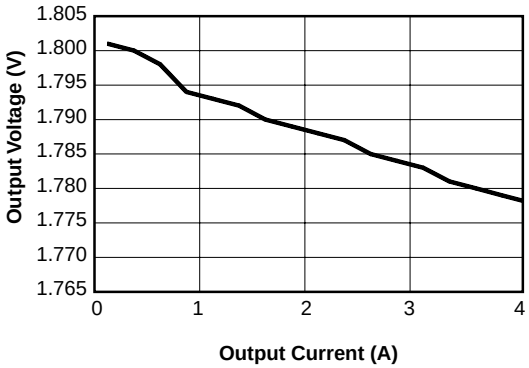
Typical Operating Characteristics

(VCCA = 5V, VCCL = 12V and T_A = +25°C using circuit in Figure 1, unless otherwise noted)

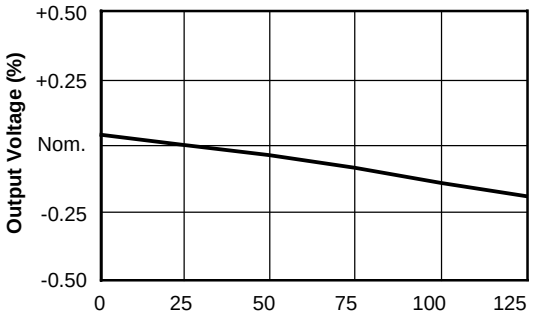
Switcher Efficiency vs. Output Current



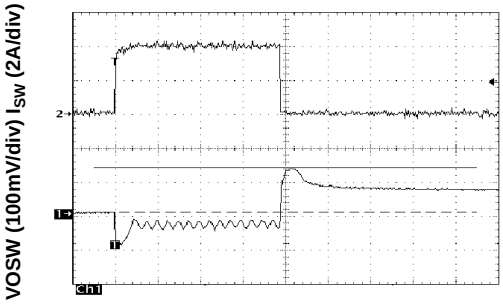
Switcher Output Voltage vs. Load



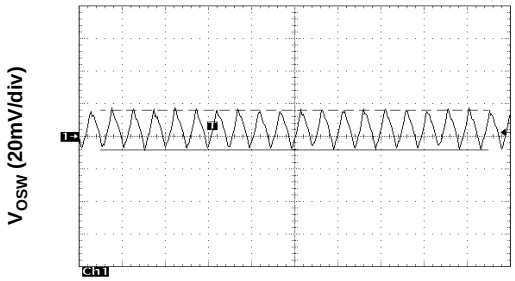
Output Voltage vs. Temperature, I_{SW} = 5A or I_{LR} = 5A



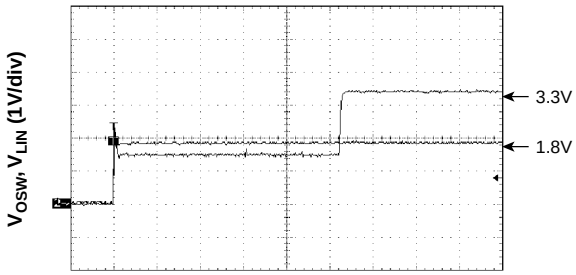
Switcher Transient Response, 0 to 4A



Switcher Output Ripple, I_{OUT} = 4A



System Power-Up



Application Circuit

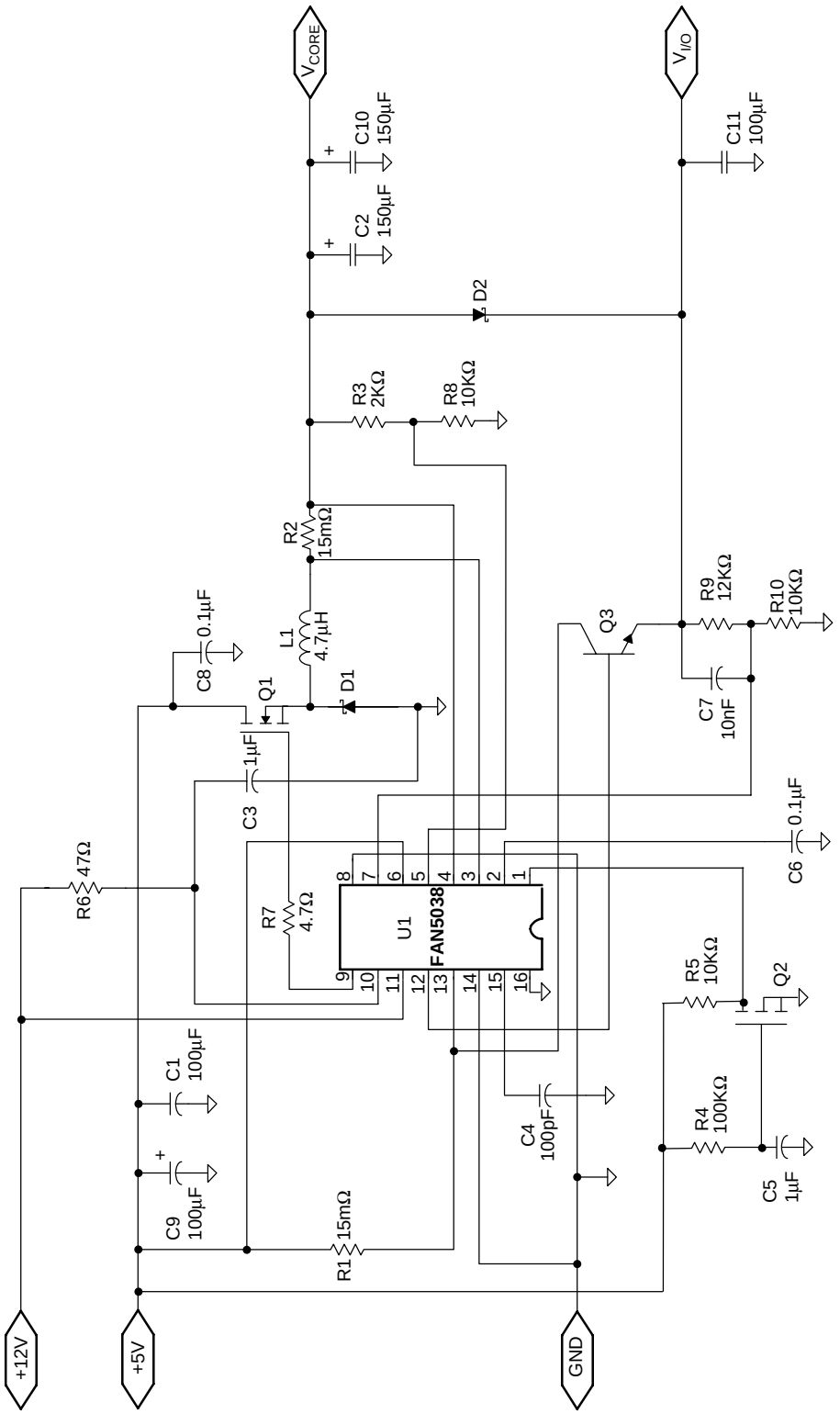


Figure 1. DSP Power, 4A Core, 500mA I/O

Table1. Bill of Materials for a FAN5038 DSP Application

Reference	Manufacturer Part #	Qty.	Description	Requirements and Comments
C1, C9, C11	Sanyo 10TPB100M	3	100µF, 10V Capacitor	I_{RMS} = 1.9A
C2, C10	Sanyo 6TPB150M	2	150µF, 6V Capacitor	ESR ≤ 55mΩ
C3, C5	Panasonic ECU-V1C105ZFX	2	1µF, 16V Capacitor	
C4	Panasonic ECU-V1H101JCG	1	100pF Capacitor	5%, COG
C6, C8	Panasonic ECU-V1C104ZFX	2	100nF, 16V Capacitor	
C7	Panasonic ECU-V1C103ZFX	1	10nF, 16V Capacitor	
D1	Motorola MBRS835	1	8A Schottky Diode	
D2	Fairchild MBRS320	1	3A Schottky Diode	
L1	Any	1	4.7µH, 4A Inductor	DCR ~ 2mΩ
Q1	Fairchild NDS8425	1	N-Channel MOSFET	$R_{DS(ON)}$ = 25mΩ @ V_{GS} = 4.5V
Q2	Fairchild FDV301N	1	N-Channel MOSFET	
Q3	Fairchild MJD200	1	NPN	40V, 5A
R1-2	Dale WSL2010R015FRE4	2	15mΩ, 1/2W	
R3	Any	1	2KΩ	
R4	Any	1	100KΩ	
R5, R8, R10	Any	3	10KΩ	
R7	Any	1	4.7KΩ	
R8	Any	1	6.49KΩ	
R9	Any	1	12KΩ	
U1	Fairchild FAN5038M	1	DC/DC Controller	

Application Information

The FAN5038 contains a precision trimmed low TC voltage reference, a constant-on-time architecture controller, a high current switcher output driver, a low offset op-amp, and switches for selecting various output modes. The block diagram in Figure 2 shows how the FAN5038 in combination with the external components achieves a dual power supply for DSP power.

Switch-Mode Control Loop

The main control loop for the switch-mode converter consists of a current conditioning amplifier and one of the two voltage conditioning amplifiers that take the raw voltage and current information from the regulator output, compare them against the precision reference and present the error signal to the input of the constant-on-time oscillator. The two voltage conditioning amplifiers act as an analog switch to select between the internal resistor divider network (set for 3.5V) or an external resistor divider network (adjustable for 1.5V to 3.6V.) The switch-mode select pin determines which of the two amplifiers is selected. The current feedback signals come across the Iout sense resistor to the IFBH and IFBL inputs of the FAN5038. The error signals from both the current feedback loop and the voltage feedback loop are summed together and used to control the off-time duration of the oscillator. The current feedback error signal is also used as part of the FAN5038 short-circuit protection.

Linear Control Loop

The low-offset op-amp is configured to be the controlling element in a precision low-drop-out linear regulator. As can be seen from Figure 2, the op-amp is used to compare the divided down output of the linear regulator to the precision reference. The error signal is used to control either an N-channel MOSFET or a power NPN transistor.

High Current Output Drivers

The FAN5038 switching high current output driver (SDRV) contains high speed bipolar power transistors configured in a push-pull configuration. The output driver is capable of supplying 0.5A of current in less than 100ns. The driver's power and ground are separated from the overall chip power and ground for added switching noise immunity.

Internal Reference

The reference in the FAN5038 is a precision band-gap type reference. Its temperature coefficient is trimmed to provide a near zero TC. For guaranteed stable operation under all conditions, a 0.1µF capacitor is recommended on the VREF output pin. No load may be attached to this pin.

Constant-On-Time Oscillator

The FAN5038 switch-mode oscillator is designed as a fixed on-time, variable off-time oscillator. The constant-on-time oscillator consists of a comparator, an external capacitor, a fixed current source, a variable current source, and an analog switch that selects between two threshold voltages for the comparator. The external timing capacitor is alternately charged and discharged through the enabling and disabling of the fixed current source. The variable current source is controlled from the error inputs that are received from the current and voltage feedback signals. The oscillator off-time is controlled by the amount of current that is available from the variable current source to charge the external capacitor up to the high threshold level of the comparator. The on-time is set be the constant current source that discharges the external capacitor voltage down to the lower comparator threshold.

Using SWCTRL and LIN_EN

When the SWCTRL pin is HIGH, the switching regulator will set its output at 3.5V using two internal precision resistors. When this pin is LOW, the switching regulator output can be set to any voltage between 1.5V and 3.6V using external precision resistors. The LIN_EN pin is used to enable or disable the linear regulator. When the LIN_EN pin is HIGH, the linear regulator will be disabled. If this pin is LOW, the linear regulator output can be set from 1.5V to 3.5V using external precision resistors.

Power Sequencing

The linear regulator output can be sequenced with the circuit shown in Figure 1. The combination R4 = 100KΩ and CS = 1µF sets a delay of approximately 25 msec. Diode D2 prevents core voltage from exceeding I/O voltage, so that I/O tracks core until after the delay.

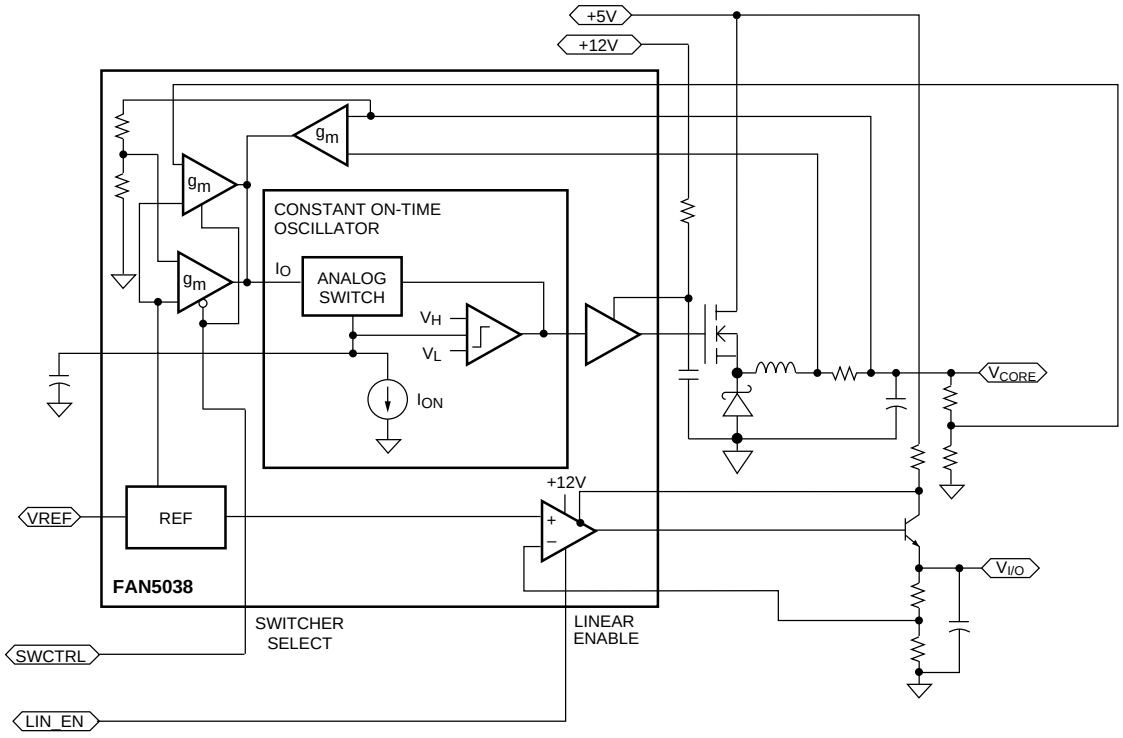


Figure 2. FAN5038 Block Diagram

Output Voltage Selection

The FAN5038 precision reference is trimmed to be 1.5V nominally. When using the FAN5038, the system designer has complete flexibility in choosing the output voltage for each regulator from 1.5V to 3.6V. This is done by appropriately selecting the feedback resistors. These could be 0.1% resistors to realize optimum output accuracy. The following equations determine the output voltages of the two regulators:

Switching Regulator:

$$V_{OUT} = 1.5 \times \left(\frac{R8 + R3}{R8}\right)$$

Linear Regulator:

$$V_{OUT} = 1.5 \times \left(\frac{R10 + R9}{R10}\right)$$

where R8 > 1.5kΩ and (R8 + R3) ≤ 25kΩ and R10 > 1.5kΩ and (R9 + R10) ≤ 25kΩ

Example:

For 3.3V,

$$V_{OUT} = 1.5 \times \left(\frac{R10 + R9}{R10}\right) = 1.5 \times \left(\frac{12k + 10k}{10k}\right) = 3.3V$$

Input Capacitors

The number of input capacitors required for the FAN5038 is dependent on their ripple current rating, which assures their rated life. The number required may be determined by

$$\text{No. Caps} = \frac{I_{out} * \sqrt{DC - DC^2}}{I_{rating}} \quad (2)$$

where the duty cycle DC = V_{out}/V_{in}. For example, with a 1.5V output at 4A, 5V input, and using the Sanyo capacitors specified in Table 1 which have a 1.9A ripple current rating, we have DC = 1.5/5 = 0.3, and

$$\text{No. Caps} = \frac{4 * \sqrt{0.3 - 0.3^2}}{1.9} = 0.96$$

so that we need 1 input capacitor.

Linear Regulator Design Considerations

Figure 1 shows the application schematic for the FAN5038 with an NPN used for the linear regulator.

Careful consideration must be given to the base current of the power NPN device. The base current to the power NPN device is limited by:

- The FAN5038 op-amp output current (50mA)
- The internal power dissipation of the FAN5038 package
- The β of the power NPN device.

The internal FAN5038 power dissipation is the most important limitation for this application. For optimum reliability, we require that the junction temperature not exceed 130°C; thus we can calculate the maximum power dissipation allowable for this 16-lead SOIC package as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\Theta JA}}$$

If we assume that the ambient temperature T_A is 70°C and the thermal resistance of the 16-lead SOIC package is 112°C/W, then the maximum power dissipation for the IC is:

$$P_D = \frac{130 - 70}{112} \leq 0.533W$$

$$P_D = P_{SW} + P_{LR} =$$

$$(35mA \times 5.25V) + (12.6V - V_{OUT} - V_{BE}) \times I_{OL} \leq 0.533W$$

where P_{SW} is the internal power dissipation of the switching regulator and P_{LN} is the internal power dissipation of the linear regulator. I_{OL} is the linear regulator op-amp output current. For V_{OUT} = 3.3V nominal, the worst case output will be determined by the current used.

For example, for a worst case V_{OUT} = 3.135V, the maximum op-amp output current is:

$$I_{OL} = \frac{0.533W - (35mA \times 5.25V)}{(12.6V - 3.135V - 0.8V)} \leq 40mA$$

$$\beta \geq \frac{500mA}{40mA} = 12.5$$

The power NPN transistor must have a minimum β of 12.5 at I_L = 500mA in order to meet the internal power dissipation limit of the 16-SOIC package.

Short Circuit Considerations

For the Switch-Mode Regulator

The FAN5038 uses a current sensing scheme to limit the load current if an output fault condition occurs. The current sense resistor carries the peak current of the inductor, which is greater than the maximum load current due to ripple currents flowing in the inductor. The FAN5038 will begin to limit the output current to the load by turning off the top-side FET driver when the voltage across the current-sense resistor exceeds the short circuit comparator threshold voltage (V_{th}). When this happens the output voltage will temporarily go out of regulation. As the voltage across the sense resistor becomes larger, the top-side MOSFET will continue to turn off until the current limit value is reached. At this point, the FAN5038 will continuously deliver the limit current at a reduced output voltage level. The short circuit comparator threshold voltage is typically 90mV, with a variability of +10/-20mV. The ripple current flowing through the inductor is typically 0.5A. Refer to Application Note AM-53 for detailed discussions. The sense resistor value can be approximated as follows:

$$R_{SENSE} = \frac{V_{th,min}}{I_{PK}} \times (1 - TF) = \frac{V_{th,min}}{0.5A + I_{LOAD,MAX}} \times (1 - TF)$$

where TF = Tolerance Factor for the sense resistor and 0.5A accounts for the inductor current ripple.

Since the value of the sense resistor is often less than 20mΩ, care should be taken in the layout of the PCB. Trace resistance can contribute significant errors. The traces to the IFBH and IFBL pins of the FAN5038 should be Kelvin connected to the pads of the current-sense resistor. To minimize the influence of noise, the two traces should be run next to each other.

For the Linear Regulator

The analysis for short circuit protection of the linear regulator is much simpler than that of the switching regulator. The formula for the inception point of short-circuit protection for the linear regulator is:

$$R_{SENSE} = \frac{V_{th,min}}{I_{LOAD,MAX}} \times (1 - TF)$$

V_{th} = 50mV ± 10mV and $I_{LOAD,MAX}$ = 500mA,

$$R_{SENSE} = \frac{40mV}{0.5A} \times (1 - 29\%) = 57m\Omega$$ for using an embedded PC trace resistor

$$R_{SENSE} = \frac{40mV}{0.5A} \times (1 - 5\%) = 76m\Omega$$ for using a discrete resistor

It should be noted that the presence of D2 in Figure 1 bypasses the short circuit protection of the linear regulator. If D2 is used and short circuit protection is desired, D2 must be rated to take the short circuit current of the switch-mode regulator.

Schottky Diode

In Figure 1, MOSFET Q1 and flyback diode D1 are used as complementary switches in order to maintain a constant current through the output inductor L1. As a result, D1 will have to carry the full current of the output load when the power MOSFET is turned off. The power in the diode is a direct function of the forward voltage at the rated load current during the off time of the FET. The following equation can be used to estimate the diode power:

$$P_{DIODE} = I_D \times V_D \times (1 - DutyCycle)$$

where I_D is the forward current of the diode, V_D is the forward voltage of the diode, and DutyCycle is defined the same as

$$\text{Duty Cycle} = \frac{Vout}{Vin}$$

For the Motorola MBRS835 Power Rectifier used in Figure 1,

$$P_{DIODE} = 4A \times 0.35 \times (1 - 36\%) = 0.9W$$

Board Design Considerations

FAN5038 Placement

Preferably the PC layer directly underneath the FAN5038 should be the ground layer. This serves as extra isolation from noisy power planes.

MOSFET Placement

Placement of the power MOSFET is critical in the design of the switch-mode regulator. The FET should be placed in such a way as to minimize the length of the gate drive path from the FAN5038 SDRV pin. This trace should be kept under 0.5" for optimal performance. Excessive lead length on this trace causes high frequency noise resulting from the parasitic inductance and capacitance of the trace. Since this voltage can transition nearly 12V in around 100nsec, the resultant ringing and noise will be very difficult to suppress. This trace should be routed on one layer only and kept well away from the “quiet” analog pins of the device: VREF, CEXT, FBSW, IFBH, IFBL, and VFBL. Refer to Figure 3.

Inductor and Schottky Diode Placement

The inductor and fly-back Schottky diode must be placed close to the source of the power MOSFET. The node connecting the inductor and the diode swing between the drain voltage of the FET and the forward voltage of the Schottky diode. It is recommended that this node be converted to a plane if possible. This node is part of the high current path in the design, and is best treated as a plane to minimize the parasitic resistance and inductance on that node.

Most PC board manufacturers utilize 1/2oz copper on the top and bottom signal layers of the PCB; thus, it is not recommended to use these layers to rout the high current portions of the regulator design. Since it is more common to use 1 oz.

copper on the PCB inner layers, it is recommended to use those layers to route the high current paths in the design.

Capacitor Placement

One of the keys to a successful switch-mode power supply design is correct placement of the low ESR capacitors. Decoupling capacitors serve two purposes; first there must be enough bulk capacitance to support the expected transient current, and second, there must be a variety of values and capacitor types to provide noise supression over a wide range of frequencies. The low ESR capacitors on the input side (5V) of the FET must be located close to the drain of the power FET. Minimizing parasitic inductance and resistance is critical in supressing the ringing and noise spikes on the power supply. The output low ESR capacitors need to be placed close to the output sense resistor to provide good decoupling at the voltage sense point. One of the characteristics of good low ESR capacitors is that the impedance gradually increases as the frequency increases. Thus for high frequency noise supression, good quality low inductance ceramic capacitors need to be placed in parallel with the low ESR bulk capacitors. These can usually be 0.1µF 1206 surface mount capacitors.

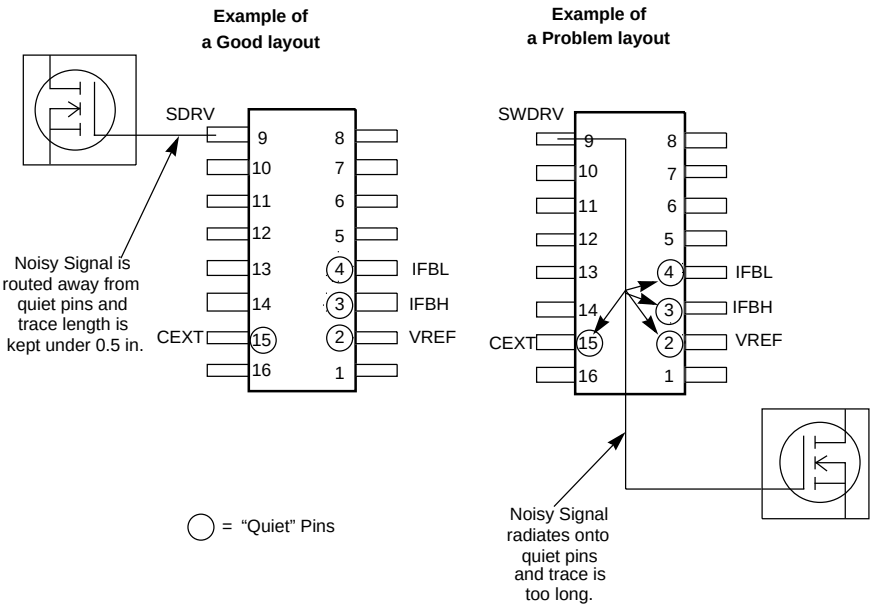


Figure 3. Examples of good and poor layouts

Power and Ground Connections

The connection of VCCA to the 5V power supply plane should be short and bypassed with a 0.1µF directly at the VCCA pin of the FAN5038. The ideal connection would be a via down to the 5V power plane. A similar arrangement should be made for the VCCL pin that connects to +12V, though this one is somewhat less critical since it powers only the linear op-amp. Each ground should have a separate via connection to the ground plane below.

MOSFET Gate Bias

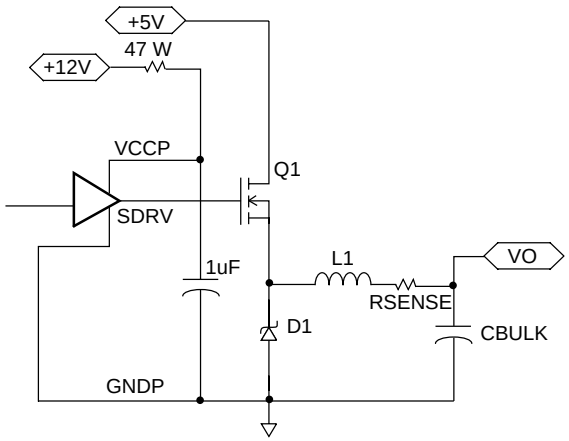


Figure 4. 12V Gate Bias Configuration

A 12V power supply is used to bias the VCCP. A 47Ω resistor is used to limit the transient current into VCCP. A 1uF capacitor filter is used to filter the VCCP supply and source the transient current required to charge the MOSFET gate capacitance. This method provides sufficiently high gate bias voltage to the MOSFET (V_{GS}), and therefore reduces $R_{DS(ON)}$ of the MOSFET and its power loss.

Figure 4 provides about 5V of gate bias which works well when using typical logic-level MOSFETs.

Layout Gerber File and Silk Screen

A reference design for motherboard implementation of the FAN5038 along with the Layout Gerber File and the Silk Screen is available. Please call Fairchild Electronics Semiconductor Division's Marketing Departmentat to obtain this information.

FAN5038 Evaluation Board

Fairchild Electronics Semiconductor Division provides an evaluation board for verifying the system level performance of the FAN5038. The evaluation board provides a guide as to what can be expected in performance with the supplied external components and PCB layout. Please call your local Sales Office or Fairchild Electronics Semiconductor Division for an evaluation board.

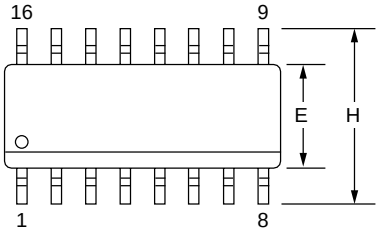
Mechanical Dimensions

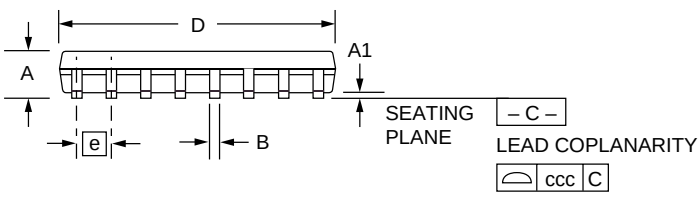
16-Lead SOIC Package

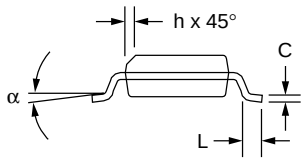
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
B	.013	.020	0.33	0.51	
C	.008	.010	0.19	0.25	5
D	.386	.394	9.80	10.00	2
E	.150	.158	3.81	4.00	2
e	.050 BSC		1.27 BSC		
H	.228	.244	5.80	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	16		16		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Ordering Information

Product Number	Package
FAN5038M	16 pin SOIC