FAN5230

System Electronics Regulator for Mobile PCs

Features

- 5.4V to 24V input voltage range
- Five regulated outputs:
- 5V @ 5A (PWM)
- 3.3V @ 5A (PWM)
- 5V @ 50mA Always On (Linear)
- 3.3V @ 50mA Always On (Linear)
- 12V/Adjustable @ 120mA Boost (PWM)
- >96% efficiency
- Hysteretic mode for light loads
- PWM mode for normal loads
- Main regulators switch out of phase
- 300kHz fixed frequency switching
- RDS(ON) current sense over-current
- Reduced BOM; Max. efficiency
- Optional current sense resistor for precision over-current detect
- Power Good signal for all voltages
- Input under-voltage lock-out (UVLO)
- Thermal shutdown
- ACPI compliant
- 24-pin QSOP
- 2nd source by Intersil (IPM6220)

Applications

- Notebook PCs
- Web tablets
- Battery-powered instruments

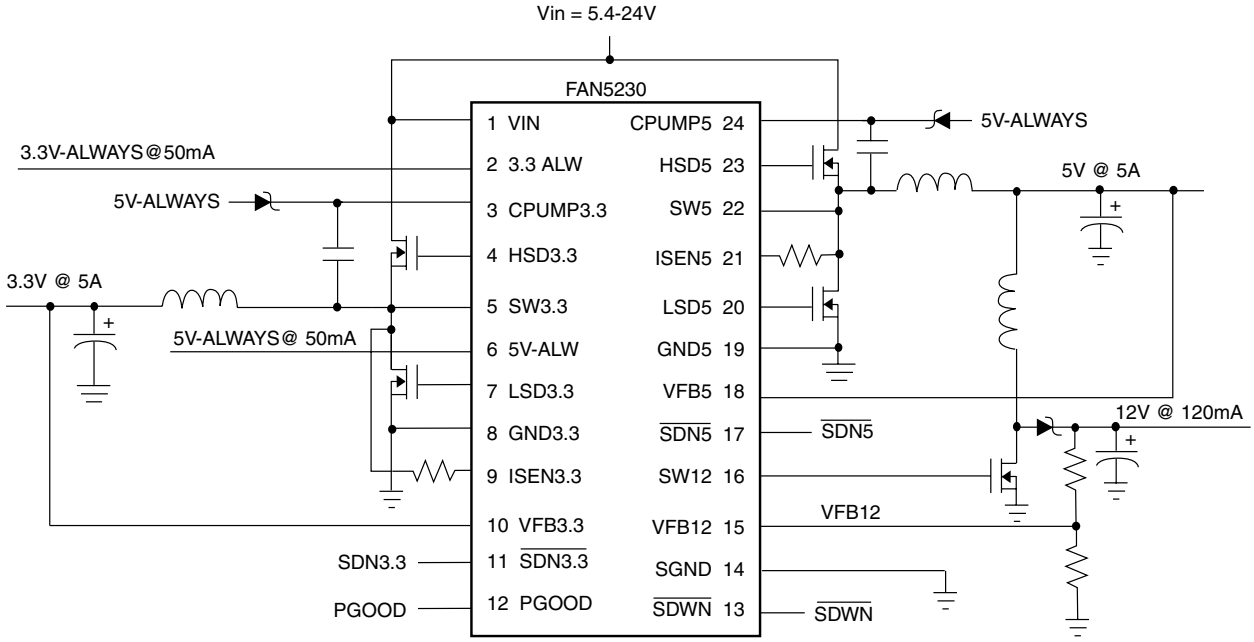
Description

The FAN5230 is a high efficiency and high precision multiple-output voltage regulator for notebook PC and other similar battery-powered applications. It integrates three pulse-width modulated (PWM) switching regulator controllers and two linear regulators to convert 5.4V-to-24V notebook battery power into the voltage used by the circuitry that surrounds the microprocessor in these systems.

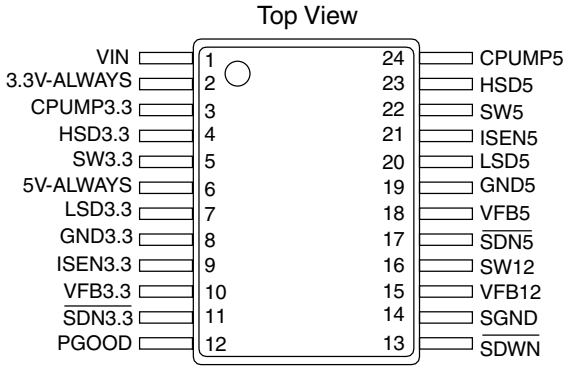
The two primary PWM controllers in the FAN5230 use synchronous-mode rectification to provide 3.3V and 5V at over 5A each. They switch out-of-phase to minimize input ripple-current. Utilization of both input and output voltage feedback in a current-mode control allows for fast and stable loop response over a wide range of input and output variations. PWM control in normal operation and hysteretic control under light load provides efficiency of greater than 95% over a wide range of input and output variations. The third PWM controller generates 12V at 120mA. A proprietary technology is used for accurate [± 1%] sensing of output current using the RDS(ON) of the external MOSFETs, eliminating external current sense resistors which saves board space and reduces BOM cost.

Two integrated linear regulators provide stand-by ALWAYS-ON power at 3.3V and 5V for light (50mA) loads. Additional FAN5230 features include over-voltage, under-voltage, and over-current monitors and thermal shutdow protection.
A single Power-Good signal is issued when soft start is completed and all outputs are within ± 10% of their settings.

Typical Application



Pin Assignments



Pin Description

Pin Name	Pin Number	Pin Function Description
VIN	1	**Input power.**
3.3V-ALWAYS	2	**3.3V Always on linear regulator.** Load current on pins 2 and 6 must not exceed 50mA total. This pin should be decoupled to ground with a 10µF capacitor.
CPUMP3.3	3	**Charge Pump 3.3V.** High side Gate drive voltage for 3.3V. This pin is to be connected to SW3.3 through a 100nF cap. and to 5V-ALWAYS through a diode
HSD3.3	4	**High-side gate driver for 3.3V.** Connect this pin directly to the gate of an N-channel MOSFET. The trace from this pin to the MOSFET gate should be < 1".
SW3.3	5	**High side FET Source and Low Side FET Drain Switching Node.** Switching node for 3.3V.
5V-ALWAYS	6	**5V Always on linear regulator output.** The sum of the load currents on pins 2 and 6 must not exceed 50mA total. This pin should be decoupled to ground with a 10µF capacitor.

Pin Description (Continued)

Pin Name	Pin Number	Pin Function Description
LSD3.3	7	**Low-side gate driver for 3.3V.** Connect this pin directly to the gate of an N-channel MOSFET. The trace from this pin to the MOSFET gate should be < 1".
GND3.3	8	**Ground for 3.3V MOSFET.**
ISEN3.3	9	**Current sense for 3.3V.** This pin should be connected to the Drain of the bottom Mosfet with an appropriate resistor and an RC filter. See Application Section.
VFB3.3	10	**Voltage feedback for 3.3V.**
$\overline{\text{SDN3.3}}$	11	**Soft Start and ON/OFF for 3.3V.** OFF=GND. ON=open with $\overline{\text{SDWN}}$=High. Use open collector device for control.
PGOOD	12	**Power Good Flag.** An open collector output that will be logic low if any output voltage is not above 89% of the nominal output voltage.
$\overline{\text{SDWN}}$	13	**Master Shutdown.** Shutdown for all power. Off when low. When high 5V/3.3V-ALWAYS are ON while 5V/3.3V-Main are ready to turn on if $\overline{\text{SDN5}}$, $\overline{\text{SDN3.3}}$ go open.
SGND	14	**Signal ground.**
VFB12	15	**Voltage feedback for 12V.**
SW12	16	**FET driver for 12V Boost.**
$\overline{\text{SDN5}}$	17	**Enable/Soft Start for 5V and 12V.** Soft start and ON/OFF for 5V & 12V. OFF=Grounded. ON=open with $\overline{\text{SDWN}}$=High.
VFB5	18	**Voltage feedback for 5V.**
GND5	19	**Ground for 5V MOSFET.**
LSD5	20	**Low side FET driver for 5V.** Connect this pin directly to the gate of an N-channel MOSFET. The trace from this pin to the MOSFET gate should be < 1".
ISEN5	21	**Current Sense for 5V.** This pin should be connected to the drain of the bottom Mosfet using appropriate resistor and RC filter. See Application Section.
SW5	22	**High Side Driver Source and Low Side Driver Drain Switching Node.** Switching node for 5V.
HSD5	23	**High side FET driver for 5V.** Connect this pin directly to the gate of an N-channel MOSFET. The trace from this pin to the MOSFET gate should be < 1".
CPUMP5	24	**Charge Pump 5V.** High side Gate drive voltage for 5V. High side Gate drive voltage for 5V. This pin is to be connected to SW5 through a 100nF cap. and to 5V-ALWAYS through a diode.

Absolute Maximum Ratings[1]

Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IN}		-0.3		27	V
SW, ISEN Pins,SDWN Pin		-0.3		27	V
CPUMP, HSD Pins		-0.3		33	V
SDN, VFB, V_always pins		-0.3		6.5	V
CPUMP to SW pins, and all other pins		-0.3		6.5	V
The sum of the load currents on pins 2 and 6 must not exceed 60mA total					

Note:

1. Stresses beyond "Absolute Maximum Ratings" may cause permanent device damage. Continuous exposure to absolute maximum rating conditions may affect device reliability. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied.

Recommended Operating Conditions

Input Voltage, V_{IN}	+5.4V to 24V
Ambient Temperature, T_A	-20°C to 85°C

Thermal Information

Thermal Resistance, RTH_{JA}	88°C/W
Thermal Resistance, RTH_{JC}	28.5°C/W
Maximum Junction Temperature	150°C
Storage Temperature Range	-65°C to 150°C
Maximum Lead Temperature, Soldering 10 Sec	300°C

ELECTRICAL SPECIFICATIONS

Operating Conditions

Recommended Operating Conditions Unless Noted Refers to Block Diagrams

Parameter	Conditions	Min.	Typ.	Max.	Units
Supply					
V_{IN} Input Supply Voltage	(DC loading only) Note 1	5.4		24	V
Input Quiescent Current	H/LSD Open		1.4	3	mA
	Stand-by		300	400	µA
	Shut-down		<1	5	µA
Input UVLO Threshold	Rising Vbat	4.3	4.7	5.1	V
	hysteresis		100		mV
5V and 3.3V Main Regulators					
Output Voltage Precision	0.1 to 5.5A, 5.4 to 24V	-2		+2	%
Oscillator Frequency, f_{osc}		255	300	345	kHz
HSD On-Resistance, pull up			7	12	Ω
HSD On Resistance pull down			4	10	Ω
LSD On-Resistance, pull up			6	9	Ω
LSD On Resistance pull down			5	8	Ω

Operating Conditions (Continued)

Recommended Operating Conditions Unless Noted Refers to Block Diagrams

Parameter	Conditions	Min.	Typ.	Max.	Units
HSD On Output, V_{CPUMP}-V_{GS}	I = 10µA			100	mV
HSD Off Output, V_{GS}	I = 10µA			100	mV
LSD On Output, $V_{5V\text{-}Always}$-V_{GS}	I = 10µA			100	mV
LSD Off Output, V_{GS}	I = 10µA			100	mV
Ramp Amplitude, pk-pk	VIN = 16V		2		V
Ramp Offset			0.5		V
Ramp Gain from V_{IN}			125		mV/V
Error Amplifier GBW			3		MHz
Current Limit Threshold	R2, R8 = 1KΩ	90	135	180	µA
Over Voltage Threshold	2µs delay	110	115	120	%VO
Under Voltage Threshold	2µs delay	70	75	80	%VO
SDN/SS Full On Voltage Min.	(End of Soft Start)	4.2			V
SDN/SS Full Off Voltage Max.				800	mV
Max Duty Cycle			94		%
Min PWM Time			200		nsec
VFB3.3 Input Leakage Current		40	55	70	µA
12V Regulator					
Output Voltage Precision	V_5 =4.9 to 5.1V and Io=0 to 150mA	-2		+2	%
V_{FB12}			2.472		V
V_{FB12} Input Current	Note 2		100	200	nA
Oscillator Frequency (f_{osc}/3)		85	100	115	kHz
Gate Drive On-Resistance	High or Low		6	12	Ω
12V Regulator (Continued)					
On Output, $V_{5V\text{-}Always}$-V_{GS}	I = 10µA			100	mV
Off Output, V_{GS}	I = 10µA			100	mV
Ramp Amplitude, pk-pk			2		V
Error Amplifier GBW			1		MHz
Under Voltage Shut Down	2µs delay	70	76	80	%V_O
Over Voltage Shut Down	Measured at VFB_{12}		115		%V_O
Min Duty Cycle		0			%
Max Duty Cycle	(By design)	32	33	34	%
5V and 3.3V Always					
Bypass Switch rdson			1.3	1.5	Ω
Linear Regulator Accuracy	5.6 to 24V, 0 to 50mA, 5V Main On or Off	-3.3		2	%
Rated Output Current	$I_{3.3} + I_5$	0		50	mA
Over-current Limit	2µs delay	100	180		mA
Under-voltage Threshold	2µs delay	70	75	80	%
Reference					
Internal Reference Accuracy	0-70°C	-1		1	%

Operating Conditions (Continued)

Recommended Operating Conditions Unless Noted Refers to Block Diagrams

Parameter	Conditions	Min.	Typ.	Max.	Units
Control Functions					
SDWN Off Voltage Max.				800	mV
SDWN On Voltage Min.		3			V
Over-temperature Shutdown, t_j			150		°C
Over-temperature Hysteresis			25		°C
PGOOD Threshold	PWM Buck Converters	-14	-11	-8.5	$\%V_O$[1]
PGOOD Sink Current		-4			mA
PGOOD leakage				1	µA
+5V Analog Softstart	Css=100nF		65		msec
+3.3V Analog Softstart	Css=100nF		65		msec
Soft Start Current			5		µA
PGOOD Min Pulse Width	Note 2	5	10		µs

Notes

1. The minimum input voltage does not include voltage drop in the source supply due to source resistance. It is operating voltage for static load conditions. To get acceptable load transient performance, the input voltage required will be much higher, in the 7.5 to 8.5 volt range or even higher depending on the severity of dynamic load, source impedance and input and output capacitance and inductor values. The user should thoroughly test the performance at minimum input voltage using intended component values and transient loading.
2. Min/Max specifications are guaranteed by design.

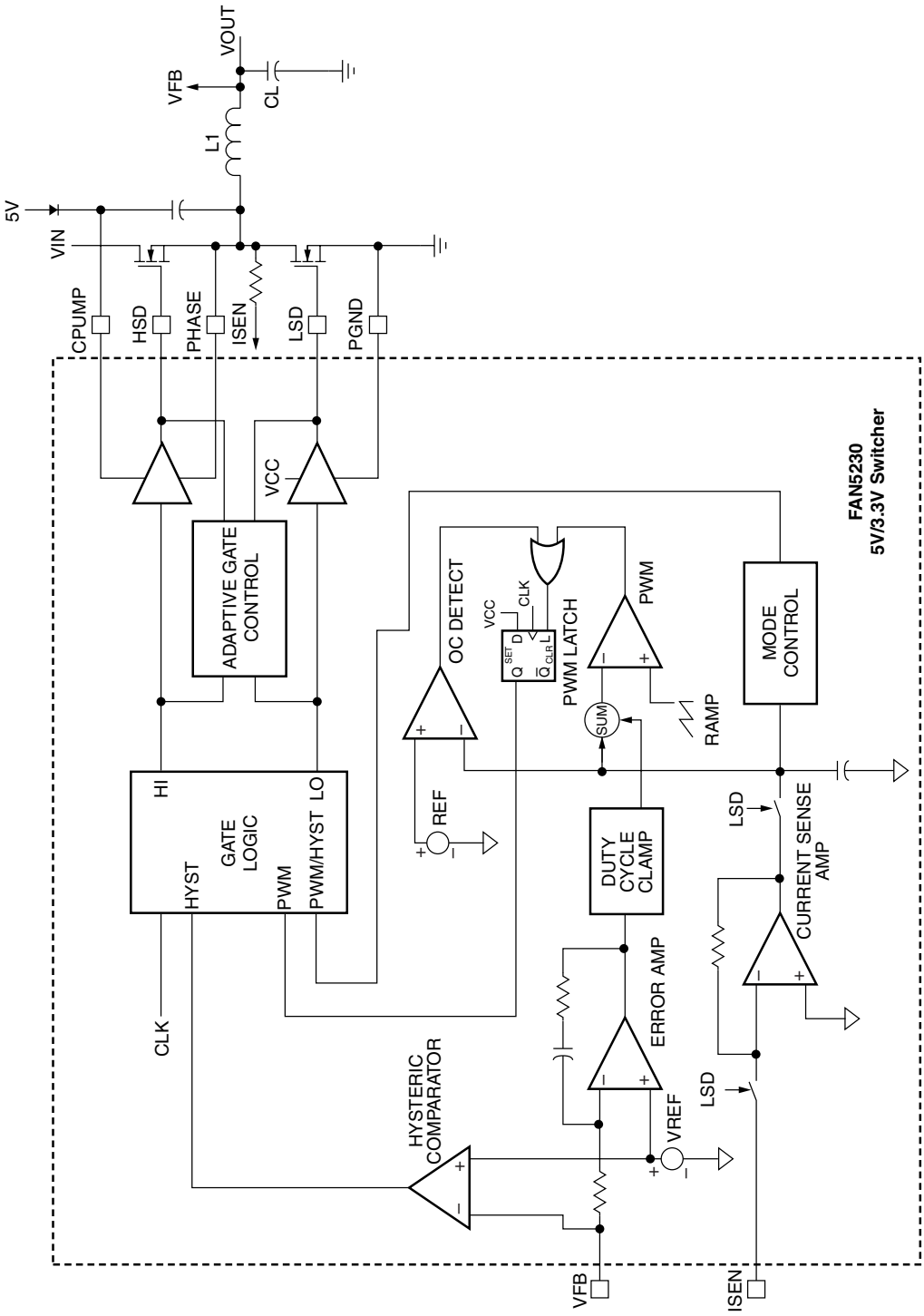


Figure 1. FAN5230 5V/3.3V Internal Block Diagram of PWM/PFM Loops.

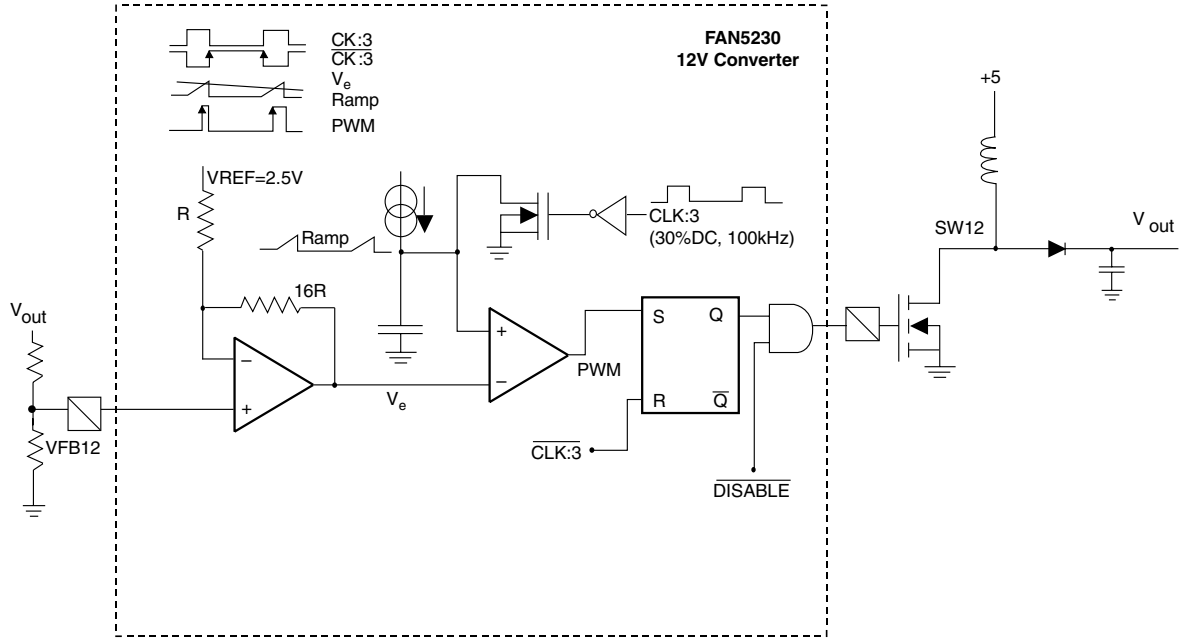


Figure 2. FAN5230 12V Internal Block Diagram

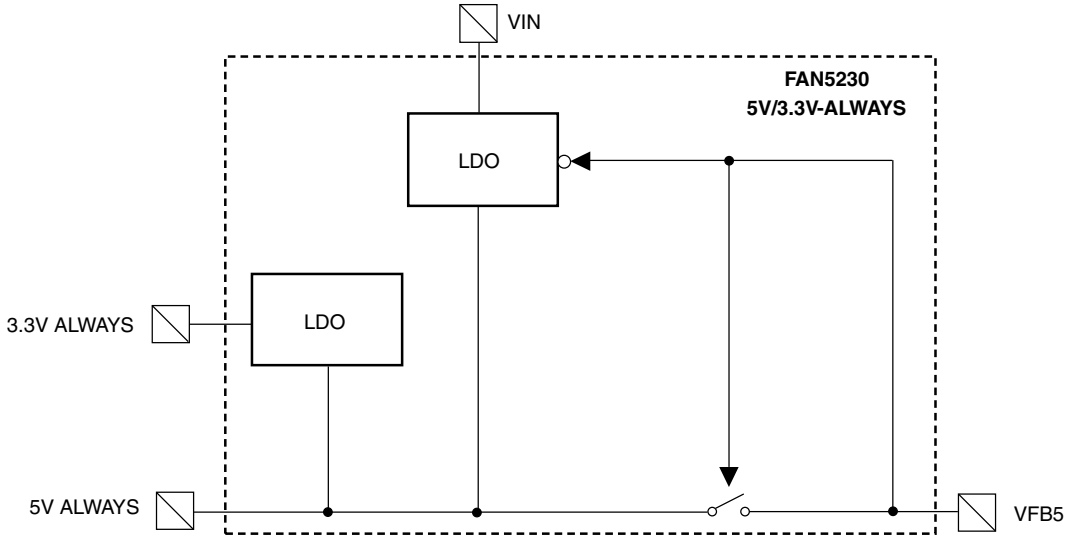


Figure 3. FAN5230 5V/3.3V—ALWAYS Internal Block Diagram

Functional Description

The FAN5230 is a high efficiency and high precision DC/DC controller for notebook and other portable applications. It provides all of the voltages necessary for system electronics: 5V, 3.3V, 12V, and both 3.3V-ALWAYS and 5V-ALWAYS. Utilization of both input and output voltage feedback in a current-mode control allows for fast loop response over a wide range of input and output variations. Current sense based on MOSFET $R_{DS,on}$ gives maximum efficiency, while also permitting the use of a sense resistor for high accuracy.

3.3V and 5V Architecture

The 3.3V and 5V switching regulator outputs of the FAN5230 are generated from the unregulated input voltage using synchronous buck converters. Both high side and low-side MOSFETs are N-channel.

The 3.3V and 5V switchers have pins for current sensing and for setting of output over-current threshold using MOSFET $R_{DS,on}$. Each converter has a pin for voltage-sense feedback, a pin that shuts down the converter, and a pin for generating the boost voltage to drive the high-side MOSFET.

If the 5V switcher is not used, connect SDN5 (pin 17) to SGND (pin 14). If the 3.3V switcher is not used, connect SDN3.3 (pin 11) to SGND (pin 14).

The following discussion of the FAN5230 design will be done with reference to Figures 1 through 4, showing the internal block diagram of the IC.

3.3V and 5V PWM Current Sensing

Peak current sensing is done on the low side driver because of the very low duty-cycle on the high side MOSFET. The current is sampled 50ns after turn on and the value is held for current feedback and over-current limit.

3.3V and 5V PWM Loop Compensation

The 3.3V and 5V control loops of the FAN5230 function as voltage mode with current feedback for stability. They each have an independent voltage feedback pin, as shown in Figure 1. They use voltage feed-forward to guarantee loop rejection of input voltage variation: that is to say that the PWM (pulse width modulation) ramp amplitude is varied as a function of the input voltage. Compensation of the control loops is done entirely internally using current-mode feedback compensation. This scheme allows the bandwidth and phase margin to be almost independent of output capacitance and ESR.

3.3V and 5V PWM Current Limit

The 3.3V and 5V converters each sense the voltage across their own low-side MOSFET to determine whether to enter current limit. If an output current in excess of the current limit threshold is measured then the converter enters a pulse skipping mode where Iout is equal to the over-current (OC) set limit. After 8 clock cycles then the regulator is latched off (HSD and LSD off). This is the likely scenario in the case of a "soft" short. If the short is "hard" it will instantly trigger the under-voltage protection which again will latch the regulator off (HSD and LSD off) after a 2μs delay.

Selection of a current-limit set resistor must include the tolerance of the current-limit trip point, the MOSFET on resistance and temperature coefficient, and the ripple current, in addition to the maximum output current.

Example: Maximum DC output current on the 5V is 5A, the MOSFET $R_{DS,on}$ is 17mΩ, and the inductor is 5μH at a current of 5A. Because of the low $R_{DS,on}$, the low-side MOSFET will have a maximum temperature (ambient + self-heating) of only 75°C, at which its $R_{DS,on}$ increases to 20mΩ.

Peak current is DC output current plus peak ripple current:

$$I_{pk} \approx I_{dc} + \frac{TV_0}{2L} = 5A + \frac{4\mu sec \bullet 5V}{2 \bullet 5\mu H} = 7A$$

where T is the maximum period, V_O is output voltage, and L is the inductance. This current generates a voltage on the low-side MOSFET of 7A • 20mΩ = 140mV. The current limit threshold is typically 150mV (worst-case 135mV) with R2 = 1KΩ, and so this value is suitable. R2 could be increased a further 10% if additional noise margin is deemed necessary.

Precision Current Limit

Precision current limiting can be achieved by placing a discrete sense resistor between the source of the low-side MOSFET and ground.

In this case, current limit accuracy is set by the tolerance of the IC, +10%.

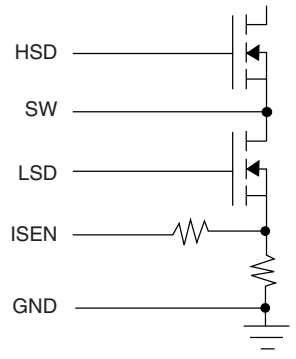


Figure 4. Using a Precision Current Sense Resistor

Shutdown ($\overline{SDWN}$)

The $\overline{SDWN}$ pin turns off all 5 converters (+5V, +3.3V, and +12V, 5V/3.3V-ALWAYS) and puts the FAN5230 into a low-power mode (Shutdown mode).

This mode of operation implies the use of a push button switch between $\overline{SDWN}$ and Vin. Pushing the button allows (for the duration of the contact) to power the 3.3V-ALWAYS and 5V-ALWAYS long enough for the uC to power up and in turn latch the $\overline{SDWN}$ pin high.

Once the $\overline{SDWN}$ is high then the ALWAYS voltages are enabled to go high if the respective $\overline{SDN3.3}$ and $\overline{SDN5}$ go high.

MAIN 3.3V and 5V Softstart, Sequencing and Stand-by

Softstart of the 3.3V and 5V converters is accomplished by means of an external capacitor between pins $\overline{SDN3.3}$ ($\overline{SDN5}$) and ground.

The 3.3V (5V) main converter is turned ON if $\overline{SDWN}$ and $\overline{SDN3.3}$ ($\overline{SDN5}$) are both high and is turned off if either $\overline{SDWN}$ or $\overline{SDN3.3}$ ($\overline{SDN5}$) is low.

Stand-by mode is defined as the condition by which V-Mains are OFF and V-ALWAYS are ON ($\overline{SDWN}$=1 and $\overline{SDN3.3}$=$\overline{SDN5}$=0).

ALWAYS mode of Operation

If it is desired that 5V-ALWAYS and 3.3V-ALWAYS are always ON then the $\overline{SDWN}$ pin must be connected to Vin permanently. This way the two ALWAYS regulators come up as soon as there is power while the state of the Main regulators can be controlled via the $\overline{SDN5}$ and $\overline{SDN3.3}$ pins.

Sequencing Table

$\overline{SDN5}$	$\overline{SDN3.3}$	$\overline{SDWN}$	3V&5V ALWAYS	5V MAIN	3.3V MAIN
X	X	0	0	0	0
0	0	1	1	0	0
1	0	1	1	1	0
0	1	1	1	0	1
1	1	1	1	1	1

3.3V and 5V Light Load Mode

The 3.3V and 5V converters are synchronous bucks, and can operate in two quadrants, this means that the ripple current is constant and independent of the load current. At light loads, this ripple current translates into poor efficiency, since it causes circulating current losses in the MOSFETs. To optimize the efficiency at light loads, then, the FAN5230 switches from normal operation to a special light load mode after an 8 clock pulse delay. This prevents false triggering when the voltage across the on-state low-side MOSFET goes positive. Vice-versa when this voltage becomes negative the FAN5230 switches back to PWM operation. The current threshold for switch to and from light load is therefore:

$$Ith = Iripplepeak$$

In light load mode, the FAN5230 switches from PWM (pulse width modulation) to PFM (pulse frequency modulation), which reduces the gate drive current.

As the load current becomes very light, the FAN5230 begins pulse skipping, but remains synchronized with the clock. See next section for low side drive management.

Low Side Driver Forcing in Light Load

During light load operation, the Low Side Driver (LSD) is traditionally turned permanently OFF to avoid current inversion in the inductor and associated efficiency losses. At the same time the low side driver also needs to be turned ON in order to a) measure current (current is sensed on the low side driver) and b) assure proper operation of the charge pump, especially under low current and low input voltage conditions. In order to accomplish all the above, when the circuit enters hysteretic operation the LSD is kept "ON" to re-circulate positive and decaying currents (corresponding to negative drops across low side driver Rdson) and turned off as soon as current crosses zero (corresponding to drop across Rdson becoming positive). This way the low side driver is utilized in "partial duty" or as "active zero drop diode" (compared to classic light load operation in which the LSD is turned permanently OFF) allowing more functionality without loss in efficiency.

3.3V Voltage Adjustment

The output voltage of the 3.3V converter can be increased by as much as 10% by inserting a resistor divider in the feedback line. The feedback pin impedance is about 66KΩ. Thus, for example, to increase the output of the 3.3V converter by 10%, use a 2.21KΩ/33.2KΩ divider.

Note that the output of the 5V regulator cannot be adjusted. The feedback line of the 5V regulator is used internally as a 5V supply and, therefore, cannot tolerate any impedance in series with it.

3.3V and 5V Main Overvoltage Protection (Soft Crowbar)

When the output voltage of the 3.3V (or the 5V) converter exceeds approximately 115% of nominal, the converter enters the over-voltage (OV) protection mode, with the goal of protecting the load from damage. During operation, severe load dump or a short of an upper MOSFET could cause the output voltage to increase significantly over normal operation range without circuit protection. When the output exceeds the over-voltage threshold, the over-voltage comparator forces the lower gate driver high and turns the lower MOSFET on. This will pull down the output voltage and eventually may blow the battery fuse. As soon as output voltage drops below the threshold, OVP comparator is disengaged.

The OVP scheme also provides a soft crowbar function (bang-bang control followed by blow of the fuse) which helps to tackle severe load transients but does not invert output voltage when activated—a common problem for OVP schemes with a latch. The prevention of output inversion eliminates the need for a Schottky diode across the load.

3.3V and 5V Under-voltage Protection

When the output voltage of either the 3.3V or 5V falls below 75% of the nominal value, both converters, go into under-voltage (UV) protection, after a 2μsec delay. In under-voltage protection, the high and low side MOSFETs are turned off. Once under-voltage protection is triggered, it remains on until power is recycled or the $\overline{\text{SDWN}}$ pin is reset.

12V Architecture

The 12V converter is a traditional non-isolated fly-back (also known as a "boost" converter). The converter's input voltage is the +5V switcher output, so that +12V can only be present if +5V is present. Also, if the external MOSFET is off, the output of the +12V converter is +5V, not zero. This in turn will provide non-zero output for the 12V regulator.

For complete turn-off of the 12V regulator an external P-channel MOSFET or an LDO regulator with on/off control may be used. If an LDO is used for 12V then the boost converter should be set to 13.2V using the external resistor divider network. If the 12V "boost" converter is not used, connect VFB12 (pin 15) to 5V-ALWAYS (pin 6).

12V Loop Compensation

The 12V converter should be run in discontinuous conduction mode. In this mode, the converter will be stable if a capacitor with suitable ESR value is selected. A 68uF tantalum with 500mA ripple current rating and 95mΩ is recommended here.

12V Protection

The 12V converter is protected against overvoltage. If the 12V feedback is more than 10–15% above the nominal set voltage, a comparator forces the MOSFET off until the voltage falls below the comparator threshold.

The 12V converter is also protected against over-current. If a short circuit pulls the output below 9V, all of the switching converters go into UV protection, after a 2μs delay. In UV protection, all MOSFETs are turned off. Once UV protection is triggered, it remains on until the input power is recycled or the $\overline{\text{SDWN}}$ is reset.

12V Softstart and Sequencing

The 12V output is started at the same time as the 5V output. The softly rising 5V output automatically generates a softly rising 12V output. The duty cycle of the 12V PWM is limited to prevent excessive current draw.

The 12V supply must build up a voltage higher than the UVLO limit (9V) by the time the 5V is above its UVLO (3.75V) in order to avoid triggering of UV protection during soft start.

5V/3.3V-ALWAYS Operation

The 5V-ALWAYS supply is generated from either the on-chip linear regulator or through an internal switch from the VFB pin of the 5V switching supply. The 5V-ALWAYS supply should be decoupled to ground with a 10μF capacitor.

When the 5V switching supply is off, or if its output voltage is not within tolerance, the 5V-ALWAYS switch is open, and the linear regulator is on. When the 5V switching supply is running and has an output voltage within specification, the linear regulator is off, and the switch is on. The switch has sufficiently low resistance that at maximum current draw on the 5V-ALWAYS supply, the output voltage is regulated within specifications.

The 3.3V-ALWAYS is generated from a linear regulator attached internally to the 5V-ALWAYS. The 3.3V-ALWAYS supply should be decoupled to ground with a 10μF capacitor.

The purpose of the two ALWAYS supplies (combined current is specified to never exceed 50mA) is to provide power to the system micro-controller (8051 class) as well as other IC's needing a stand-by power. The micro-controller as well as the other IC's could be operated from either 5V or 3.3V ALWAYS, so the FAN5230 provides both.

5V/3.3V-ALWAYS Protections

The two internal linear regulators are current limited and under-voltage protected. Once protection is triggered all outputs are turned off until power is cycled or the $\overline{\text{SDWN}}$ is reset.

Power good

Power good is asserted when both PWM Buck converters are above specified threshold. No other regulators are monitored by Power good. When PGOOD goes low it will stay low for at least 10μsec (Tw). See fig. 5.

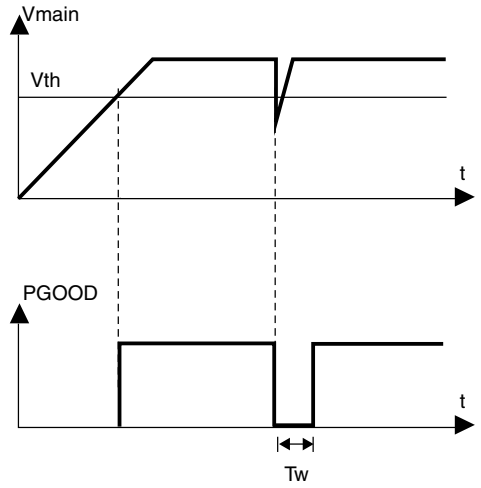


Figure 5. PGOOD Timing Diagram

Error Amplifier output voltage clamp

During a load transient the error amplifier voltage is allowed full swing. After two clock cycles, if the amplifier is still out of range the voltage and consequently the duty cycle (DC) is clamped. The DC clamp automatically limits the build up of over-currents during abnormal conditions, including short circuits:

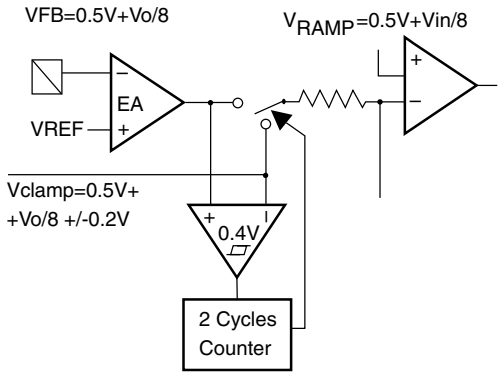


Figure 6. Duty-Cycle Clamp

Thermal shutdown

If the die temperature of the FAN5230 exceeds safe limits, the IC shuts itself off. When the over-temperature (OT) event ends, the IC comes back to normal operation. There is a 25°C thermal hysteresis between shutdown and start up.

Input UVLO

If the input voltage falls below the UVLO threshold, the FAN5230 turns itself off and stays off as long as Input voltage is below threshold.

IC Protections Table

	HSD Buck	LSD Buck	LDO	LSD Boost
OC/UV (Bucks)	OFF-LATCH	OFF-LATCH	ON	OFF-LATCH
OC/UV (LDO)	"	"	OFF-LATCH	"
OV (Buck)*	OFF	SOFT CROWBAR	ON	ON
OV (Boost)	ON	ON	ON	OFF
$\overline{SDWN}$=0	OFF	OFF	OFF	OFF
OT	OFF	OFF	OFF	OFF
UV (Boost)	OFF-LATCH	OFF-LATCH	ON	OFF-LATCH
OC (Boost)	ON	ON	ON	33% DC

* Only the converter in Over-Voltage goes in SOFT CROWBAR mode.

Generic Mobile System Block Diagram

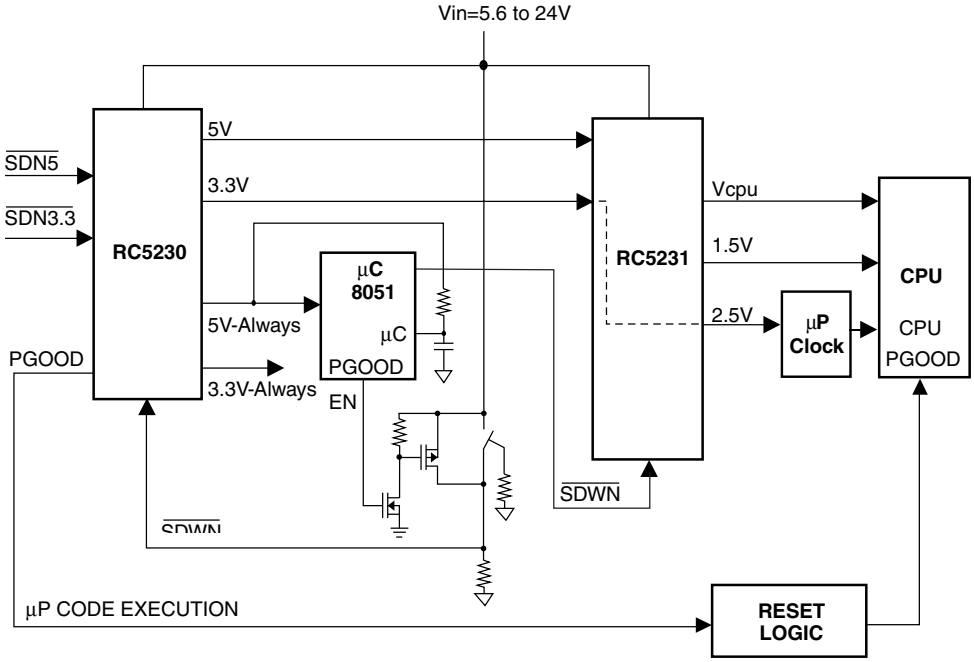


Figure 7. System Block Diagram

Notebook Application Circuit

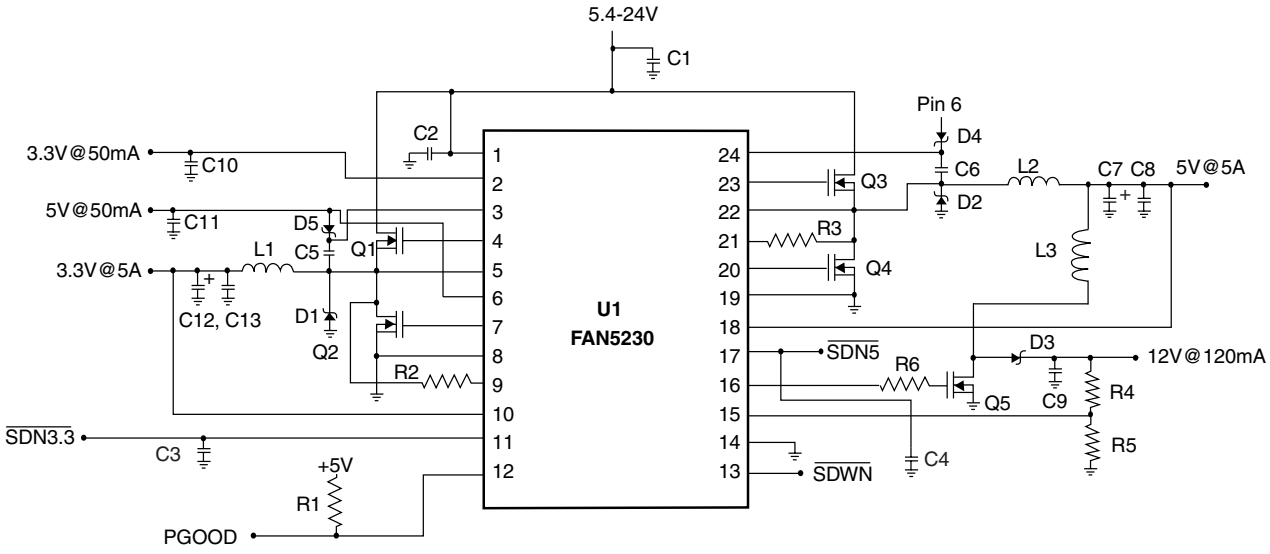


Figure 8. FAN5230 Notebook Application Circuit

Table 1. FAN5230 Application Bill of Materials

Reference	Manufacturer, Part #	Quantity	Description	Comments
C1	SANYO 25SP33M	1	33µF, 25V	OSCON, I_{rms} = 3A, 19V adapter.
C2-6	Any	5	100nF, 50V	Ceramic
C7-8 C12-13	KEMET T510X337(1)010AS	2 2	330µF, 10V	Tantalum, ESR=35mΩ
C10-11	AVXTPSA106010#1800	2	10µF, 10V	Tantalum, ESR=1.8Ω
C9	AVX TPSV68*025R0095	1	68µF, 25V, ESR=95mΩ	Tantalum, I_{rms} = 0.5A
R1	Any	1	10KΩ, 1%	
R2, R3	Any	2	1KΩ, 1%	
R4, R5	Any	1	380KΩ, 100KΩ	1%
R6	Any	1	10Ω	
D1-3	Fairchild SS22	3	2A, 40V Schottky	
D4-5	Fairchild MBR0520L	2	500mA, 20V Schottky	
L1-2	Any	2	6.4µH, 5A	R < 25mΩ
L3	Any	1	5.6µH, 2A	
Q1-4	Fairchild FDS6690A	4	30V N-channel MOSFET	R = 17mΩ
Q5	Fairchild NDC631N	1	20V N-channel MOSFET	R = 60mΩ
U1	Fairchild FAN5230	1	SER Controller	

MOSFET Selection

The notebook application circuit shown in Figure 1 is designed to run with an input voltage operating range of 5.4-24V. This wide input range helps determine the selection of the MOSFETs for the 3.3V and 5V converters, since the high-side MOSFET is on (V_{out} / V_{in}) of the time, and the low-side MOSFET 1 – (V_{out} / V_{in}) of the time. The maxima and minima are tabulated in Table 2:

Table 2. MOSFET Duty Cycles

High-side FET

	V_{in}	
V_{out}	5.4V	24V
3.3V	.61	.14
5V	.43	.21

Low-side FET

	V_{in}	
V_{out}	5.4V	24V
3.3V	.34	.86
5V	.07	.79

All four MOSFETs have maximum duty cycles greater than 50%. Thus, it is necessary to size all four approximately the same.

3.3V and 5V Schottky Selection

The maximum current at which the converters operate in PFM mode determines selection of a Schottky. In the application shown in Figure 8, since the transition can occur at a current as high as 28mV * (17.5KΩ / 10KΩ) / 35mΩ = 1.4A, the diode (with 24V input) will be conducting 86% of the period (from Table 2). It thus has an average current of 1.4A * 0.86 = 1.2A, which requires a Schottky current rating >1A.

3.3V and 5V Inductor Selection

See Table 1.

3.3V and 5V Output Cap Selection

See Table 1.

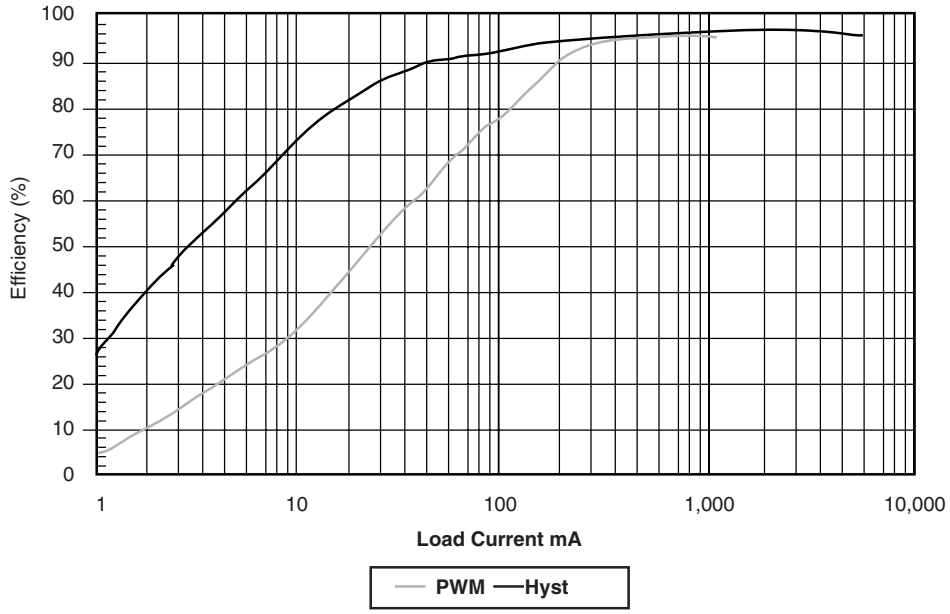
12V Component Selection

Calculation of the inductor, diode and output capacitor for the +12V output fly-back is complex, depending on output power and efficiency. See Applications Bulletin AB-19 for an Excel spreadsheet calculation tool. See Table 1 also.

Input Capacitor Selection

Input capacitor selection is determined by ripple current rating. With two converters operating in parallel at differing duty cycles, calculation of input ripple current is complex; see Applications Bulletin AB-19 for an Excel spreadsheet calculation tool.

Efficiency



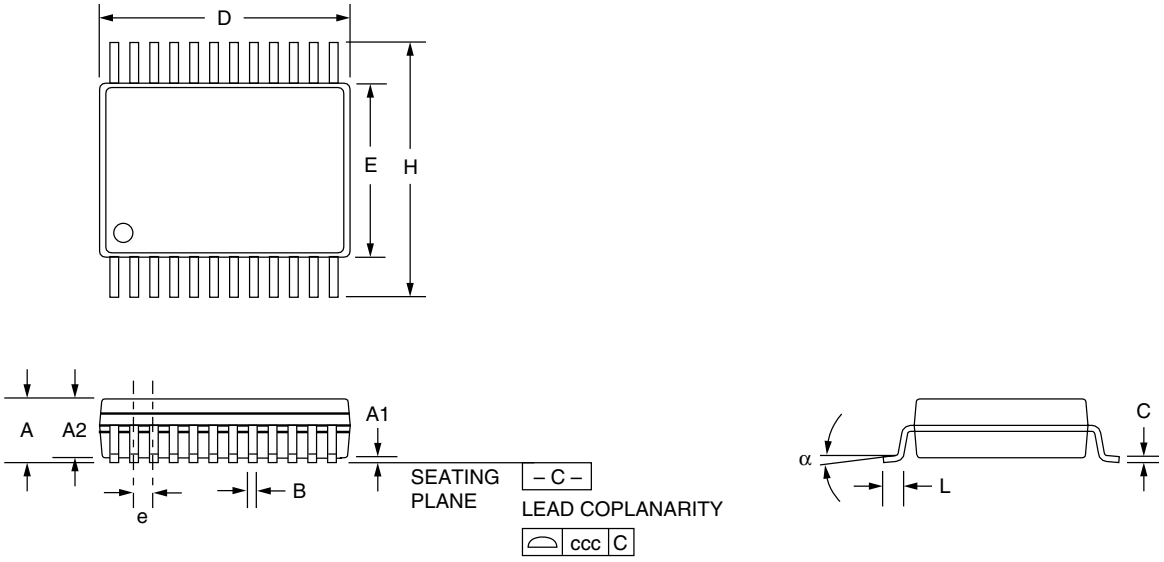
Mechanical Dimensions

QSOP 24-Lead

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	0.0532	0.0668	1.35	1.75	
A1	0.0040	0.0098	0.1	0.25	
A2	0.054	0.062	1.37	1.57	
b	0.008	0.012	0.20	0.30	5
c	0.0075	0.0098	0.19	0.25	5
D	0.337	0.344	8.55	8.74	2, 4
E	0.150	0.157	3.81	3.99	2
e	0.025 BSC		0.635 BSC		
H	0.228	0.244	5.79	6.20	
L	0.016	0.050	0.40	1.27	3
N	24		24		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .006 inch (0.15mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "b" and "c" dimensions include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.



Ordering Information

Product Number	Package
FAN5230QSC	24 Lead QSOP

10/17/01 0.0m 002
Stock#DS30005230