FAN8403D3

3-Phase BLDC Motor Driver with PLL

Features

- 3-Phase BLDC motor drive IC with speed control
- Phase Locked Loop (PLL) speed control
- Built-in phase locked detector output
- External clock for control of motor speed
- Built-in FG amplifier and FG schmidt comparator
- Built-in integrating amplifier with phase error
- Auto Gain Control (AGC) circuit for compensation hall amplifier
- Built-in protection circuits (over-current limit, under-voltage limit, thermal shut down)

Description

The FAN8403D3 is a monolithic integrated circuit. It is suitable for polygon mirror motor of laser beam printer (LBP).

28-SSOPH-375SG2

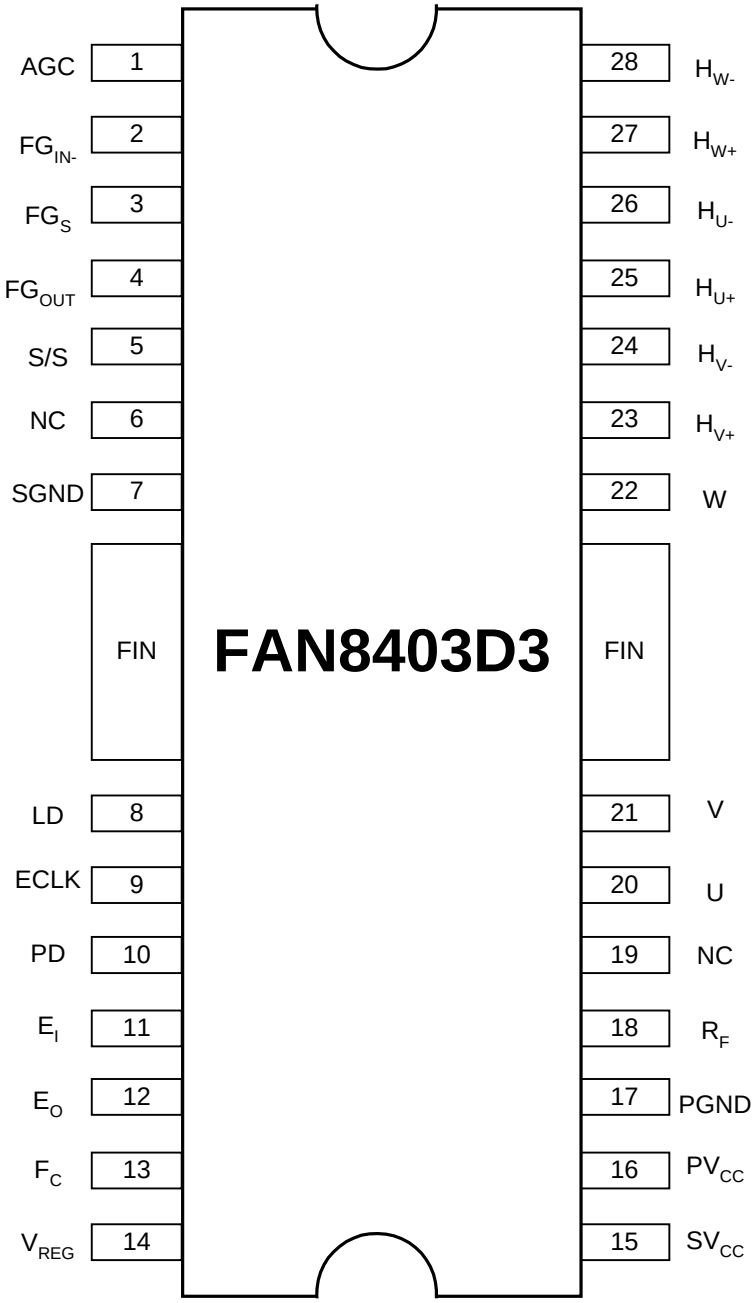
Typical application

- Polygon mirror motor for laser beam printer
- Polygon mirror motor for facsimile
- Polygon mirror motor for duplicator
- Polygon mirror motor for multi-function printer
- General 3 phase BLDC motor

Ordering Information

Device	Package	Operating Temp.
FAN8403D3	28-SSOPH-375SG2	–20°C ~ +80°C
FAN8403D3TF	28-SSOPH-375SG2	–20°C ~ +80°C

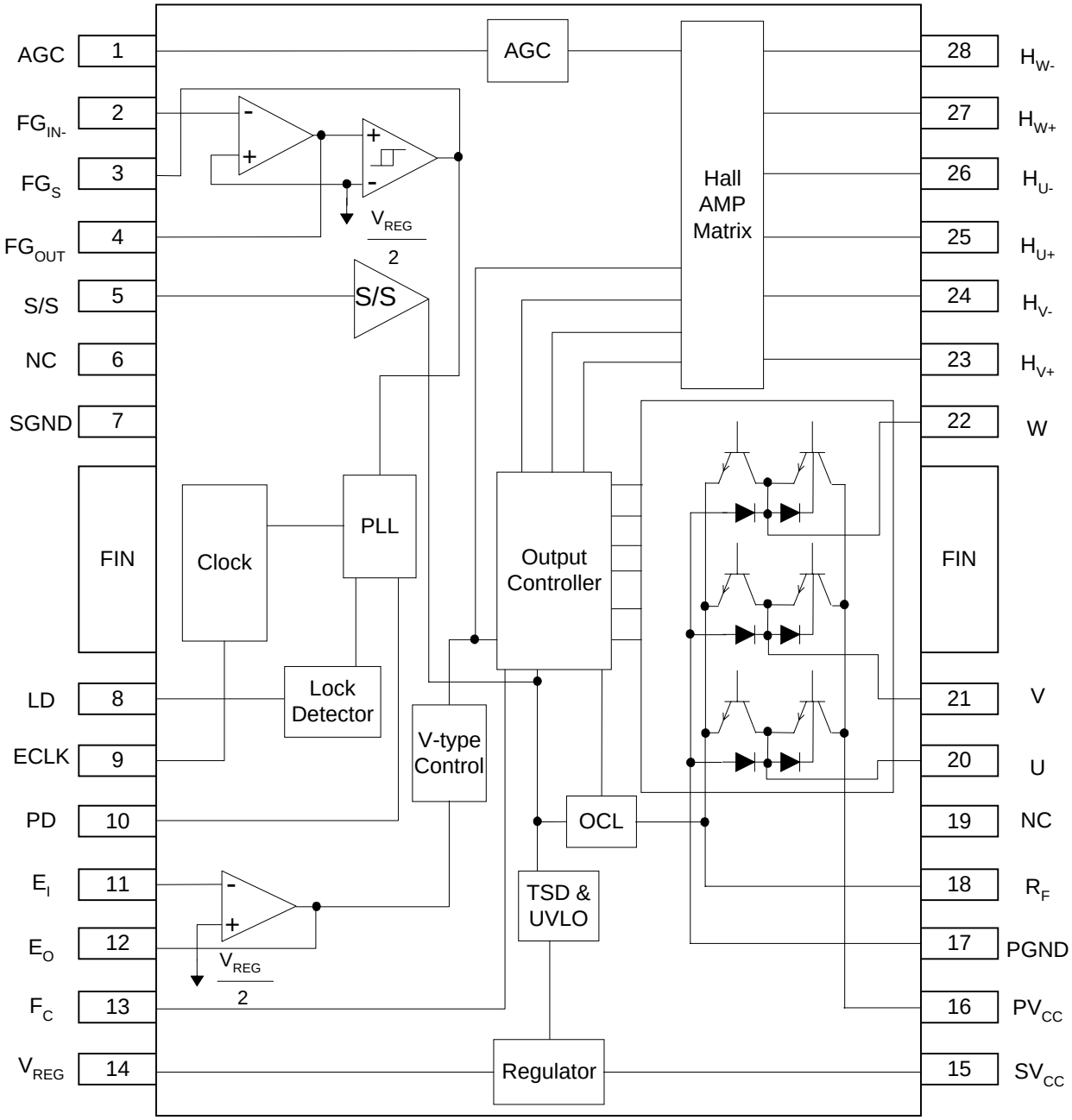
Pin Assignments



Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	AGC	AGC Amplifier Frequency Characteristics Correction
2	FG_{IN-}	FG Amplifier Inverting Input
3	FG_S	FG Pulse Output
4	FG_{OUT}	FG Amplifier Output (Open collect)
5	S/S	Stop And Start
6	NC	-
7	SGND	Signal Ground
8	LD	Phase Locked Loop Detector Output (Open Collect)
9	ECLK	External Clock
10	PD	Phase Locked Loop Detector Output
11	EI	Error Amplifier Inverting Input
12	EO	Error Amplifier Output
13	FC	Control Amplifier Frequency Correction
14	V_{REG}	Regulator Voltage Stabilization Output
15	SV_{CC}	Signal V_{CC}
16	PV_{CC}	Power V_{CC}
17	PGND	Power Ground
18	RF	Output Current Detection
19	NC	-
20	U	U Output
21	V	V Output
22	W	W Output
23	HV+	V Hall Amplifier Non Inverting Input
24	HV-	V Hall Amplifier Inverting Input
25	HU+	U Hall Amplifier Non Inverting Input
26	HU-	U Hall Amplifier Inverting Input
27	HW+	W Hall Amplifier Non Inverting Input
28	HW-	W Hall Amplifier Inverting Input

Internal Block Diagram

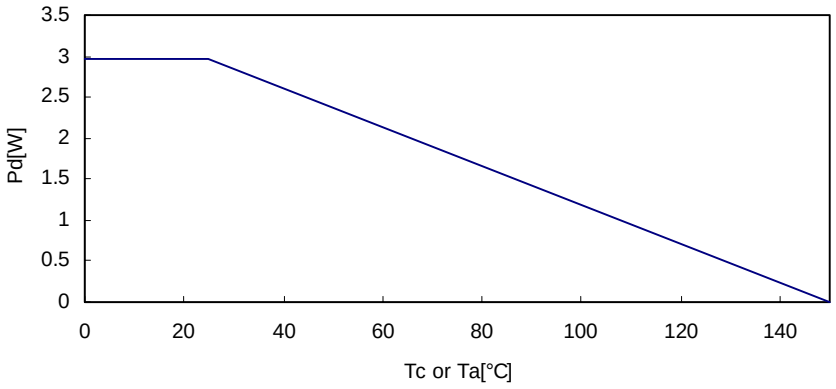


Absolute Maximum Ratings (Ta = 25°C)

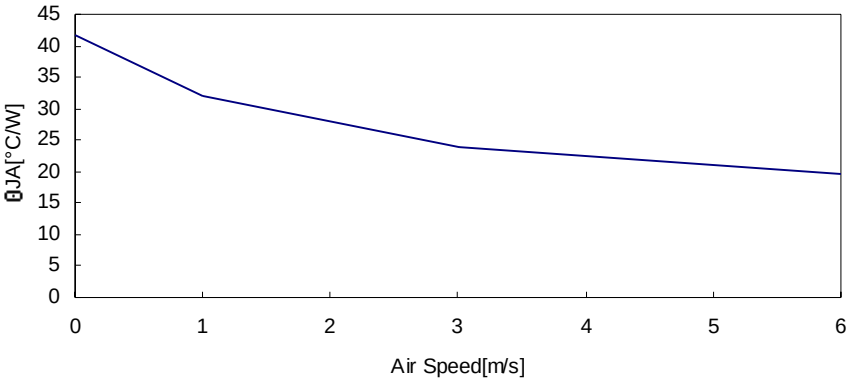
Parameter	Symbol	Value	Unit	Remark
Maximum Supply Voltage	V_{CCMAX}	30	V	-
Maximum Output Current	I_{OMAX}	1.0	A	-
Maximum Power Dissipation[note1]	P_{DMAX}	3.0[note2]	W	-
		5.25[note3]		
Thermal Resistance[note1]	Θ_{JA}	41.57[note2]	°C/W	-
		23.81[note3]		
Operating Temperature	T_{OPR}	–20 ~ +80	°C	-
Storage Temperature	T_{STG}	–50 ~ +150	°C	-

Note 1.
PCB Condition: Thickness (1.6mm), Dimension (76.2mm * 114.3mm)
Refer: EIA/JSED 51-3 & EIA/JSED 51-7
Note 2. Air condition (0m/s)
Note 3. Air condition (3m/s)

Power Dissipation Curve (Air condition = 0m/s)



Air Speed & ΘJA



Recommended Operating Conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating Voltage Range (PV_{CC},SV_{CC})	V_{CC}	20	24	28	V

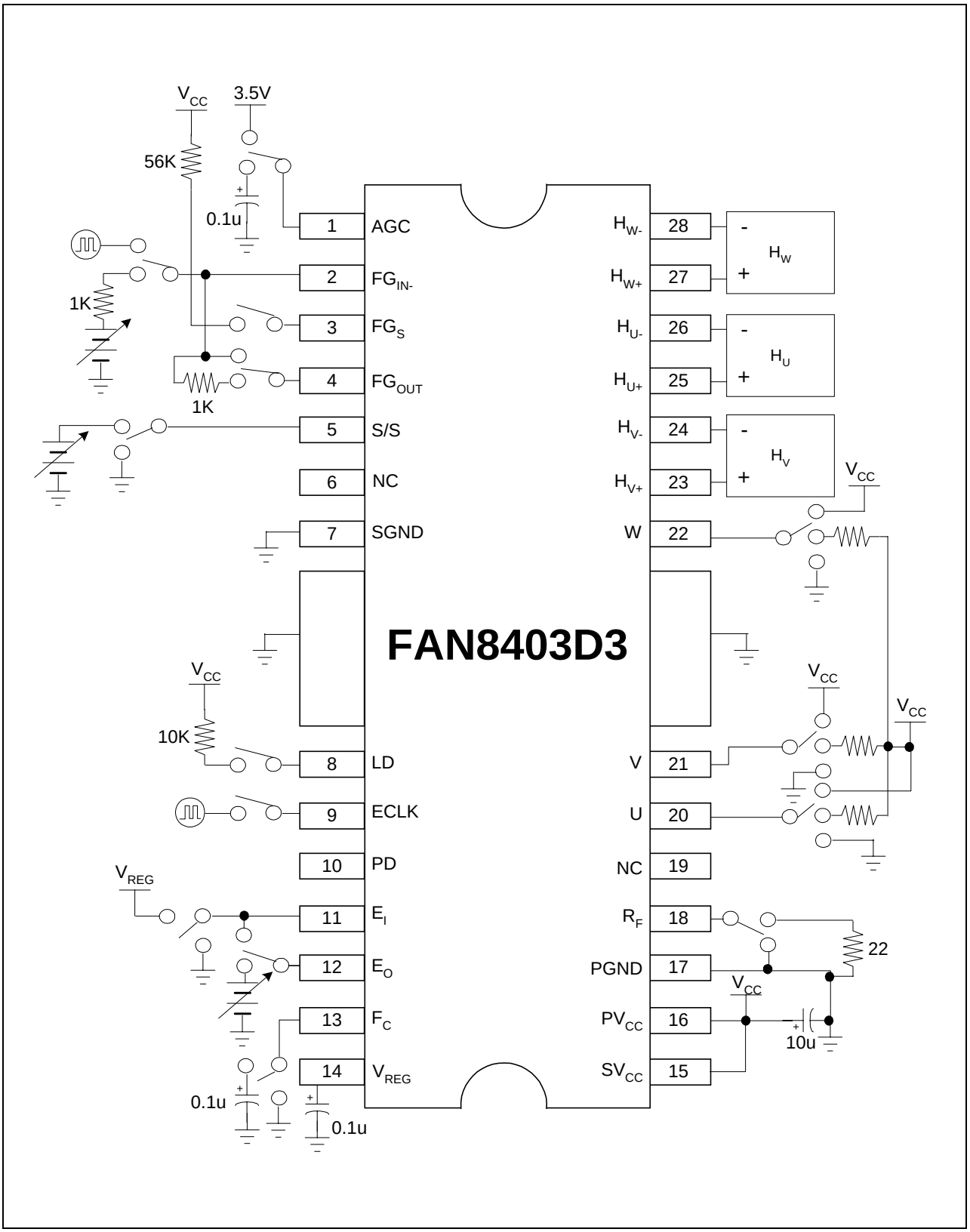
Electrical Characteristics (Ta = 25°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
POWER SUPPLY CURRENT						
Low Power Supply Current	I_{CCL}	Stop mode, V_{CC}=20V	7	17	27	mA
Typical Power Supply Current	I_{CCT}	Stop mode, V_{CC}=24V	7.5	17.5	27.5	mA
High Power Supply Current	I_{CCH}	Stop mode, V_{CC}=28V	8	18	28	mA
OUTPUT POWER TRANSISTOR CHARACTERISTICS						
Source Saturation Voltage (1)	V_{SATU1}	I_O=0.6A, RF=0Ω	-	1.8	2.5	V
Source Saturation Voltage (2)	V_{SATU2}	I_O=0.3A, RF=0Ω	-	1.6	2.3	V
Sink Saturation Voltage (1)	V_{SATL1}	I_O=0.6A, RF=0Ω	-	0.5	1.0	V
Sink Saturation Voltage (2)	V_{SATL2}	I_O=0.3A, RF=0Ω	-	0.25	0.7	V
Output Leakage Current	I_{OLEAK}	V_{CC}=28V, OUT=28V	-	-	100	µA
UNDER VOLTAGE LOCK-OUT						
UVLO Operating Voltage	V_{SD}	-	8.7	9.3	9.9	V
UVLO Hysteresis	HV_{SD}	-	1.3	1.6	1.9	V
REGULATOR VOLTAGE OUTPUT						
Regulator Output Voltage	V_{REG}	-	5.8	6.3	6.8	V
Power Supply Variation	HV_{REG1}	V_{CC}=20~28V	-	-	100	mV
Load Variation	HV_{REG2}	I_{LOAD}=0~10mA	-	-	100	mV
HALL AMPLIFIER INPUT BLOCK						
H+ Hall Amp Input Bias Current	I_{BHA+}	-	-	2	10	µA
H– Hall Amp Input Bias Current	$I_{BHA–}$	-	-	2	10	µA
Hall Differential Input Range	V_{HIN}	Sine wave input	50	-	350	mVp-p
Hall Common Input Range	V_{ICM}	Differential input: 50mVp-p	3.5	-	V_{CC}-3.5	V
FG AMPLIFIER BLOCK						
FG AMP Input Bias Current	I_{BFG}	-	-1	-	1	µA
FG AMP DC Bias Level	V_{BFG}	-	2.90	3.15	3.40	V
FG Output High Level Voltage	V_{OHFG}	No external load	V_{REG}-1.1V	-	-	V
FG Output Low Level Voltage	V_{OLFG}	No external load	-	0.8	1.2	V
FG SCHMIDT COMPARATOR BLOCK						
FG_S High / Low Input Hysteresis	V_{SHL}	-	-50	0	50	mV
FG_S Low / High Input Hysteresis	V_{SLH}	-	100	150	200	mV
FG_S Hysteresis	V_{FGL}	-	100	-	200	mV
FG_S Input Operating Level	V_{FGSIL}	-	400	-	-	mVp-p
FG_S Output Saturation Voltage	V_{FGSSAT}	I_{FGS}=4mA	-	0.2	0.4	V
FG_S Output Leakage Current	$I_{FGSLEAK}$	V_{CC}=28V	-	-	10	µA

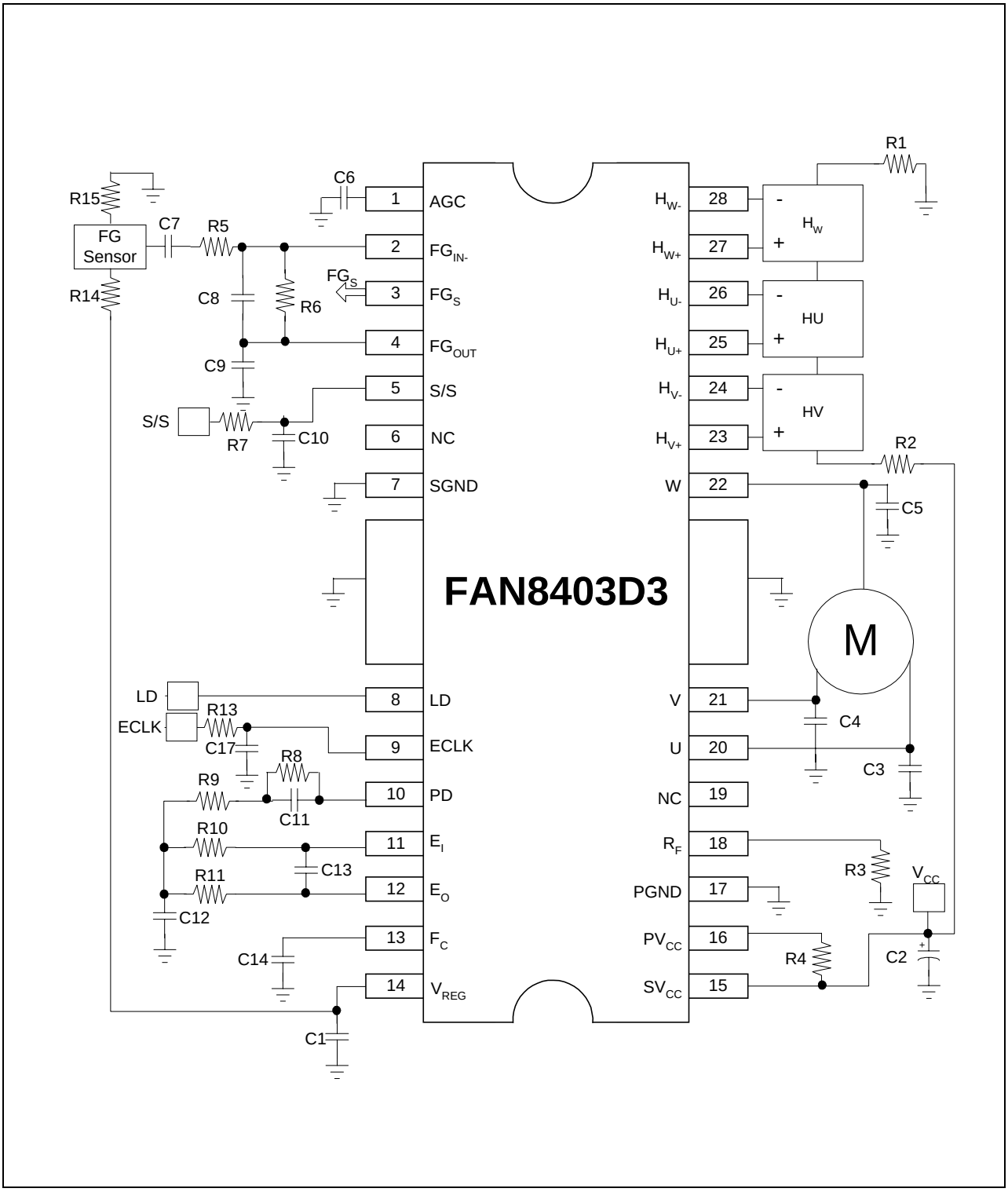
Electrical Characteristics (Continued)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
ERROR AMPLIFIER BLOCK						
Error AMP Input Bias Current	I_{BER}	-	-1	-	1	μA
Error AMP DC Bias Level	V_{BER}	-	2.90	3.15	3.40	V
Error Output High Level Voltage	V_{OHER}	No external load	V_{REG}-1.1V	-	-	V
Error Output Low Level Voltage	V_{OLER}	No external load	-	-	1.0	V
CONTROLLER BLOCK						
Dead Zone	V_{DZ}	-	50	100	300	mV
Output Idle Voltage	V_{ID}	-	-	-	5	mV
Forward Gain	GDF+	-	0.4	0.5	0.6	-
Reverse Gain	GDF–	-	-0.6	-0.5	-0.4	-
Accelerate Command Voltage	V_{STA}	-	V_{REG}-1.1V	-	-	V
Decelerate Command Voltage	V_{STO}	-	-	0.8	1.5	V
Forward Limit Voltage	V_{L+}	RF=22Ω	-	0.60	-	V
Reverse Limit Voltage	$V_{L–}$	RF=22Ω	-	0.60	-	V
CURRENT LIMIT OPERATION						
RF Output Voltage Limit	V_{RF}	-	0.55	0.60	0.65	V
PHASE COMPARATOR OUTPUT BLOCK						
PD Output High Level Voltage	V_{PDH}	No external load	5.2	-	-	V
PD Output Low Level Voltage	V_{PDL}	No external load	-	-	0.7	V
PD Output Source Current	I_{PD+}	V_{PD}=0.5*V_{REG}	-	-	-0.6	mA
PD Output Sink Current	$I_{PD–}$	V_{PD}=0.5*V_{REG}	1.0	-	-	mA
PHASE LOCK DETECTOR OUTPUT BLOCK						
LD Output Saturation Voltage	V_{LDSAT}	I_{LD}=5mA	-	0.1	0.4	V
LD Output Leakage Current	I_{LDLEAK}	V_{CC}=28V	-	-	10	μA
S/S BLOCK						
S/S Input High Level Voltage	V_{IHSS}	-	3.0	-	V_{REG}	V
S/S Input Low Level Voltage	V_{ILSS}	-	0	-	2	V
S/S Hysteresis	V_{ISSS}	-	0.3	0.5	0.7	V
S/S Input Open Voltage	V_{IOSS}	-	3.7	4.2	4.7	V
S/S Input High Level Current	I_{IHSS}	V_{SS}=V_{REG}	100	150	200	μA
S/S Input Low Level Current	I_{ILSS}	V_{SS}=0V	-400	-300	-200	μA
EXTERNAL CLOCK INPUT BLOCK						
ECLK Input High Level Voltage	V_{IHCLK}	-	3.3	-	V_{REG}	V
ECLK Input Low Level Voltage	V_{ILCLK}	-	0	-	2.1	V
External Input Frequency	F_{CLK}	External clock mode	0.5	-	7.0	KHz
ECLK Input Open Voltage	V_{IOCLK}	-	3.7	4.2	4.7	V
ECLK Input High Level Current	I_{IHCLK}	V_{CLK}=V_{REG}	100	150	200	μA
ECLK Input Low Level Current	I_{ILCLK}	V_{CLK}=0V	-400	-300	-200	μA

Test Circuits

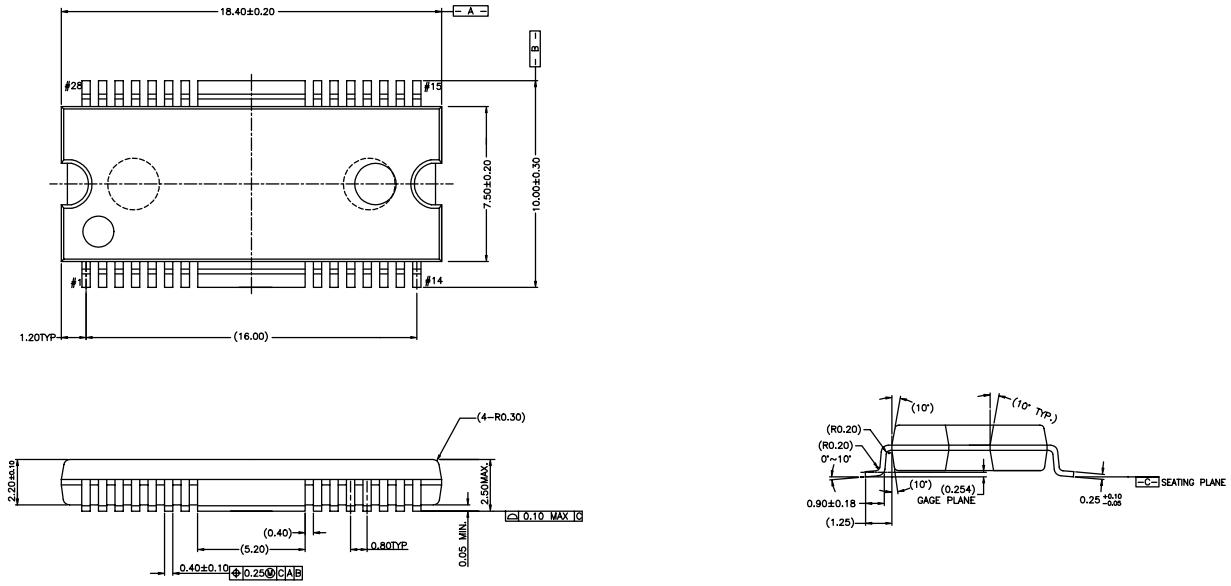


Typical Application Circuits



Package Dimensions (Unit: mm)

28-SSOPH-375SG2



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