

# FDD6035AL

## N-Channel, Logic Level, PowerTrench® MOSFET

### General Description

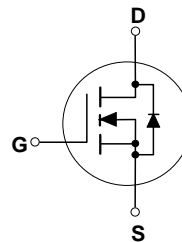
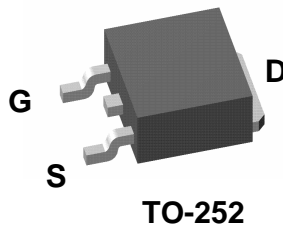
This N-Channel Logic level MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on state resistance and yet maintain low gate charge for superior switching performance.

### Applications

- DC/DC converter
- Motor drives

### Features

- 46 A, 30 V.  $R_{DS(ON)} = 0.0125 \Omega @ V_{GS} = 10 \text{ V}$   
 $R_{DS(ON)} = 0.016 \Omega @ V_{GS} = 4.5 \text{ V}$ .
- Low gate charge (17nC typical).
- Fast switching speed.
- High performance trench technology for extremely low  $R_{DS(ON)}$ .



### Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain-Source Voltage	30	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Drain Current - Continuous (Note 1)	46	A
	Drain Current - Pulsed (Note 1a)	12	
$P_D$	Maximum Power Dissipation @ $T_C = 25^\circ\text{C}$ (Note 1)	50	W
	$T_A = 25^\circ\text{C}$ (Note 1a)	2.8	
	$T_A = 25^\circ\text{C}$ (Note 1b)	1.3	
$T_J, T_{stg}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1a)	2.5	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1b)	96	$^\circ\text{C/W}$

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDD6035AL	FDD6035AL	13"	16mm	2500

## Electrical Characteristics

$T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Drain-Source Avalanche Ratings (Note 1)

$W_{DSS}$	Single Pulse Drain-Source Avalanche Energy	$V_{DD} = 15\text{ V}, I_D = 12\text{ A}$			180	mJ
$I_{AR}$	Maximum Drain-Source Avalanche Current				12	A

### Off Characteristics

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		25		$\text{mV}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$			-100	nA

### On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1	1.6	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		-4		$\text{mV}/^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 12\text{ A}$ $V_{GS} = 10\text{ V}, I_D = 12\text{ A}, T_J = 125^\circ\text{C}$ $V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$		.0009 .0015 .0120	0.0125 0.019 0.016	$\Omega$
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 5\text{ V}$	50			A
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 12\text{ A}$		44		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		1700		pF
$C_{oss}$	Output Capacitance			340		pF
$C_{rss}$	Reverse Transfer Capacitance			140		pF

### Switching Characteristics (Note 2)

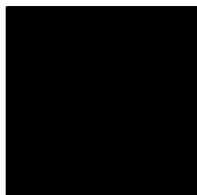
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\ \Omega$		10	18	ns
$t_r$	Turn-On Rise Time			12	22	ns
$t_{d(off)}$	Turn-Off Delay Time			35	56	ns
$t_f$	Turn-Off Fall Time			10	18	ns
$Q_g$	Total Gate Charge	$V_{DS} = 15\text{ V}, I_D = 12\text{ A},$ $V_{GS} = 5\text{ V},$		17	23	nC
$Q_{gs}$	Gate-Source Charge			5		nC
$Q_{gd}$	Gate-Drain Charge			6		nC

### Drain-Source Diode Characteristics and Maximum Ratings

$I_S$	Maximum Continuous Drain-Source Diode Forward Current			2.3	A	
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 2.3\text{ A}$ (Note 2)		0.72	1.3	V

#### Notes:

- $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the drain tab.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a)  $R_{\theta JA} = 45^\circ\text{C}/\text{W}$  when mounted on a  $1\text{ in}^2$  pad of 2oz copper.

b)  $R_{\theta JA} = 96^\circ\text{C}/\text{W}$  on a minimum mounting pad.

- Scale 1 : 1 on letter size paper  
2. Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$

## Typical Characteristics

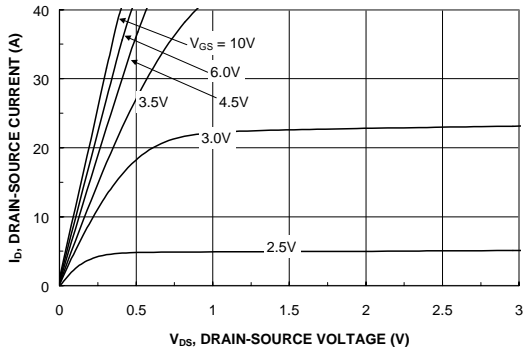


Figure 1. On-Region Characteristics.

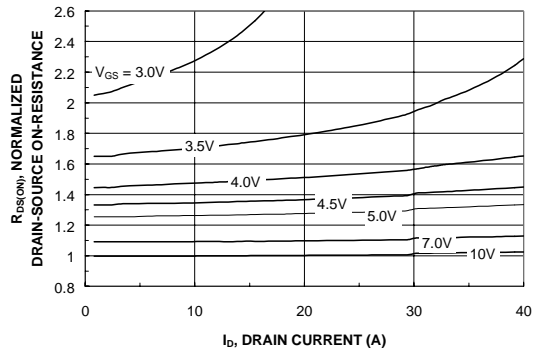


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

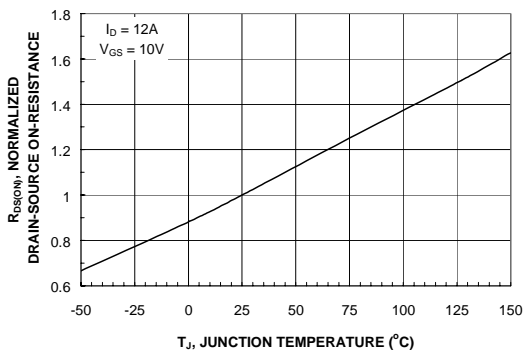


Figure 3. On-Resistance Variation with Temperature.

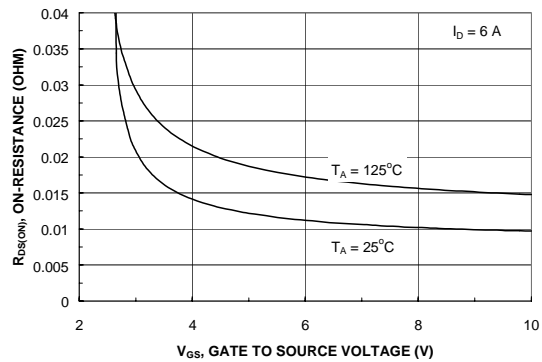


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

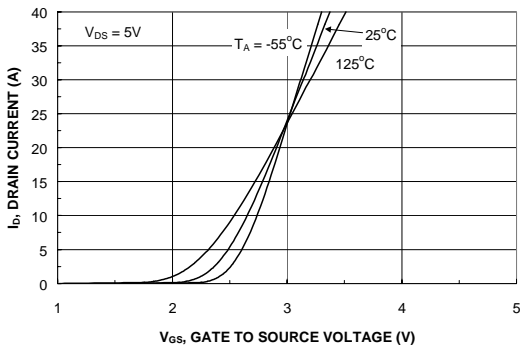


Figure 5. Transfer Characteristics.

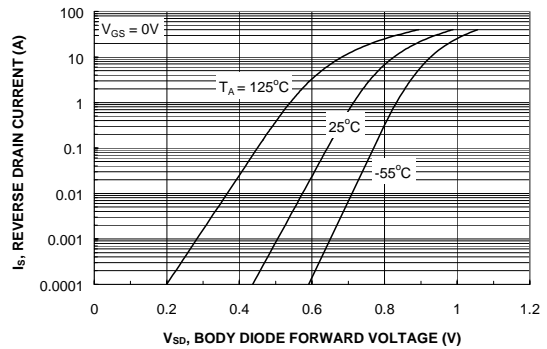


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics (continued)

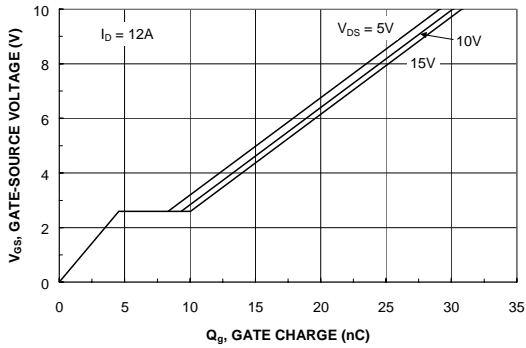


Figure 7. Gate-Charge Characteristics.

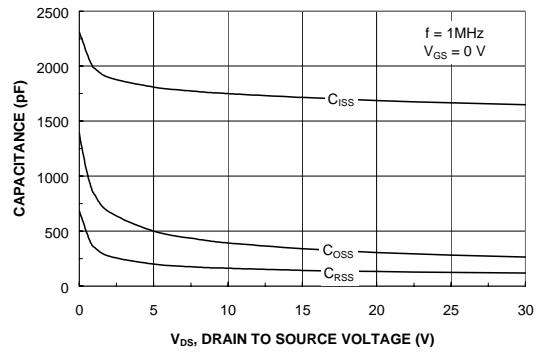


Figure 8. Capacitance Characteristics.

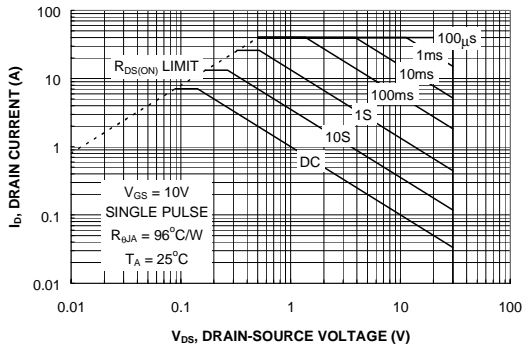


Figure 9. Maximum Safe Operating Area.

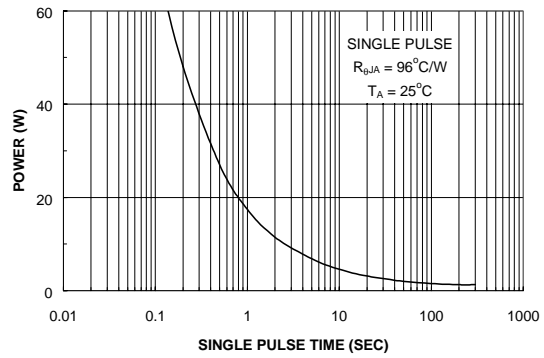


Figure 10. Single Pulse Maximum Power Dissipation.

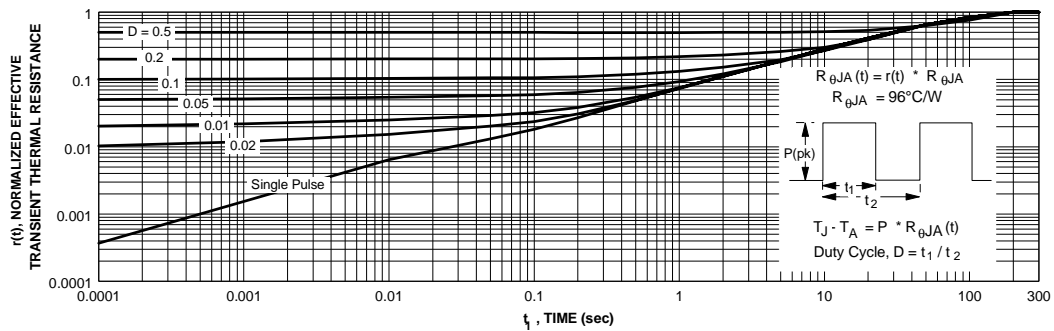


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.

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