

## FEATURES

- **programmable parameters**
  - gain
  - low pass filter
  - high pass filter
  - AGC threshold
  - release time
  - MPO
  - receiver bias voltage
- **on-chip voltage regulator**
- **typical gain 60 dB**
- **voltage drive output stage**
- **telecoil preamp**

## STANDARD PACKAGING

- Chip (136 x 110 mils)  
Au Bump

## CIRCUIT DESCRIPTION

The GP520A is a programmable analog signal path IC designed for use in hearing instruments. The GP520A's programmable parameters are adjusted by external programming currents, such as generated by the GP521. The GP520A provides a  $2.5 \mu\text{A}$  reference current for use by the GP521. Sixteen settings are possible in the GP521, allowing the Programmable Current Sink (PCS) to sink between 0 and  $1.875 \times I_{\text{REF}}$ .

The GP520A is composed of five functional blocks. The input preamp, a filter block, the AGC block, MPO clipper and the output stage.

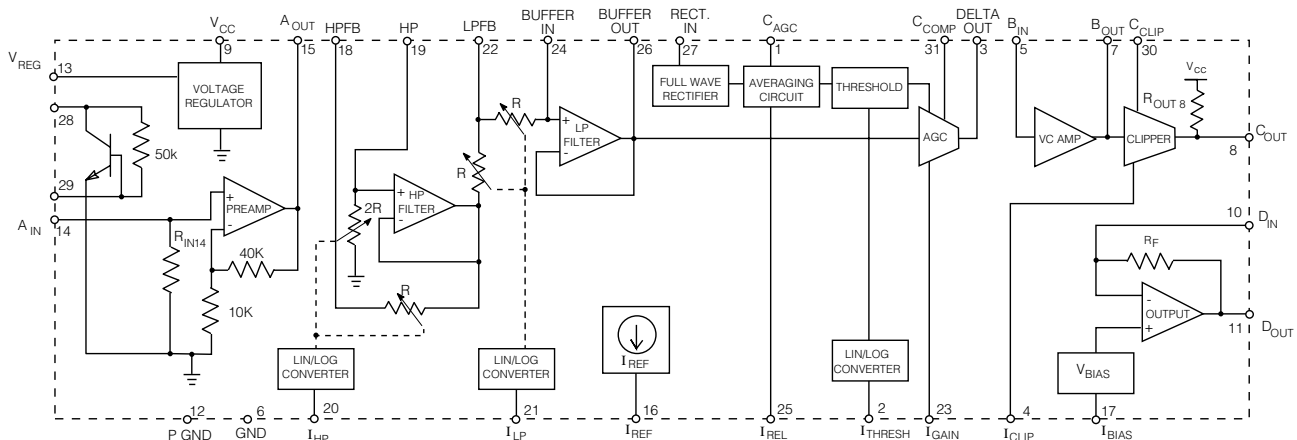
Principle features of the preamp are the input impedance  $100 \text{ k}\Omega$  and a gain of 14 dB.

The programmable filter block is composed of a low pass and high pass filter which generates a range of high and low pass corner frequencies. Although the control current to this block varies linearly, linear to logarithmic conversion is performed internally in order to adjust the corner frequencies logarithmically. Both filters feature a 12 dB/octave rolloff and unity gain.

The filters are followed by an AGC block. Up to 35 dB of adjustable gain is provided as well as programmable threshold and release time. The attack time of the AGC block remains fixed and is independent of the release time. The output current is driven into the preamp of the clipper, thus, the AGC converts a voltage input into a current output and is therefore, a transconductance block.

The next stage is an electronic MPO control peak "clipper" providing electronic clipping of the signal and setting of the maximum output level. The clipper output is also a transconductance block and drives a  $40 \text{ k}\Omega$  resistor ( $R_{\text{OUT } 8}$ ) tied to the supply.

The input of the final stage is an inverting operational amplifier. A feedback resistance of  $240 \text{ k}\Omega$  is provided internally and this final stage is thus configured as a voltage drive output stage. The DC bias current through the receiver is also programmable.



All resistors in ohms, all capacitors in farads unless otherwise stated.

## FUNCTIONAL BLOCK DIAGRAM

## CHIP PAD DIAGRAM

### ABSOLUTE MAXIMUM RATINGS

PARAMETER	VALUE / UNITS
Supply Voltage	5 V
Pad 3, 8, 10, 11, 13, 17	-0.1 V to $V_{CC} + 0.1$ V
Pad 1, 15, 16, 18, 19, 22, 24, 26	-0.1 V to $V_{REG} + 0.1$ V
Pad 4, 5, 7, 14, 20, 21, 23, 25, 27	-0.1 V to 0.7 V
Pad 2	$V_{REG} - 0.7$ V to $V_{REG} + 0.1$ V

**CAUTION**  
CLASS 1 ESD SENSITIVITY



### ELECTRICAL CHARACTERISTICS

All parameters are measured at  $T_A = 25^\circ\text{C}$

All gains are calculated from equation  $G = 20 \text{ LOG} (\Delta\text{OUT}/\Delta\text{IN})$  where  $\Delta\text{OUT}$  and  $\Delta\text{IN}$  are appropriate voltage or current increases.

All resistances are calculated according to equation  $R = (V_P - V_Q) / I_{\text{COND}}$  where  $V_P$  is voltage on the pad loaded with  $I_{\text{COND}}$  current.

$V_Q$  - quiescent (unbias) voltage measured on the pad, (nothing connected to the pin).

$V_P$  is the actual voltage measured on the pad at given condition (where P is pad number).

For all graphs  $I_{\text{REF}}$  is measured with 0.5V biased voltage on pin 16.

#### GENERAL

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Amplifier Current	$I_{\text{AMP}}$	All PCS set to 15	-	600	-	$\mu\text{A}$
Minimum Voltage	$V_{CC}$		1.1	-	-	V

#### REGULATOR TESTS

Regulator Voltage (Pad 13)	$V_{\text{REG}}$		-	0.98	-	V
Short Circuit Current (Pad 13)	$I_{\text{SC}}$	S1 — closed	-	2.0	-	mA

#### CURRENT REFERENCE

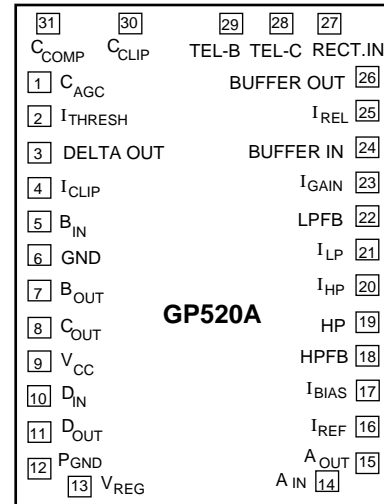
Current Reference (Pad 16)	$I_{\text{R}}$		-	2.5	-	$\mu\text{A}$
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#### PREAMPLIFIER

Quiescent Voltage on Pad 14	$V_{\text{Q14}}$		600	-	-	mV
Quiescent Voltage on Pad 15	$V_{\text{Q15}}$		600	-	-	mV
Input Resistance (Pad 14)	$R_{\text{IN } 14}$	$I_{14} = 0.3\mu\text{A}$ (S2 closed)(Note 1)	-	100	-	$\text{k}\Omega$
Output Swing High (Pad 15)	$V_{\text{OH}}$	$V_{14} = 0.8\text{V}$ (S3 closed)(Note 1)	200	-	-	mV
Output Swing Low (Pad 15)	$V_{\text{OL}}$	$V_1 = 0.4\text{V}$ (S3 closed)	-200	-	-	mV
Max Source Current (Pad 15)	$I_{\text{SOURCE}}$	$V_{14} = 0.8\text{V}$ (S3, S4 closed) $V_{15} = V_{\text{Q15}} + 100\text{mV}$	30	-	-	$\mu\text{A}$
Max Sinking Current (Pad 15)	$I_{\text{SINK}}$	$V_{14} = 0.4\text{V}$ (S3, S4 closed) $V_{15} = V_{\text{Q15}} - 100\text{mV}$	30	-	-	$\mu\text{A}$
Preamplifier Voltage Gain	GAIN	$V_{14} = V_{\text{Q14}} \pm 10\text{mV}$ (S3 closed)	-	14	-	dB

**NOTE: 1.**  $V_{\text{OL}} = V_{\text{OH}} = V_{\text{P15}} - V_{\text{Q15}}$

All switches remain OPEN unless otherwise stated in CONDITIONS column.



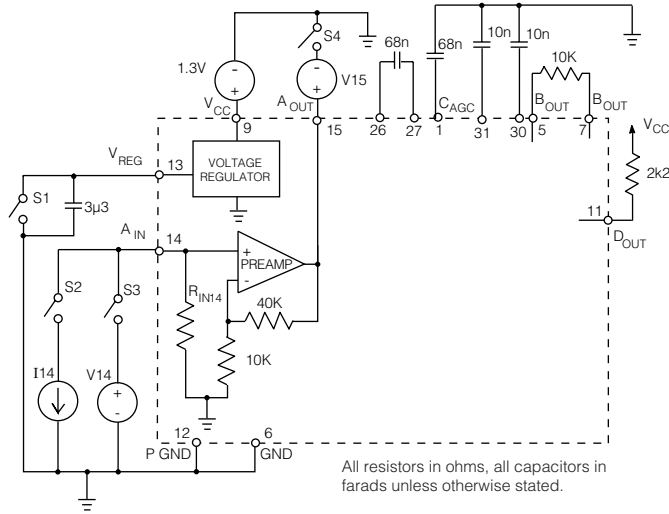


Fig. 1 Preamp and Regulator Test Circuit

**HIGH PASS FILTER**

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Quiescent Voltage on Pad 18	$V_{Q18}$		-	650	-	mV
Quiescent Voltage on Pad 19	$V_{Q19}$		-	650	-	mV
Quiescent Voltage on Pad 20	$V_{Q20}$		-	550	-	mV
Maximum DC Current from Pad 19	$I_{HP\ MAX}$	$I_{HP} = 0\mu A$ (S3 closed)	-	2	-	$\mu A$
Minimum DC Current from Pad 19	$I_{HP\ MIN}$	$I_{HP} = 1.875 \times I_R$ (S3 closed)	-	200	-	nA
Buffer Gain	GAIN	$V_{19} = V_{Q19} \pm 100mV$ (S2 closed)	-	0	-	dB
Input Resistance Pad 20	$R_{IN20}$	$I_{HP} = I_R$	-	13	-	$k\Omega$

All switches remain OPEN unless otherwise stated in CONDITIONS column.

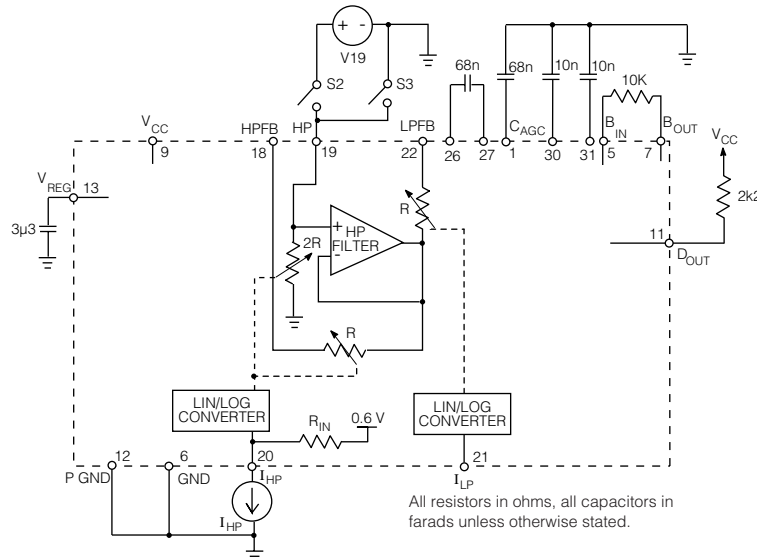


Fig. 2 High Pass Filter DC Test Circuit

## LOW PASS FILTER

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Quiescent Voltage on Pad 21	$V_{Q21}$		-	550	-	mV
Quiescent Voltage on Pad 22	$V_{Q22}$		-	650	-	mV
Quiescent Voltage on Pad 24	$V_{Q24}$		-	650	-	mV
Quiescent Voltage on Pad 26	$V_{Q26}$		-	650	-	mV
Maximum DC Current from Pad 22	$I_{LP\ MAX}$	$I_{LP} = 0\mu A$ (S1 closed)	-	2.0	-	$\mu A$
Minimum DC Current from Pad 22	$I_{LP\ MIN}$	$I_{LP} = 1.875 \times I_R$ (S1 closed)	-	0.7	-	$\mu A$
Output Swing High (Pad 26)	$V_{OH}$	$V_{24} = V_{Q24} + 100mV$ (S2 closed)(Note 1)	-	100	-	mV
Output Swing Low (Pad 26)	$V_{OL}$	$V_{24} = V_{Q24} - 100mV$ (S2 closed )(Note 1)	-	-100	-	mV
Max Sinking Current from Pad 26	$I_{SINK}$	$V_{24} = 0.4V$ ; $V_{26} = V_{Q26} - 100mV$ (S2, S3 closed)	30	-	-	$\mu A$
Max Sourcing Current to Pad 26	$I_{SOURCE}$	$V_{24} = 0.8V$ ; $V_{26} = V_{Q26} \pm 100mV$ (S2, S3 closed)	-30	-	-	$\mu A$
Buffer Gain	GAIN	$V_{26} = V_{Q26} \pm 100mV$	-	0	-	dB
Input Resistance (Pad 21)	$R_{IN21}$	$I_{LP} = I_R$	-	13	-	$k\Omega$

NOTE: 1.  $V_{OH} = V_{OL} = V_{P26} - V_{Q26}$

All switches remain OPEN unless otherwise stated in CONDITIONS column.

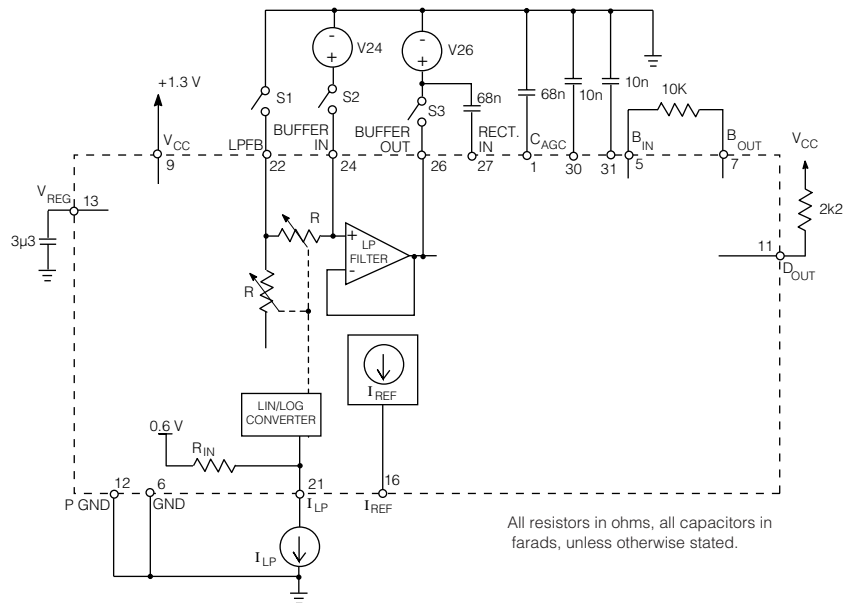


Fig. 3 Low Pass Filter DC Test Circuit

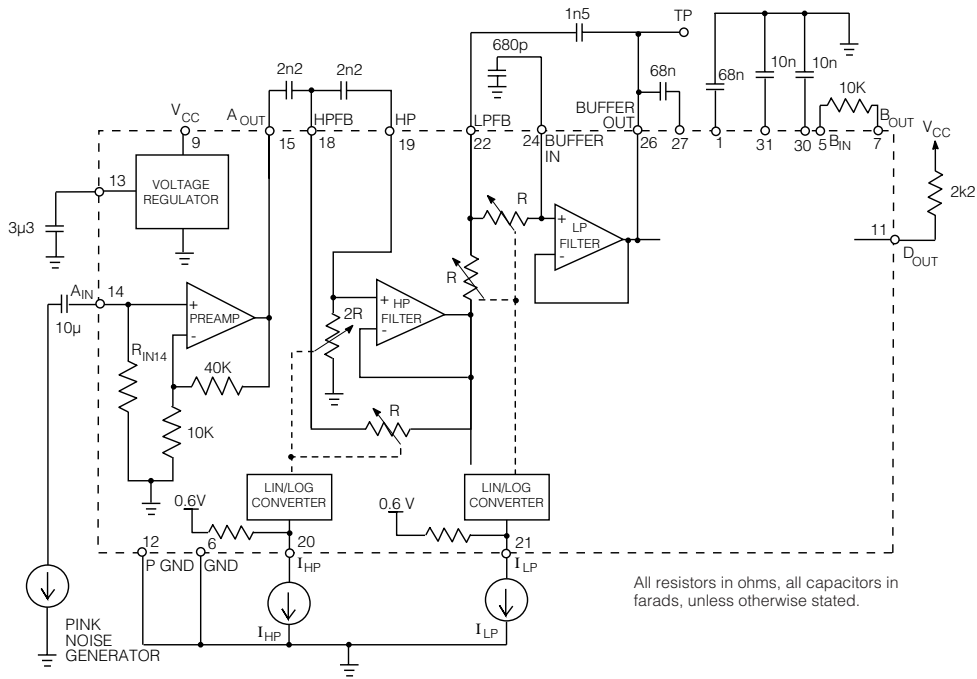


Fig. 4 AC Test Circuit for High & Low Pass Filters

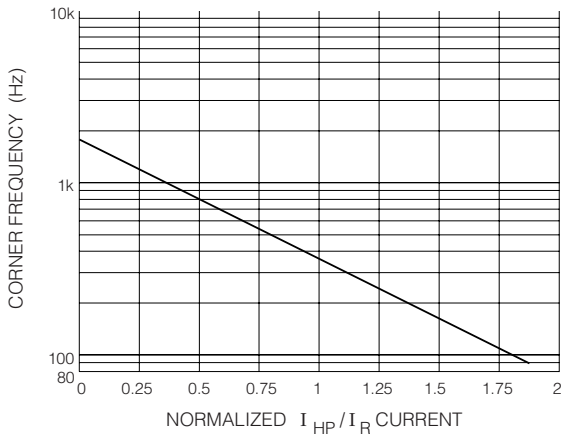


Fig. 5 High Pass Filter Corner Frequency vs  $I_{HP}$  Current (Note 1) (Fig.4 Test Circuit)

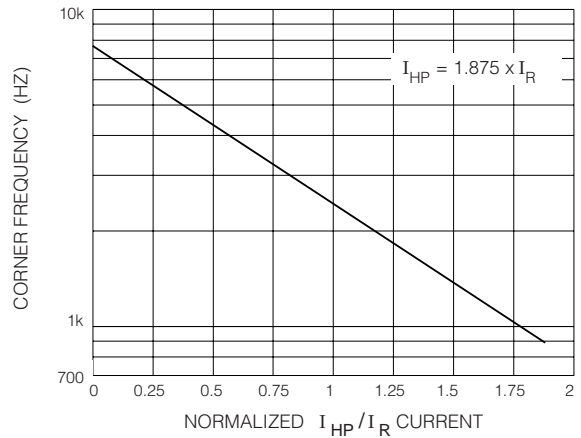


Fig. 6 Low Pass Filter Corner Frequency vs  $I_{LP}$  Current (Note 1) (Fig.4 Test Circuit)

NOTES: 1. Corner frequency calculated in reference to signal at 3 kHz

## AGC CONTROL STAGE

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Quiescent Voltage on Pad 2	$V_{Q2}$	$I_{THRESH} = I_R$	-	400	-	mV
Quiescent Voltage on Pad 3	$V_{Q3}$	$I_{GAIN} = I_R \times 1.875$	-	700	-	mV
Quiescent Voltage on Pad 23	$V_{Q23}$		-	500	-	mV
Quiescent Voltage on Pad 25	$V_{Q25}$		-	500	-	mV
Quiescent Voltage on Pad 27	$V_{Q27}$		-	600	-	mV
Release Current Max (Pad 1)	$I_{REL\ MAX}$	$I_{REL} = 0$ (S1 closed)	-	300	-	nA
Release Current Min (Pad 1)	$I_{REL\ MIN}$	$I_{REL} = 1.875 \times I_R$ (S1 closed)	-	30	-	nA
Input Resistance (Pad 25)	$R_{IN25}$	$I_{REL} = I_R$	-	17	-	k $\Omega$
Input Resistance (Pad 27)	$R_{IN27}$	$I_{27} = \pm I_R$	-	4	-	k $\Omega$
Max Transconductance (Pad 26 to $V_O$ )	$G_{MAX}$	$I_{GAIN} = I_R \times 2 \times 1.875$ $V_{P26} = 30$ mVpp $I_{THRESH} = 1.875 \times I_R$ (Note 1)	-	160	-	$\mu$ A/V
Gain Range (Pad 26 to $V_O$ )	$GAIN_{RANGE}$	$I_{THRESH} = 1.875 \times I_R$ (Note 2) $V_{26} = 25$ mVpp	-	33	-	dB
Output Limiting Level (Pad 3)	$OUT_{LIM}$	$I_{THRESH} = I_R$ , $I_{GAIN} = 2 \times 1.875 \times I_R$ $V_{26} = 100$ mVpp (Note 3)	-	0.7	-	$\mu$ ARMS
Limiting Level Range	$LIM_{RANGE}$	$I_{GAIN} = I_R \times 2 \times 1.875$ (Note 4) $V_{26} = 100$ mVpp	-	13	-	dB
AGC Compression Ratio	$CMP_{RAT}$	$I_{THRESH} = I_R$ $I_{GAIN} = 2 \times 1.875 \times I_R$ (Note 5)	-	5	-	

Unless otherwise stated in CONDITIONS column all switches remain OPEN, all current sources are 0 $\mu$ A

### NOTES:

- $G_{MAX} = V_O / (V_{26} \times 1M)$
- $GAIN_{RANGE} = 20 \text{ LOG } (V_O [I_{GAIN} = 2 \times 1.875 \times I_R] / V_O [I_{GAIN} = 0])$
- $OUT_{LIM} = V_O / 1M$
- $LIM_{RANGE} = 20 \text{ LOG } (V_O [I_{THRESH} = 1.875 \times I_R] / V_O [I_{THRESH} = 0])$
- $CMP_{RAT} = \frac{10}{20 \text{ LOG } (V_O [V_{26} = 5.62 \text{ mVRMS}] / V_O [V_{26} = 17.8 \text{ mVRMS}]) - 45 \text{ dBV} - 35 \text{ dBV}}$

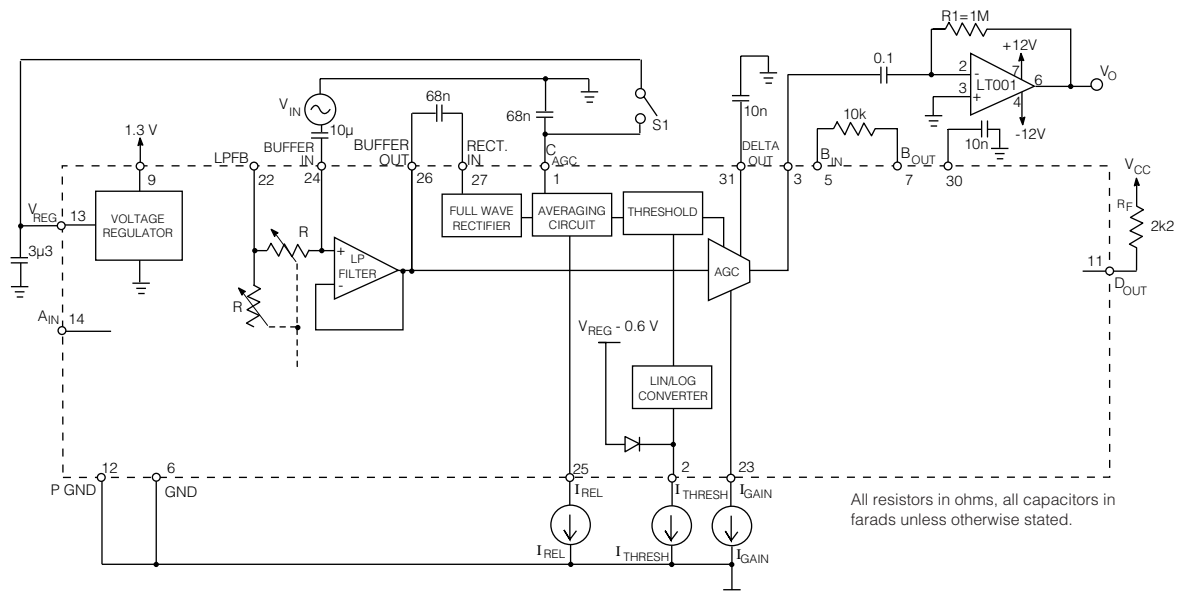


Fig. 7 AGC Control Stage Test Circuit

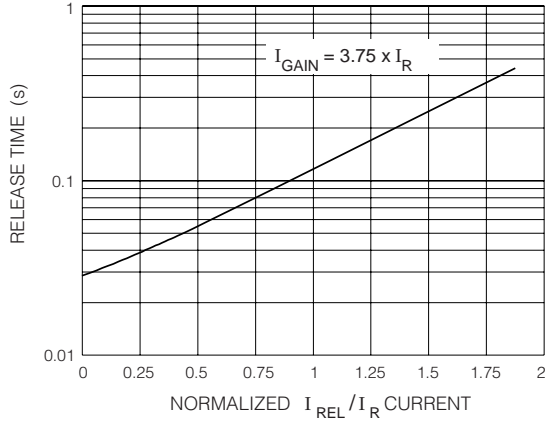


Fig. 8 Release Time vs  $I_{REL}$  (Fig.7 Test Circuit)

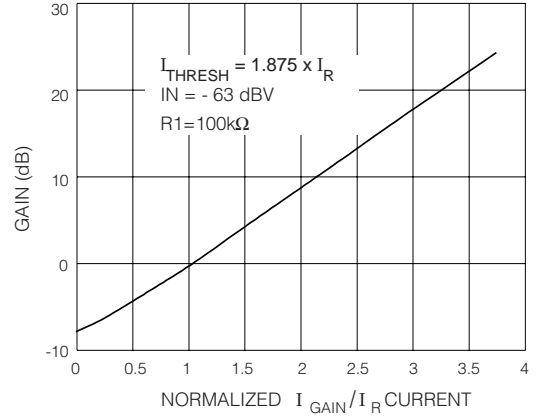


Fig. 9 AGC Gain vs  $I_{GAIN}$  (Fig.7 Test Circuit)

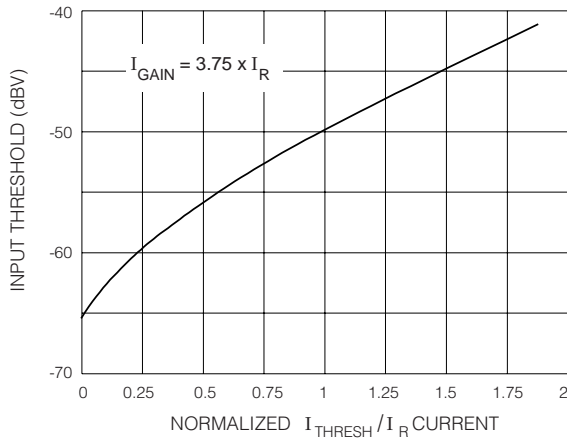


Fig. 10 Threshold Level vs  $I_{THRESH}$  (Fig.7 Test Circuit)

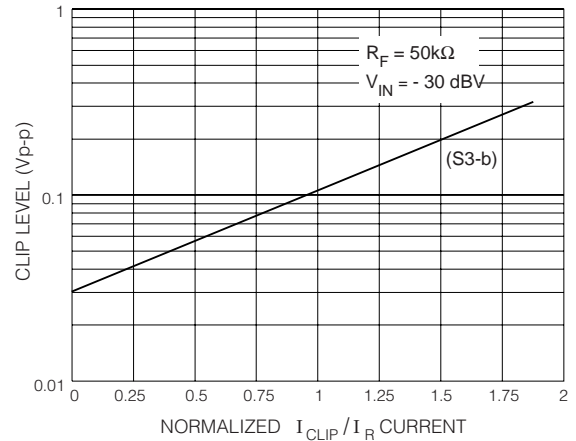


Fig. 11 Output Swing vs  $I_{CLIP}$  (Fig.13 Test Circuit) (note 1)

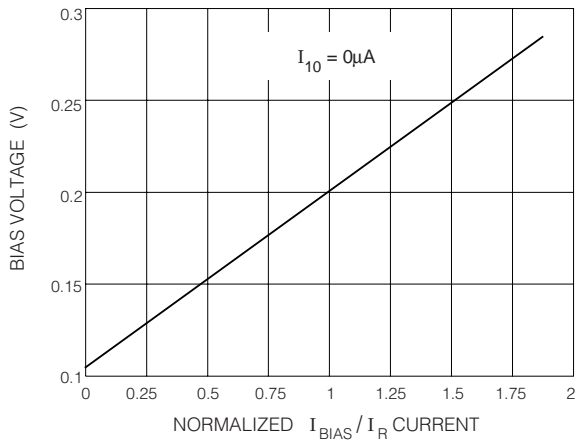


Fig. 12 Receiver Bias Voltage vs  $I_{BIAS}$  (Fig. 14 Test Circuit)

NOTE: 1. Switch S2 - open, S4 - closed.

## CLIPPER STAGE

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Quiescent Voltage on Pad 5	$V_{Q5}$	(S1 closed)	-	550	-	mV
Input Bias Current (Pad 5)	$I_{BIAS}$	$R_{F1}=1M$ $R_{F2}=0\Omega$ (Note 1)	-	0	-	nA
Quiescent Voltage on Pad 4	$V_{Q4}$		-	500	-	mV
Quiescent Voltage on Pad 8	$V_{Q8}$		-	1.2	-	V
Output Swing High 1 (Pad 8)	$V_{OH1}$	$I_{IN} = +1\mu A$ $I_{CLIP} = 0\mu A$ (Note 2)	5	-	-	mV
Output Swing Low 1 (Pad 8)	$V_{OL1}$	$I_{IN} = -1\mu A$ $I_{CLIP} = 0\mu A$ (Note 2)	-5	-	-	mV
Output Clip Symmetry 1	$V_{SYM1}$	(Note 3)	-	1	-	
Output Swing High 2 (Pad 8)	$V_{OH2}$	$I_{IN} = 5\mu A$ $I_{CLIP} = 1.875 \times I_R$ (Note 2)	-	50	-	mV
Output Swing Low 2 (Pad 8)	$V_{OL2}$	$I_{IN} = -5\mu A$ $I_{CLIP} = 1.875 \times I_R$ (Note 2)	-	-50	-	mV
Output Clip Symmetry 2	$V_{SYM2}$	(Note 3)	-	1	-	
Output Resistance (Pad 8)	$R_{OUT8}$	$I_{P8} = 10\mu A$ (S2 closed)	-	40	-	k $\Omega$
Clipper Voltage Gain	GAIN	$V_{IN} = 50mV_{pp}$ (S3-b) $I_{CLIP} = 1.875 \times I_R$ (Note 4)	-	12	-	dB

All switches remain as shown in the Test Circuit unless otherwise stated in CONDITIONS column.

**NOTES:** 1.  $I_{BIAS} = (V_7 \Big|_{R_F=1M\Omega} - V_7 \Big|_{R_F=0\Omega}) / 1M\Omega$

3.  $V_{SYM} = (2V_{OH} / (V_{OH} - V_{OL}))$

2.  $V_{OL} = V_{OH} = V_{Q8} - V_8$

4.  $GAIN = 20 \log (V_8 / V_7)$

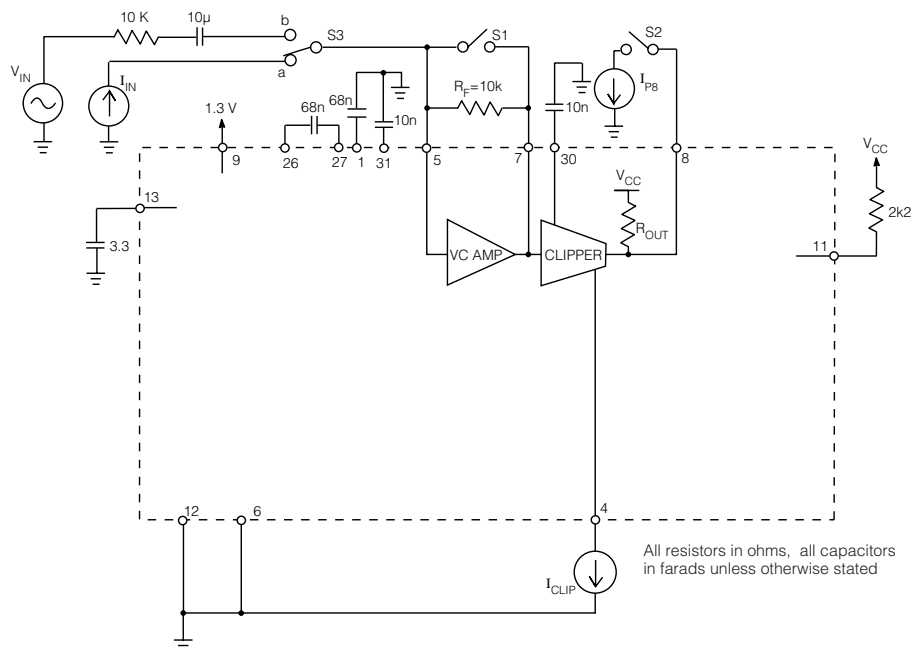


Fig. 13 Clipper Test Circuit



## OUTPUT STAGE

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Quiescent Voltage on Pad 17	$V_{17}$		-	1.2	-	V
Min Receiver Bias Voltage	$V_{REC\ MIN}$	$I_{BIAS} = 0\mu A$ (Note 1)	-	100	-	mV
Max Receiver Bias Voltage	$V_{REC\ MAX}$	$I_{BIAS} = I_R \times 1.875$ (Note 1)	-	300	-	mV
Input Resistance Pad 17	$R_{IN17}$	$I_{BIAS} = I_R$	-	40	-	k $\Omega$
Internal Feedback Resistor	$R_F$	$I_{10} = I_R$	-	240	-	k $\Omega$
Max Sinking Current (Pad 11)	$I_{SINK}$	(S1 closed)	-	10	-	mA

**NOTE:** 1.  $V_{REC} = V_{CC} - V_{11}$

All switches remain as shown in the Test Circuit otherwise stated in the CONDITION column.

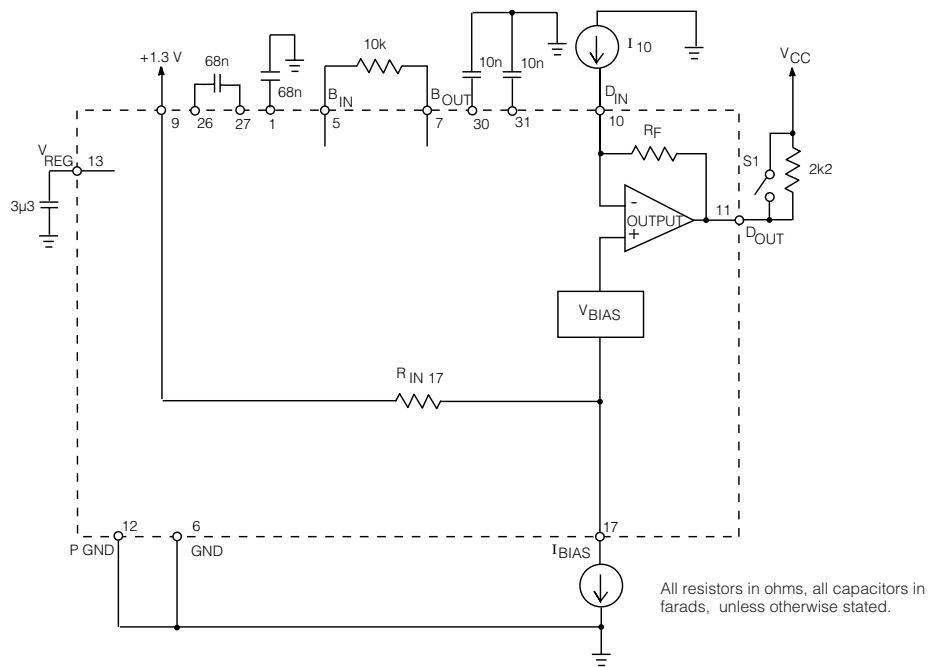
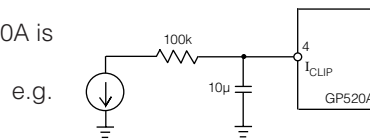


Fig. 14 Output Stage Test Circuit

### COMMENTS:

- Pin 23 and Pin 4 represent virtual ground inputs.
- If the length of the wires between the current sources and the GP520A is extensive, it may be necessary to connect an RC filter close to the appropriate GP520A pin for noise immunity.



All resistors in ohms, all capacitors in farads, unless otherwise stated.

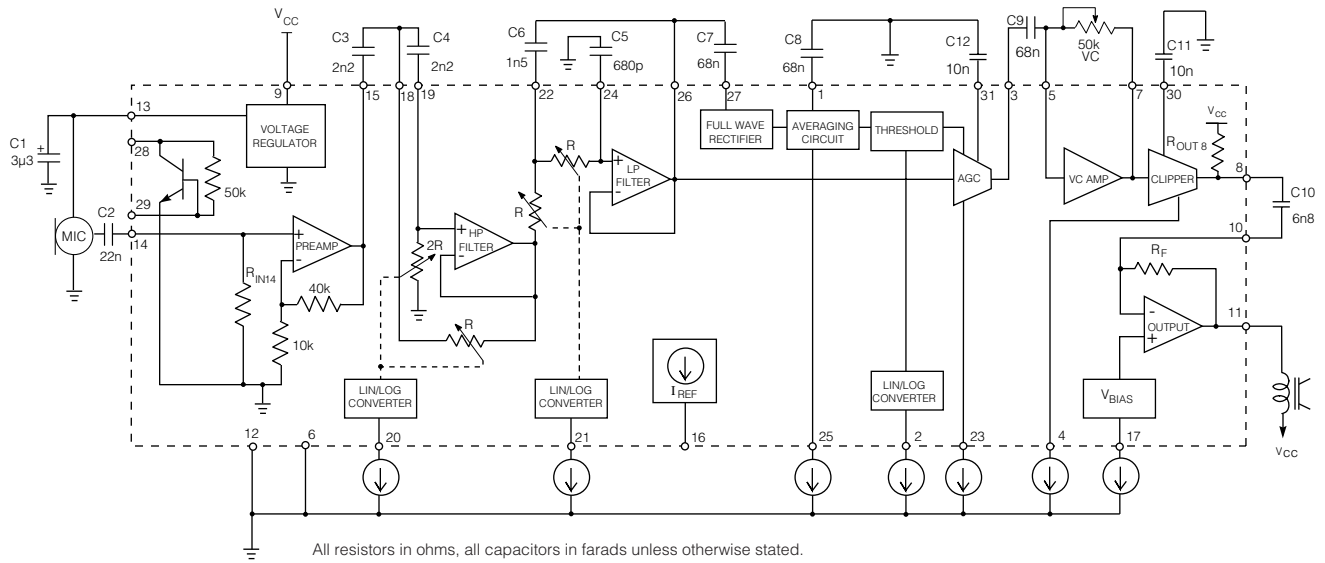


Fig. 15 Typical Application Circuit

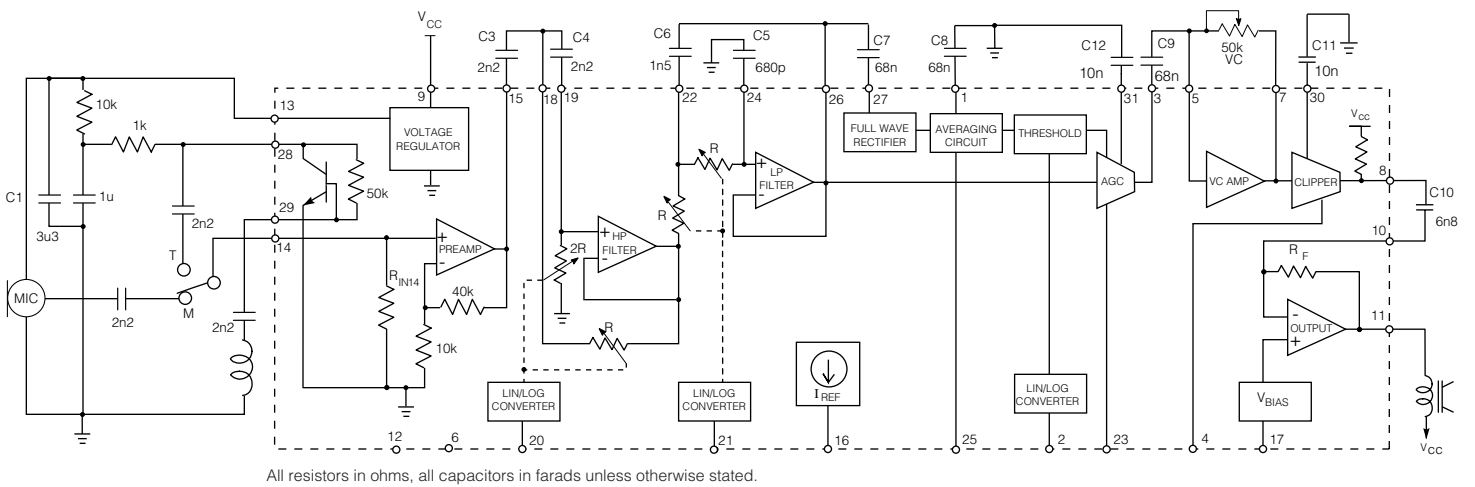


Fig. 16 Typical Telecoil Application Circuit

**DOCUMENT IDENTIFICATION: DATA SHEET**

The product is in production. Gennum reserves the right to make changes at any time to improve reliability, function or design, in order to provide the best product possible.

**REVISION NOTES:**

Updated to Data sheet