PRO-LINX™ GS7000
Serial Digital Video Transceiver

PRELIMINARY DATA SHEET

GS7000

FEATURES

- **fully integrated 270Mb/s SDI receiver or transmitter**
- **fully compliant with SMPTE 259M-C**
- **lock and carrier detect output indication**
- **performance from 0 - 85°C**

RECEIVER FUNCTION

- **accepts SMPTE 259M-C 270Mb/s serial digital video and outputs SMPTE 125M compliant 27Mb/s parallel digital video and clock**
- **integrated cable equalization (beyond 100m Belden 8281)**
- **ease of design use and adjustment free operation**
- **H timing signal output**

TRANSMITTER FUNCTION

- **accepts SMPTE 125M (27Mb/s) parallel video data and clock, outputs SMPTE 259M-C 270Mb/s serial digital video**
- **integrated cable driver provides one differential output (or two single-ended outputs)**

APPLICATIONS

Space limited, low power 270Mb/s serial to parallel or parallel to serial interfaces; Alternate, broadcast quality uncompressed video interface for industrial and professional video equipment using the IEEE P1394 interface.

DESCRIPTION

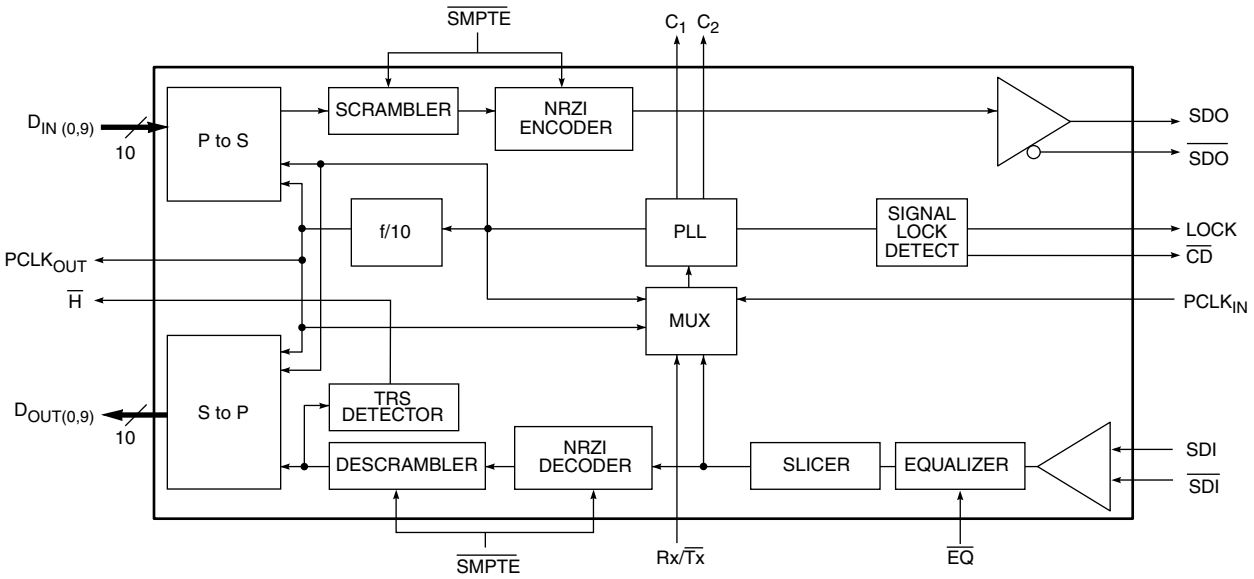
The GS7000 is a dual function IC capable of operating as either a 270Mb/s Serial Digital Video receiver or a 270Mb/s Serial Digital Video transmitter. The GS7000 is designed so that it can be programmed to operate in either receive or transmit mode via a mode select pin.

When operating as a receiver, the serial data input accepts SMPTE 259M-C compliant signals. Line terminations are on the device. An on-chip by-passable fixed gain equalizer provides cable equalization beyond 100m of high quality co-axial cable. The clock recovery is performed on chip with minimal external components. Incoming Serial Digital Video data is decoded using a NRZI decoder and SMPTE descrambler to provide clocked SMPTE 125M compliant parallel output. The SMPTE descrambler and NRZI decoding functions can be disabled.

When operating as a transmitter, the GS7000 accepts parallel SMPTE 125M compliant ten bit video. An on-chip scrambler and NRZI encoder converts the parallel data into a bit serial SMPTE 259M-C compliant NRZI output signal suitable for driving co-axial cable. Through the $\overline{\text{SMPTE}}$ select pin, the SMPTE scrambler and NRZI coding functions can be disabled.

ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMPERATURE
GS7000-CQT	52 pin MQFP	0°C to 85°C
GS7000-CTT	52 pin MQFP Tape	0°C to 85°C



BLOCK DIAGRAM

GENNUM CORPORATION P.O. Box 489, Stn. A, Burlington, Ontario, Canada L7R 3Y3
Tel. +1 (905) 632-2996 Fax. +1 (905) 632-5946 E-mail: info@gennum.com
www.gennum.com

ABSOLUTE MAXIMUM RATINGS

PARAMETER	VALUE
Supply Voltage	5.5V
Input Voltage Range (any input)	$V_{EE} < V_{IN} < V_{CC}$
DC Input Current (any one input)	10mA
Power Dissipation (V_{CC} = 5.25 V)	830mW
Maximum Die Temperature	125°C
Operating Temperature Range	$0°C \le T_A \le 85°C$
Storage Temperature Range	$-65°C \le T_S \le 150°C$
Lead Temperature (soldering 10s)	260°C

AC ELECTRICAL CHARACTERISTICS (Receiver Mode)

V_{CC} = 5V, V_{EE} = 0V, T_A = 0°C to 85°C, unless otherwise specified.
Serial Data Rate = 270Mb/s, Parallel Data Rate = 27Mb/s, f_{PCLK} = 27MHz

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES	TEST LEVEL
Parallel Data Output - Rise/Fall Time	C_L = 20pF	t_{R/F_PDO}	1.0	-	6.0	ns	1	1
PCLK rising edge to $D_{OUT(n)}$ center		t_D	-	-	± 5	ns	2, 3	1
PCLK rise/fall time	C_L = 20pF	t_{R/F_PCLKo}	0.5	-	3.0	ns	1	1
Input Return Loss	75Ω match 5MHz -> 270MHz	$LOSS_{IN}$	-	17	-	dB		6
Asynchronous Lock Time		t_{LOCK_ASYNC}	-	-	250	ms	4	1
Synchronous Lock Time		t_{LOCK_SYNC}	-	-	10	µs	5	1
Input Jitter Tolerance	pathological Input	t_{J_SI}	-	0.4	-	U.I.	6	4
Output PCLK Jitter	pathological Input	t_{J_PCLKo}	-	1000	-	ps p-p	6	1
Max Error Free Cable Length	pathological Input		75	100	-	m	6, 7	1, 4

NOTES

1. Rise/Fall time is defined as the time for the signal to rise from 20% to 80% of the specified p-p value, or to fall from 80% to 20% of the specified value.
2. Refer also to Figure 21.
3. This is the time difference between the rising edge of $PCLK_{OUT}$ and the center of the bit period.
4. This is the time delay between a valid serial TRS signal on the input, to the moment valid data appears on the parallel outputs.
5. This is the time for the PLL to re-lock when video streams are switched during the vertical blanking interval in accordance with SMPTE RP168-1993. The two streams may be 180° out of phase with respect to one another, but pixel aligned.
6. This pathological pattern is defined in SMPTE RP178-1996, paragraphs 4.1 and 4.3.
7. "Error free" is defined as no single bit errors over a period of 10 minutes, using Belden 8281 Cable and 75Ω connections. The MIN value is fully tested and the TYP value is based on using the EB7000 Evaluation Board.

TEST LEVELS

1. 100% tested at 25 °C
2. Guaranteed by design
3. Inferred or correlated value
4. Evaluated using test setup Figure 1a.
5. Evaluated using test setup Figure 1b.
6. Evaluated using test setup Figure 1c.

AC ELECTRICAL CHARACTERISTICS (Transmitter Mode)

V_{CC} = 5V, V_{EE} = 0V, T_A = 0°C to 85°C, unless otherwise specified in 'conditions'
Serial Data Rate = 270Mb/s, Parallel Data Rate = 27Mb/s, f_{PCLK} = 27MHz

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES	TEST LEVEL
Parallel Data Inputs - rise/fall time		t_{R/F_DPI}	0.5		10	ns	1	2
Parallel Data Inputs - setup		t_{SETUP}	4	-	-	ns	8	1
Parallel Data Inputs - hold		t_{HOLD}	4	-	-	ns	8	1
Parallel Data Inputs - high	V_{CC} = 5.25V	V_{DPI}	2.0	-	V_{CC}	V		1
Parallel Data Inputs - low	V_{CC} = 4.75V	V_{DPI}	V_{EE}	-	0.8	V		1
Parallel Clock Input - rise/fall time		t_{R/F_PCLK}	0.5	-	4	ns		2
Serial Data Output - signal swing	V_{CC} = 4.75 - 5.25V	V_{DSO}	720	800	880	mV p-p	9, 10	1
Serial Data Output - high		V_{OH}	-	V_{CC} - 0.8	-	V	11	2
Serial Data Output - low		V_{OL}	-	V_{CC} - 1.6	-	V	11	2
Serial Data Output - rise/fall time		$t_{R/F}$	400	600	1500	ps	1	1
Serial Data Output - jitter	V_{CC} = 4.75V	t_{J_DSO}	-	-	675	ps p-p	12	1
Lock Time		t_{LOCK}	-	-	250	ms	13	1
Output Return Loss	270MHz		15	-	-	dB		6

NOTES

8. Refer to Figure 26.
9. The outputs are capable of driving a 75Ω single-ended load, terminated to ground.
10. This value is measured after the resistor network at the SDI outputs shown in Figure 2.
11. Typical PECL values
12. 6σ additive intrinsic jitter contribution based on pathological input signal
13. This is the lapsed time between valid parallel TRS input to valid serial output

TEST LEVELS

1. 100% tested at 25°C
2. Guaranteed by design
3. Inferred or correlated value
4. Evaluated using test setup Figure 1a.
5. Evaluated using test setup Figure 1b.
6. Evaluated using test setup Figure 1c.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, V_{EE} = 0V, T_A = 0°C to 85°C, unless otherwise specified.
Serial Data Rate = 270Mb/s, Parallel Data Rate = 27Mb/s, f_{PCLK} = 27MHz

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	TEST LEVEL
Positive Supply Voltage		V_{CC}	+ 4.75	+ 5.00	+ 5.25	V	
Supply Current - Receive Mode	V_{CC} = 5.25V	I_{CC}	-	150	-	mA	1
Supply Current - Transmit Mode	V_{CC} = 5.25V	I_{CC}	-	130	-	mA	1
Power Consumption - Receive Mode	V_{CC} = 5.25V	P_D	-	750	-	mW	3
Power Consumption - Transmit Mode	V_{CC} = 5.25V	P_D	-	650	-	mW	3
Logic Inputs - Low	V_{CC} = 5.25V	V_{IL}	V_{EE}	-	0.8	V	2
Logic Inputs - High	V_{CC} = 4.75V	V_{IH}	2.0	-	V_{CC}	V	2
Logic Outputs - Low	V_{CC} = 5.25V	V_{OL}	V_{EE}	-	0.5	V	2
Logic Outputs - High	V_{CC} = 4.75V	V_{OH}	2.4	-	V_{CC}	V	2

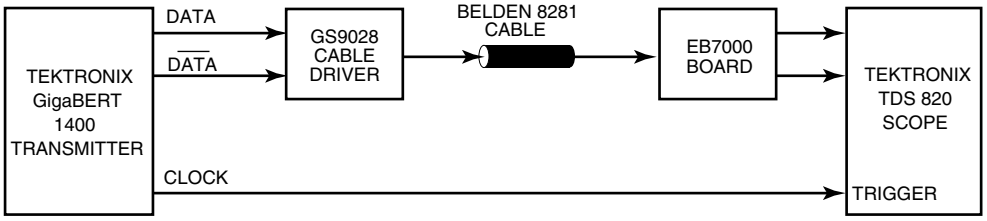


Fig. 1a Test Setup for Jitter Measurements

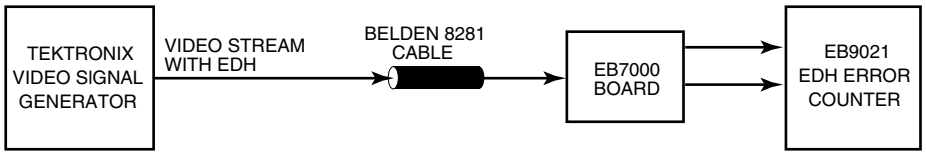


Fig. 1b Test Setup for Error-Free Cable Length

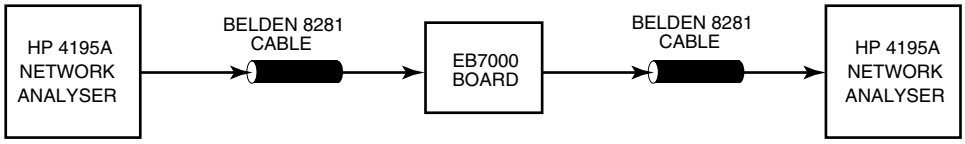


Fig. 1c Test Setup for Return Loss Measurements

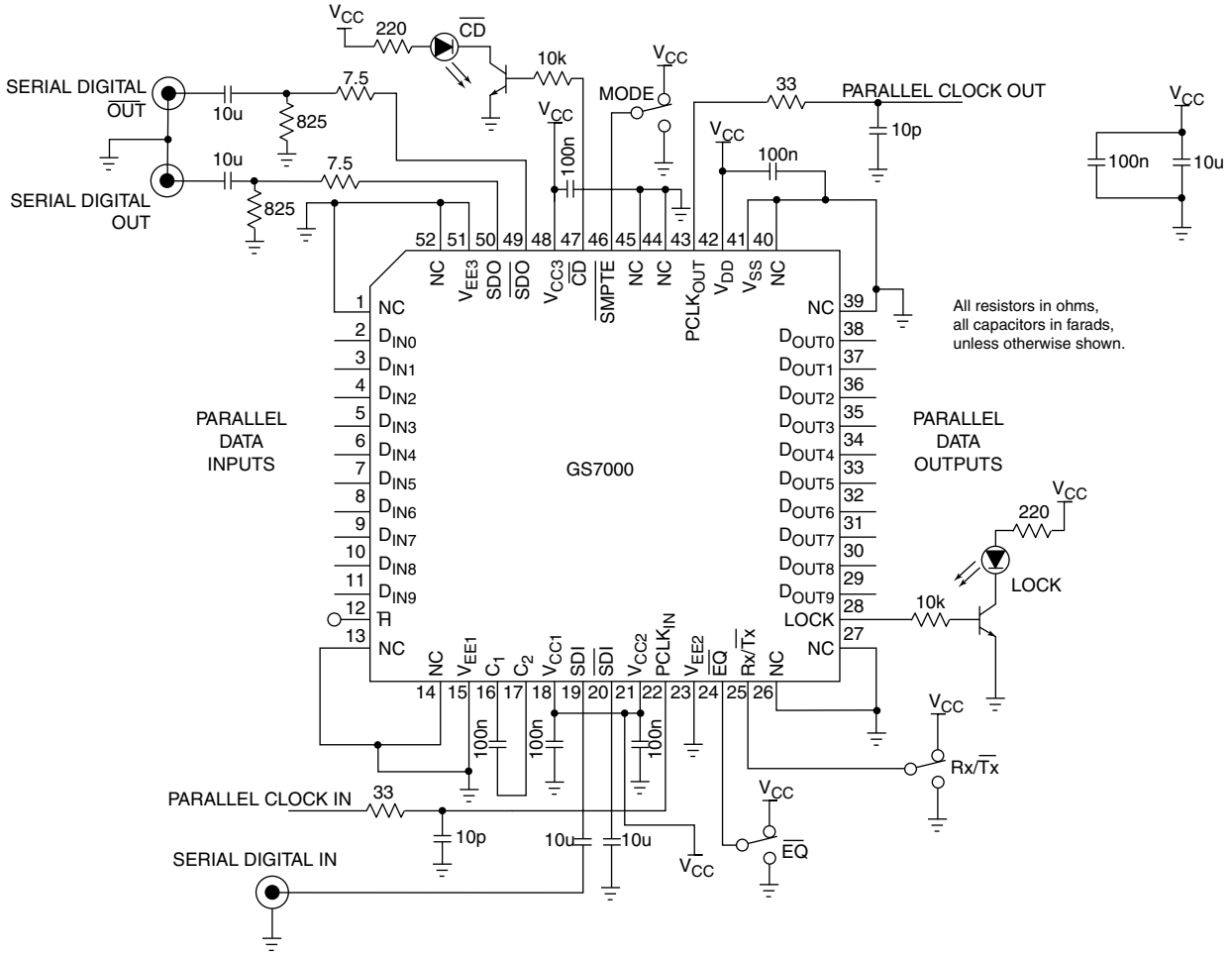
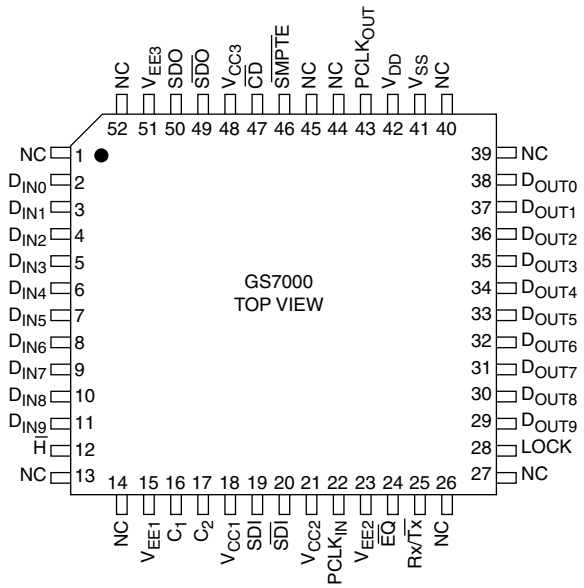


Fig. 2 Test Circuit (Half Duplex Operation)

PIN CONNECTIONS



PIN DESCRIPTIONS

NUMBER	SYMBOL	TYPE	MODE	DESCRIPTION
1, 13, 14, 26, 27, 39, 40, 44, 45, 52	NC	-	-	No Connect - Connected to Ground.
2-11	$D_{IN(0,9)}$	I	Tx	27Mb/s Parallel Data Input
12	$\overline{H}$	O	Rx	Indicates the presence of active video. Low after SAV ID and high after EAV ID
15	V_{EE1}	-	-	Most negative supply for analog circuits
16, 17	C_1, C_2	-	-	External 100nF Loop Filter Capacitor Connection
18	V_{CC1}	-	-	Most positive supply for analog circuits
19, 20	SDI, $\overline{SDI}$	I	Rx	Differential Serial Data Input
21	V_{CC2}	-	-	Most positive supply for PECL circuits
22	$PCLK_{IN}$	I	Tx	27MHz External Clock Input
23	V_{EE2}	-	-	Most negative supply for PECL circuits
24	$\overline{EQ}$	I	Rx	Equalizer control. LOW = EQ on, HIGH = EQ bypassed.
25	Rx/$\overline{Tx}$	I	-	Receiver/Transmitter Mode Control Input
28	LOCK	O	Rx/Tx	Signal Lock Indication Output. Goes HIGH approximately 38 µs after valid parallel data occurs.
29 - 38	$D_{OUT(9,0)}$	O	Rx	27Mb/s Parallel Data Output

PIN DESCRIPTIONS

NUMBER	SYMBOL	TYPE	MODE	DESCRIPTION
41	V_{SS}	-	-	Most negative supply for CMOS circuits
42	V_{DD}	-	-	Most positive supply for CMOS circuits
43	$PCLK_{OUT}$	O	Rx	27MHz Clock Output
46	$\overline{SMPTE}$	I	Rx/Tx	NRZI de/encoding and SMPTE de/scrambling control. LOW = NRZI and SMPTE mode on, HIGH = NRZI and SMPTE mode disabled.
47	$\overline{CD}$	O	Rx/Tx	Indicates loss of carrier. Low when carrier is present and high when carrier is lost.
48	V_{CC3}	-	-	Most positive supply for Analog and PECL Circuits
49, 50	SDO, $\overline{SDO}$	O	Tx	Differential Serial Data Output
51	V_{EE3}	-	-	Most negative supply for Analog and PECL Circuits

INPUT / OUTPUT CIRCUITS

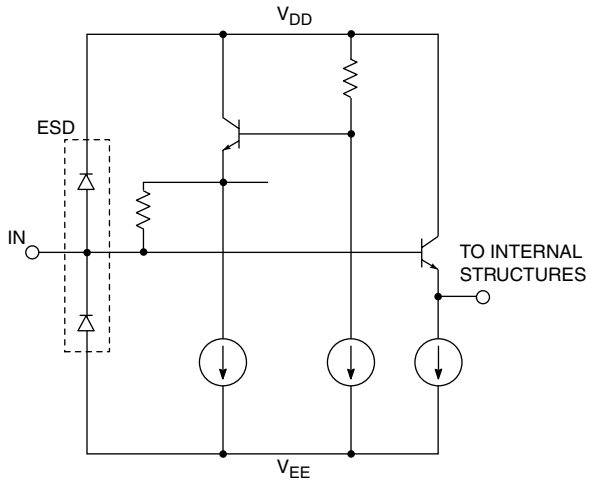


Fig. 3 SDI, $\overline{SDI}$

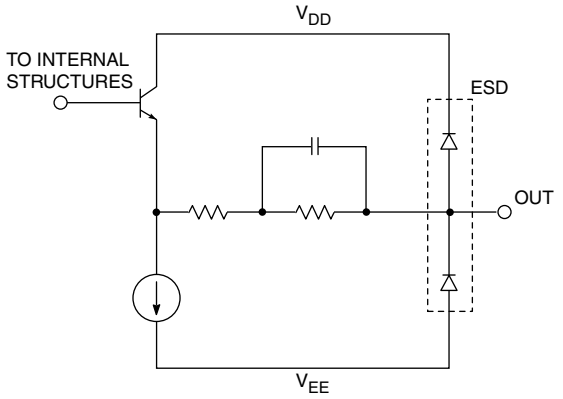


Fig. 4 SDO, $\overline{SDO}$

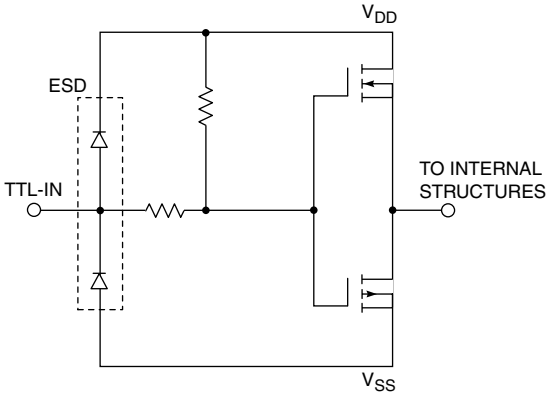


Fig. 5 $D_{IN(0,9)}$, $PCLK_{IN}$, $\overline{EQ}$, Rx/$\overline{Tx}$, $\overline{SMPTE}$

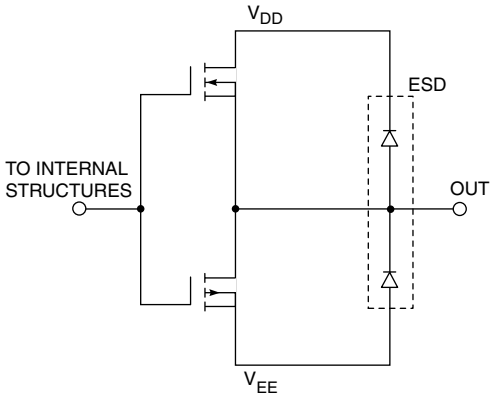


Fig. 6 $D_{OUT(0,9)}$, $\overline{H}$, LOCK, $\overline{CD}$

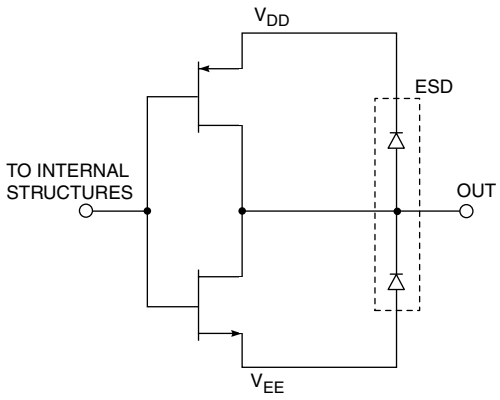


Fig. 7 $PCLK_{OUT}$

TYPICAL PERFORMANCE CURVES (V_{CC} = 5 V, T_A = 25 °C unless otherwise shown)

DATA
TO
FOLLOW

DATA
TO
FOLLOW

Fig. 8 Output PCLK Jitter vs. Cable Length

Fig. 9

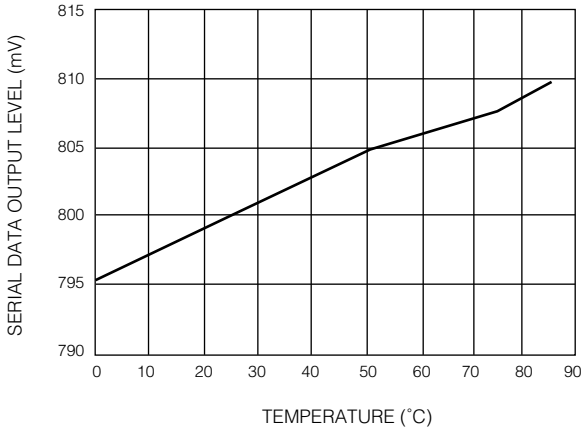


Fig. 10 Serial Data Output Level vs. Temperature

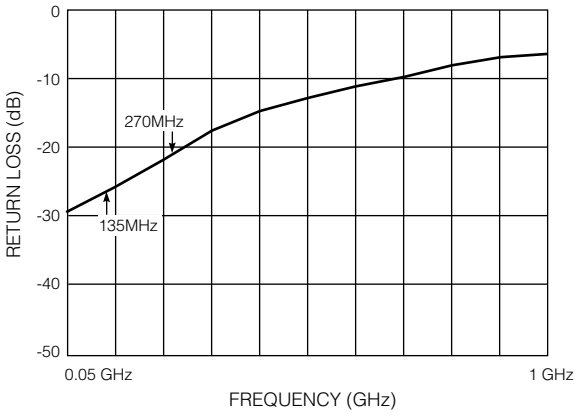


Fig. 11 Input Return Loss

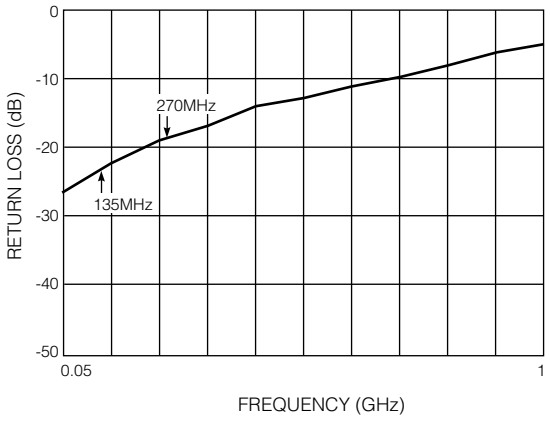


Fig. 12 Output Return Loss

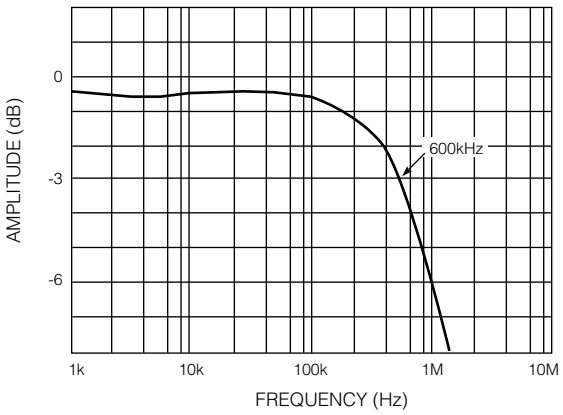


Fig. 13 Loop Bandwidth

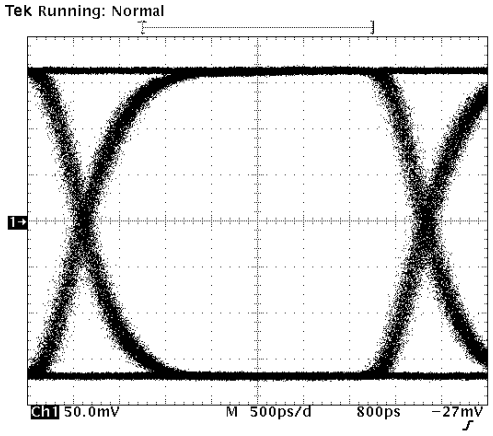


Fig. 14 Serial Data Output

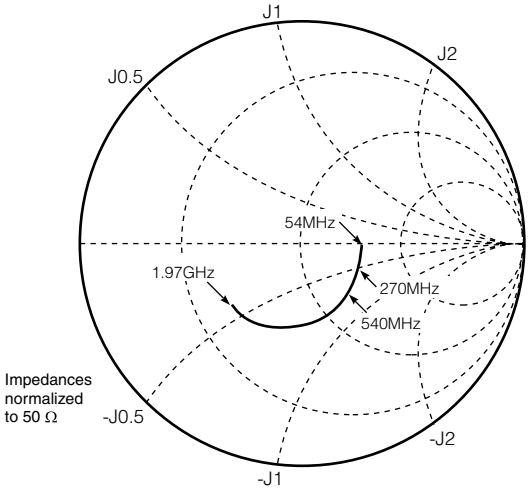


Fig. 15 Input Impedance

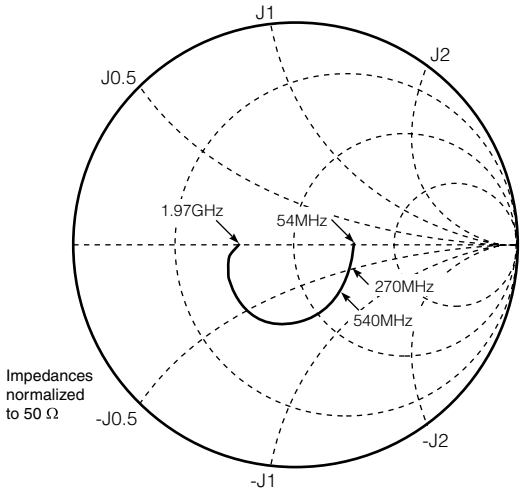


Fig. 16 Output Impedance

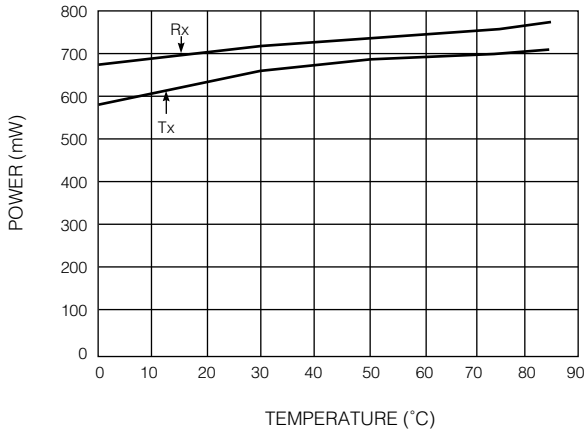


Fig. 17 Power vs. Temperature

RECEIVER OPERATION

$\overline{EQ}$	Rx/$\overline{Tx}$	$\overline{SMPTE}$	GS7000 OPERATING MODE
0	1	0	SMPTE 259M Receiver (Equalizer on, SMPTE / NRZI on)
1	1	0	SMPTE 259M Receiver with equalizer bypassed
0	1	1	Receiver function with NRZI and SMPTE Descrambler disabled, equalizer enabled.
1	1	1	Receiver function with NRZI and SMPTE Descrambler disabled, equalizer bypassed.

The diagram below depicts the active portions of the chip when operating in Receiver mode (Rx/$\overline{Tx}$ set to logic high level) with the equalizer, descrambling and NRZI functions all active. In this mode of operation the output of the LOCK pin is logic high whenever the receiver has successfully locked to the input serial bit stream. The output $\overline{H}$ is set low after the SAV ID and is set high after the EAV ID when these sequences are identified in the incoming bit stream.

Note the function available called "Equalizer Control" ($\overline{EQ}$). Setting $\overline{EQ}$ to a logic HIGH level shuts off the equalization function of the device for implementations where the length of cable to be equalized is very short (less than 10 m).

It is possible to turn off the NRZI and SMPTE Descrambler function by setting $\overline{SMPTE}$ HIGH. When operating in this mode, the output of $\overline{H}$, will be either "1" or "0" (indeterminate).

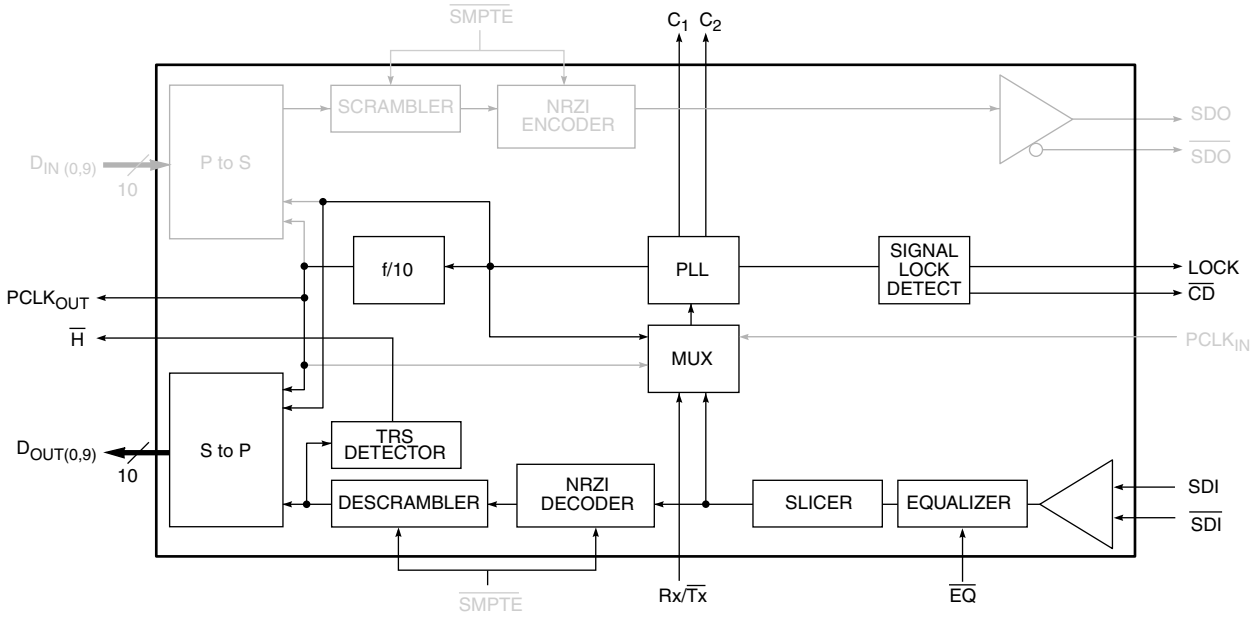


Fig. 18 Functional Block Diagram (Receiver Mode)

TRANSMITTER OPERATION

$\overline{EQ}$	Rx/$\overline{Tx}$	$\overline{SMPTE}$	GS7000 OPERATING MODE
X	0	0	SMPTE 259M Transmitter
X	0	1	Transmitter function with NRZI and SMPTE Scrambler disabled

The diagram below depicts the active portions of the chip when operating in Transmitter mode (Rx/$\overline{Tx}$ set to logic low level), with the NRZI and scrambling functions active.

Note that similar to receive mode above, it is possible to turn off the NRZI and SMPTE Scrambler by setting $\overline{SMPTE}$ high.

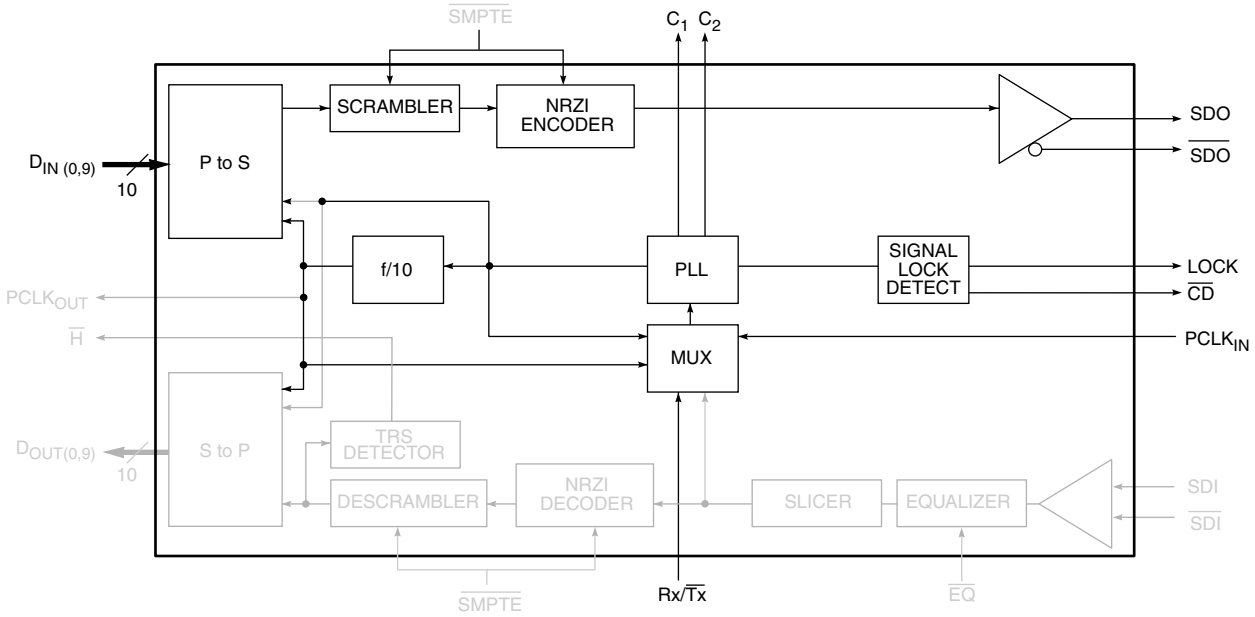


Fig. 19 Functional Block Diagram (Transmitter Mode)

DIAGRAMS

The figure below describes the timing relationship between the outputs of the GS7000 when operating in receiver mode.

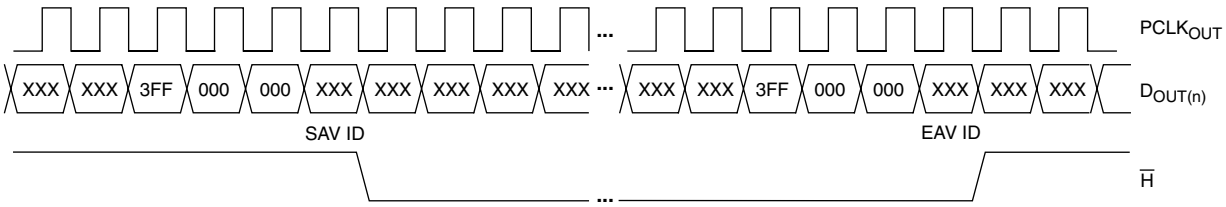


Fig. 20 Timing Diagram For Parallel Outputs, $PCLK_{OUT}$ and $\overline{H}$

The figure below describes the relationship between the output parallel clock and the output parallel data. The output parallel clock rising edge is centered on the output data within ±5 ns.

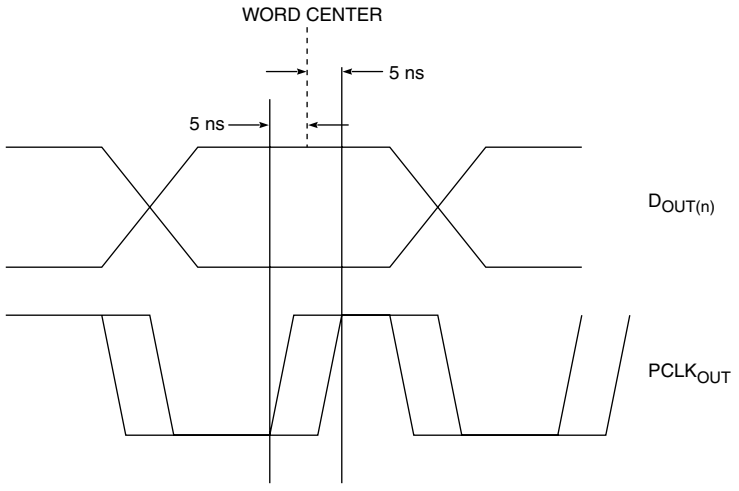


Fig. 21 Receiver Parallel Clock Alignment

The figure below describes the relationship between the input parallel clock and the input parallel data. The input parallel data must be stable for 4ns prior to the rising edge of the $PCLK_{IN}$ (setup time), and for 4 ns following the rising edge of the $PCLK_{IN}$ (hold time).

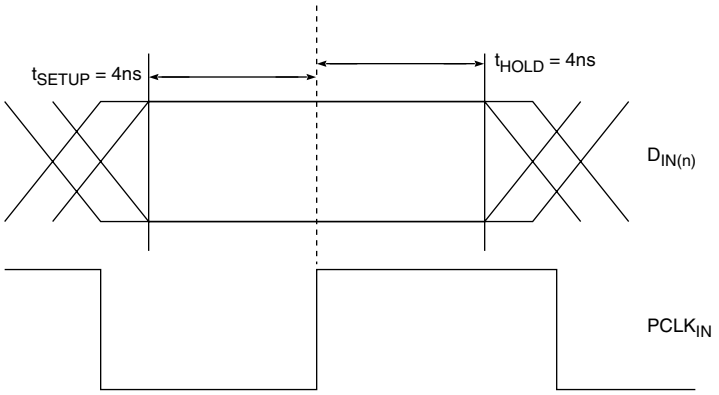
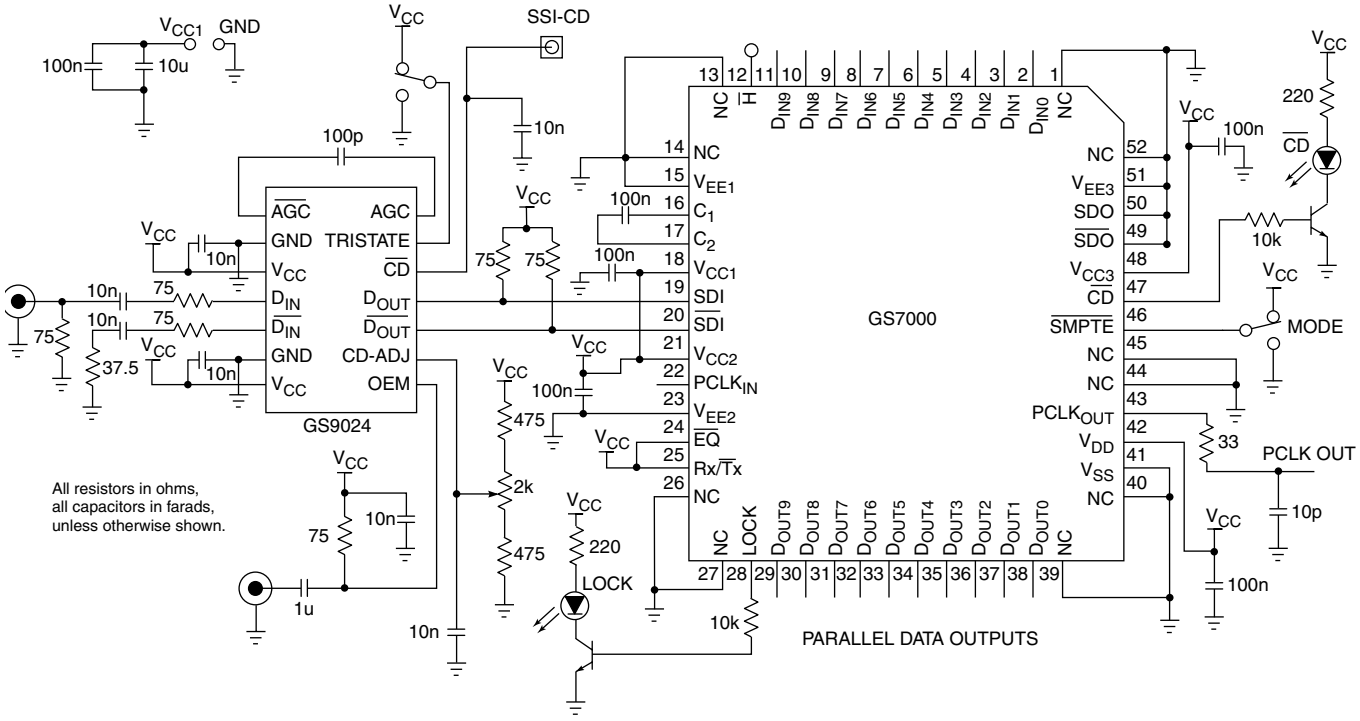
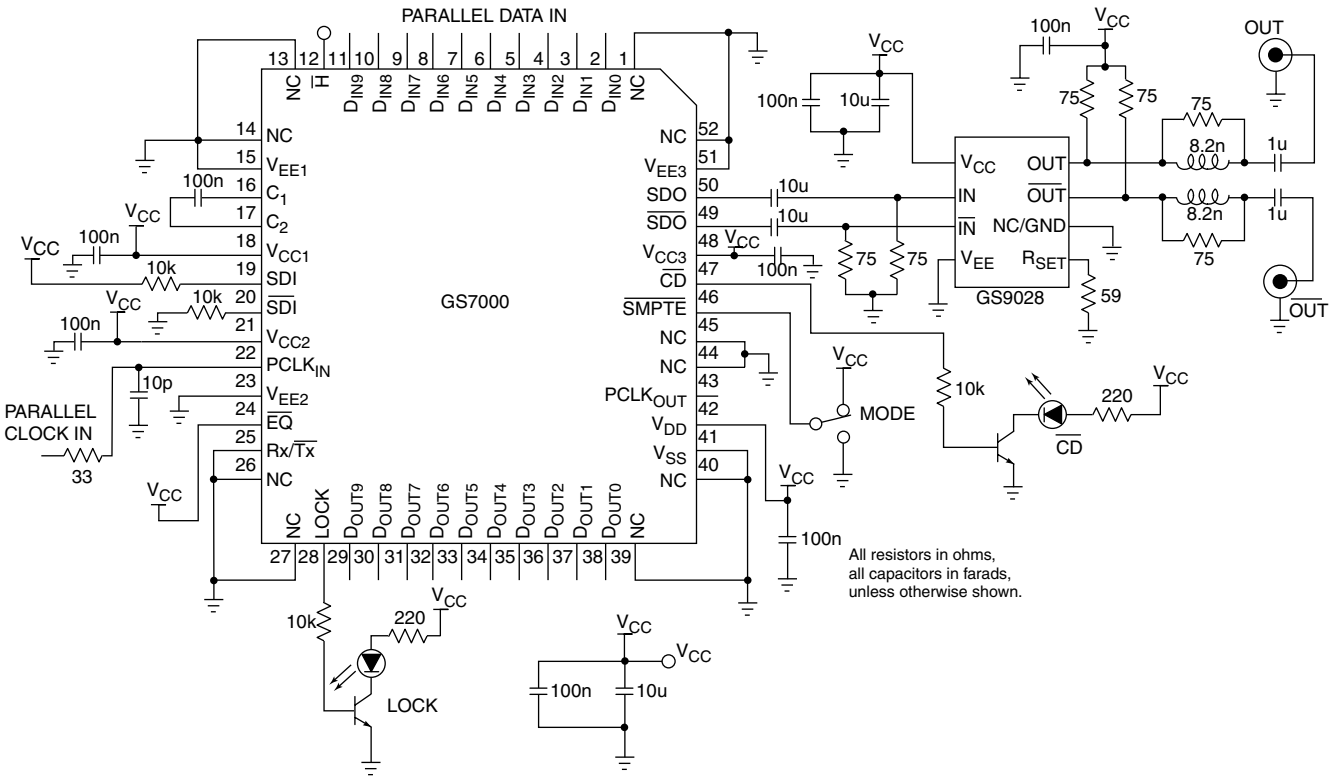


Fig. 22 Transmitter Setup and Hold Time

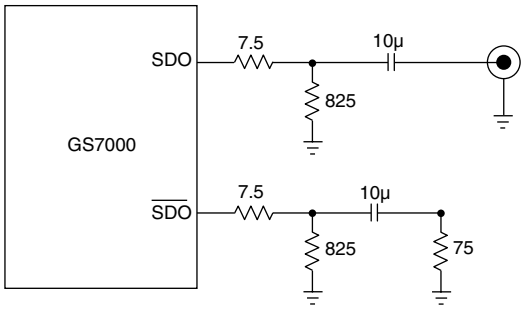
TYPICAL APPLICATION CIRCUITS



Typical Receiver Application Circuit with External Equalizer

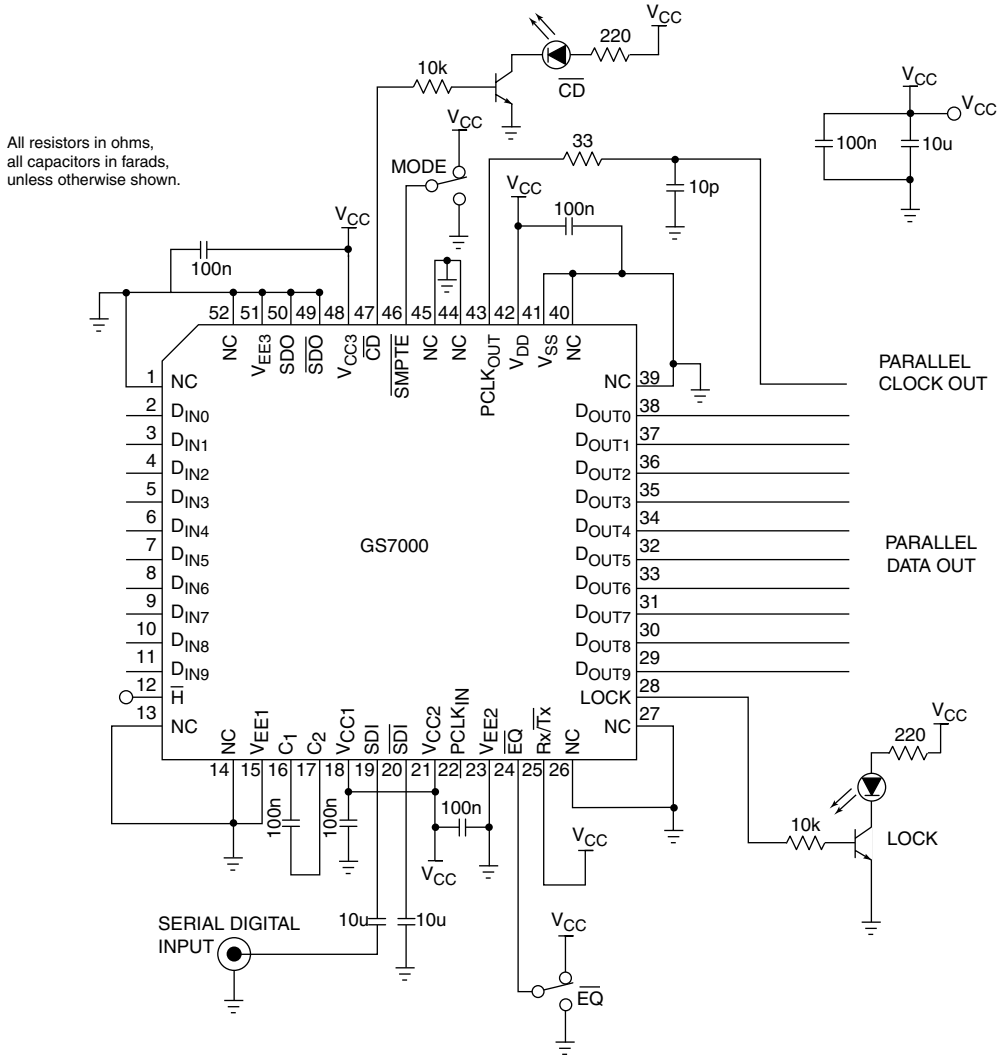


Typical Transmitter Application Circuit with Cable Driver



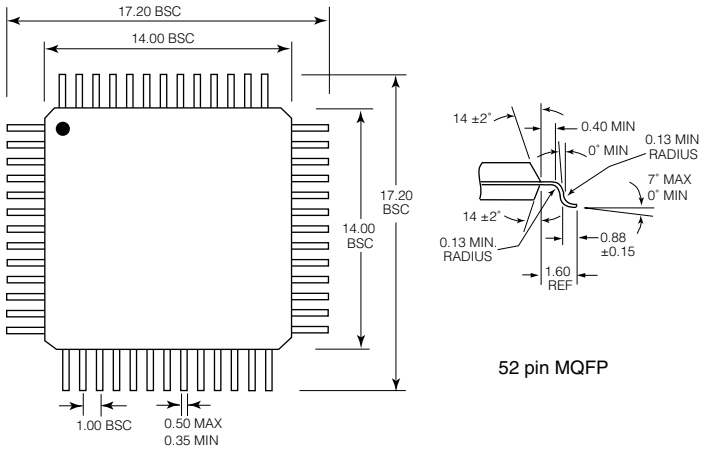
All resistors in ohms, all capacitors in farads, unless otherwise shown.

Typical Transmitter Application Circuit - Single Ended Output Operation (as above with changes shown)



Typical Receiver Application Circuit - Unbalanced Input Operation

PACKAGE DIMENSIONS



52 pin MQFP

CAUTION

ELECTROSTATIC
SENSITIVE DEVICES

DO NOT OPEN PACKAGES OR HANDLE
EXCEPT AT A STATIC-FREE WORKSTATION

DOCUMENT IDENTIFICATION

PRELIMINARY DATA SHEET
The product is in a preproduction phase and specifications are subject to change without notice.

REVISION NOTES:

Removed figure 8.

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