G-LINK Technology

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GLT44032-E

128K x 32 Embedded EDO DRAM Macro

Features

- ◆ Logical organization: 128Kx32 bits
- ◆ Physical organization: 512x256x32
- ◆ Single 3.3v ± 0.3v power supply
- ◆ 512-cycle refresh in 8 ms
- ◆ Refresh modes: $\overline{RAS}$ only, CBR, and Hidden
- ◆ Single $\overline{CAS}$ with 4 DQM for Byte Write control
- ◆ Non-multiplex row and column addresses
- ◆ Separate I/O operation
- ◆ 80/100 MHz page mode EDO cycle

General Description

The GLT44032-E 4Mbit Embedded DRAM (EmDRAM) is an asynchronous design with non-multiplexed row and column addressing scheme. $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and $\overline{OE}$ control the memory operations.

Byte Write operation is controlled by $\overline{DQM}$[0], $\overline{DQM}$[1], $\overline{DQM}$[2], and $\overline{DQM}$[3]. $\overline{DQM}$[0] going LOW will mask DI[0:7] from writing into memory; $\overline{DQM}$[1] going LOW will mask DI[8:15] from writing into memory; $\overline{DQM}$[2] going LOW will mask DI[16:23] from writing into memory; $\overline{DQM}$[3] going LOW will mask DI[24:31] from writing into memory. All output drivers, DO[0:31], will be Three-stated during a Write operation.

Performance Data

Parameter	-30	-35
Max. $\overline{RAS}$ access time, t_{RAC}	30 ns	35 ns
Max. $\overline{RAS}$ precharge time, t_{RP}	20 ns	25 ns
Max. column address access time, t_{AA}	12 ns	14 ns
Max. $\overline{CAS}$ access time, t_{CAC}	8 ns	10 ns
Min. extended data out page mode cycle time, t_{PC}	10 ns	12.5 ns
Min. read/write cycle time, t_{RC}	60 ns	70 ns

Functional Block Diagram

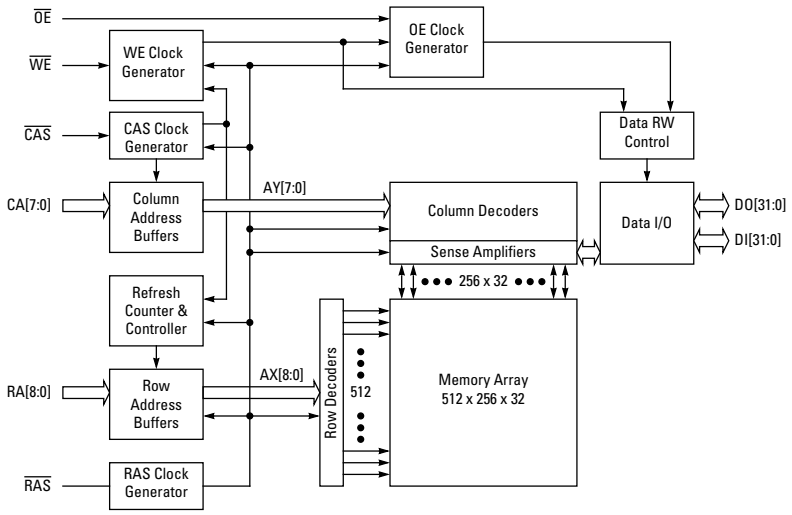

Figure 1. GLT44032-E - 128K x 32

Pin Descriptions

Symbol	Type	Description
DI[31:0]	Input	Data input.
DO[31:0]	Output	Data output.
RA[8:0]	Input	Row address.
CA[7:0]	Input	Column address.
$\overline{RAS}$	Input	Row address strobe.
$\overline{CAS}$	Input	Column address strobe.
$\overline{WE}$	Input	Write enable.
$\overline{OE}$	Input	Output enable.
$\overline{DQM}$[3:0]	I/O	Data-in mask (active low)
V_{CC} [1]	Supply	3.3v voltage supply, 4 pairs double bond minimum
V_{SS} [1]	Supply	Ground (voltage return), 4 pairs double bond minimum

1. V_{CC} and V_{SS} for the EmDRAM should be separated from the Logic portion of the chip.

Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	Address	DQM0	DQM1	DQM2	DQM3	DI[31:0]	DO[31:0]
Standby	H	H	X	X	X	X	X	X	X	X	High-Z
Read	L	L	H	L	Row/Col	X	X	X	X	X	Data Out
Write (Early)	L	L	L	X	Row/Col	H	H	H	H	Data In	High-Z
Write DI[7:0]	L	L	L	X	Row/Col	L	H	H	H	Data In	High-Z
Write DI [15:8]	L	L	L	X	Row/Col	H	L	H	H	Data In	High-Z
Write DI [23:16]	L	L	L	X	Row/Col	H	H	L	H	Data In	High-Z
Write DI [31:24]	L	L	L	X	Row/Col	H	H	H	L	Data In	High-Z
Read-Write	L	L	H→L	L→H	Row/Col	H	H	H	H	Data In	Data Out
Page-Mode Read (First Cycle)	L	H→L	H	L	Row/Col	X	X	X	X	X	Data Out
Page-Mode Read (Subsequent Cycles)		H→L	H	L	Col	X	X	X	X	X	Data Out
Page-Mode Write (First Cycle)	L	H→L	L	X	Row/Col	H	H	H	H	Data In	High-Z
Page-Mode Write (Subsequent Cycle)	L	H→L	L	X	Col	H	H	H	H	Data In	High-Z
Page-Mode R-W (First Cycle)	L	H→L	H→L	L→H	Row/Col	H	H	H	H	Data In	Data Out
Page-Mode R-W (Subsequent Cycle)	L	H→L	H→L	L→H	Col	H	H	H	H	Data In	Data Out
CBR Refresh	H→L	L	X	X	X	X	X	X	X	X	High-Z
RAS-only Refresh	L	H	X	X	Row	X	X	X	X	X	High-Z

Electrical Specifications

Absolute Maximum Ratings [1]

Parameter	Rating
Ambient Operating Temperature	0 °C to +70 °C
Storage Temperature	-50 °C to +125 °C
Voltage Relative to V_{SS}	-0.5 V to 4.5 V
Power Dissipation	0.8W

1. Operation above Absolute Maximum ratings can adversely affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Power Supply	3.0	3.3	3.6	V
V_{IH}	Input High Voltage	2	–	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	-0.5	–	–	V

Capacitance

Symbol	Description	Min	Max	Units	Notes
C_{IN}	Input Capacitance	–	2	pF	[1]
C_{IO}	Input/Output Capacitance	–	2	pF	[1]

1. Capacitance is sampled and not 100% tested

DC Characteristics (V_{CC} = 3.3V ±10%, T_A = 0 °C to +70 °C)

Symbol	Description	Conditions	-30		-35		Units
			Min	Max	Min	Max	
V_{IH}	Input High (Logic 1) Voltage		2.4	V_{CC} +1	2.4	V_{CC} +1	V
V_{IL}	Input Low (Logic 0) Voltage		-0.5	0.8	-0.5	0.8	V
V_{OH}	Output High Voltage	I_{OH} = -2.0 mA	2.4	V_{CC}	2.4	V_{CC}	V
V_{OL}	Output Low Voltage	I_{OL} = 2 mA	0	0.4	0	0.4	V
I_{CC1}	Average Power Supply Current (Operating)	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = Min.	–	200	–	180	mA
I_{CC2}	Power Supply Current (Standby)	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}	–	1	–	1	mA
I_{CC3}	Average Power Supply Current ($\overline{RAS}$-only Refresh)	$\overline{RAS}$ = cycling; $\overline{CAS}$ = V_{IH}; t_{RC} = Min.	–	200	–	180	mA
I_{CC4}	Average Power Supply Current (Fast Page Mode)	$\overline{RAS}$ = V_{IL}; $\overline{CAS}$ cycling; t_{PC} = Min.	–	120	–	100	mA
I_{CC4}	Average Power Supply Current ($\overline{CAS}$-before-$\overline{RAS}$ Refresh)	$\overline{RAS}$ = cycling; $\overline{CAS}$ before $\overline{RAS}$	–	200	–	180	mA

AC Characteristics (V_{CC} = 3.3 V ±0.3 V, T_A = 0 °C to +70 °C, C_L < 1 pF)

Symbol	Description	-30		-35		Units	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read/Write cycle time	60	–	70	–	ns	
t_{PC}	Page Mode Read/Write cycle	10	–	12.5	–	ns	
t_{OFF}	Read Data valid from $\overline{RAS}$ high	0	–	0	–	ns	
t_{DOH}	Read Data valid from next $\overline{CAS}$ low	3	–	3	–	ns	
t_{AA}	Access time from Column Address	–	12	–	14	ns	[1]
t_{RAC}	Access time from $\overline{RAS}$ low	–	30	–	35	ns	
t_{CAC}	Access time from $\overline{CAS}$ low	–	8	–	10	ns	[1]
t_{CPA}	Access time from $\overline{CAS}$ precharge	–	14	–	17	ns	[1]
t_{RAS}	$\overline{RAS}$ pulse width	30	–	35	–	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time	15	30	18	35	ns	
t_{CAS}	$\overline{CAS}$ pulse width	4	–	5	–	ns	
t_{ASR}	Row Address setup time	2	–	2	–	ns	
t_{RAH}	Row Address hold time	3	–	4	–	ns	
t_{ASC}	Column Address setup time	2	–	2	–	ns	
t_{CAH}	Column Address hold time	3	–	4	–	ns	
t_{CP}	$\overline{CAS}$ precharge time	4	–	5	–	ns	
t_{CSH}	$\overline{CAS}$ hold time from $\overline{RAS}$	30	–	35	–	ns	
t_{DS}	Write Data setup time	2	–	2	–	ns	
t_{DH}	Write Data hold time	3	–	4	–	ns	
t_{RP}	$\overline{RAS}$ precharge time	20	–	25	–	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time	5	–	10	–	ns	
t_{RSH}	$\overline{CAS}$ low to $\overline{RAS}$ high hold time	5	–	10	–	ns	
t_{RCS}	Read command setup time	3	–	5	–	ns	
t_{RCH}	Read command hold time from $\overline{CAS}$ high	3	–	5	–	ns	
t_{RRH}	Read command hold time from $\overline{RAS}$ high	3	–	5	–	ns	
t_{WCS}	Write command setup time	3	–	5	–	ns	
t_{WCH}	Write command hold time	3	–	5	–	ns	
t_{WP}	$\overline{WE}$ pulse width	8	–	10	–	ns	
t_T	Transition time (rise and fall)	–	1.0	–	1.0	ns	
t_{RWL}	Write command to $\overline{RAS}$ high	8	–	10	–	ns	
t_{CWL}	Write command to $\overline{CAS}$ high	8	–	10	–	ns	
t_{DMS}	$\overline{DQM}$ mask write setup time to $\overline{CAS}$	0	–	0	–	ns	[2]
t_{DMH}	$\overline{DQM}$ mask write hold time from $\overline{CAS}$	3	–	4	–	ns	[2]
t_{ODW}	$\overline{WE}$ control output disable	8	–	10	–	ns	

1. For better performance margin, switch column addresses and data-in on the rising edge of $\overline{CAS}$. Switch DQM on the falling edge of $\overline{CAS}$.
2. Set-up time for $\overline{DQM}$ to $\overline{CAS}$ going active (low) is 0 ns; hold-time for $\overline{DQM}$ from $\overline{CAS}$ going non-active (high) is 4 ns. $\overline{DQM}$ going low will mask the write.

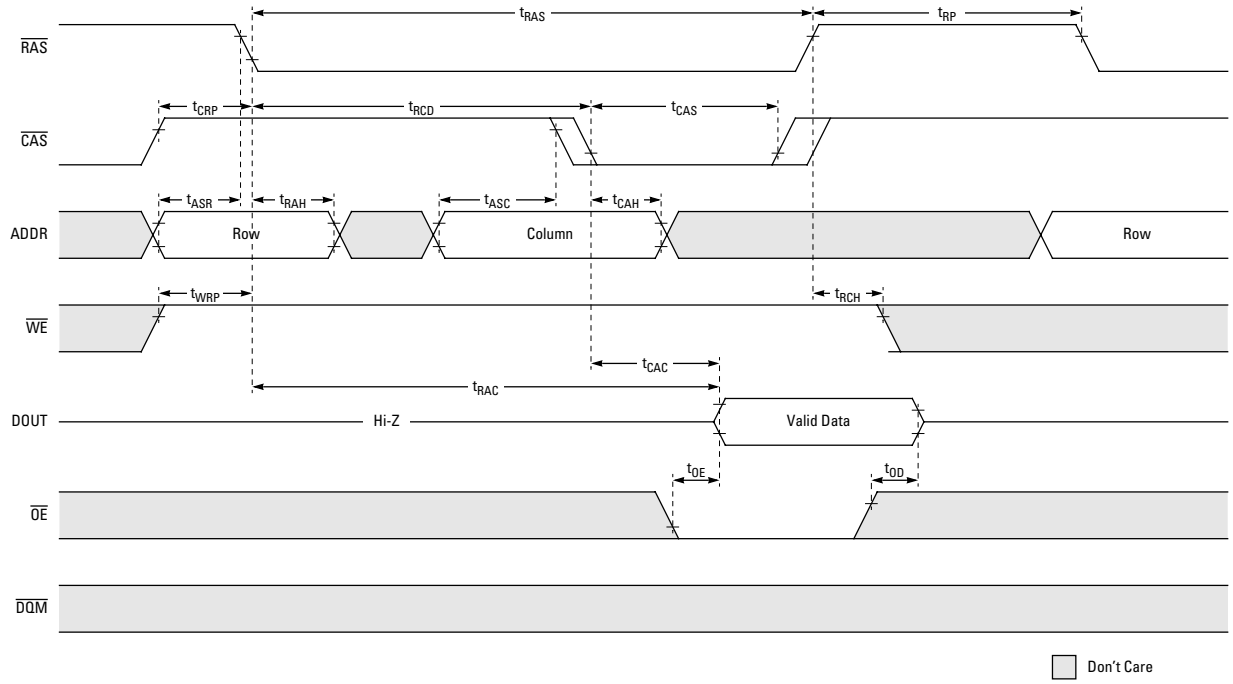

Figure 2. Read Cycle

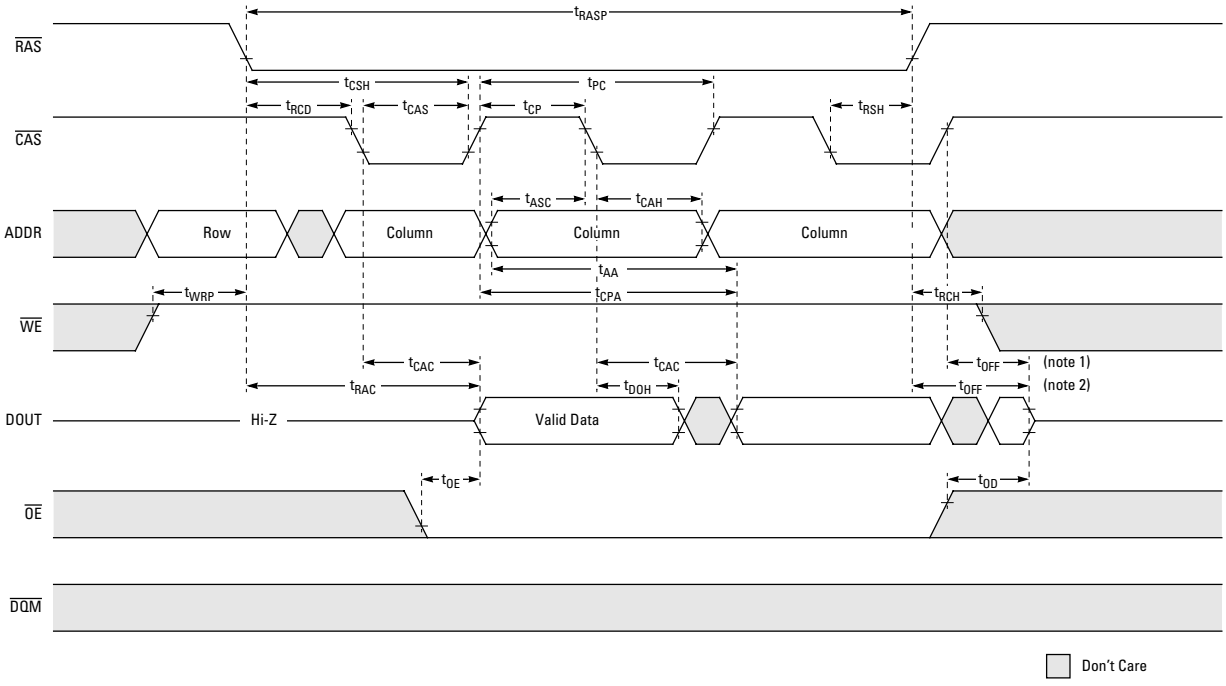

Figure 3. Page Mode Read Cycle

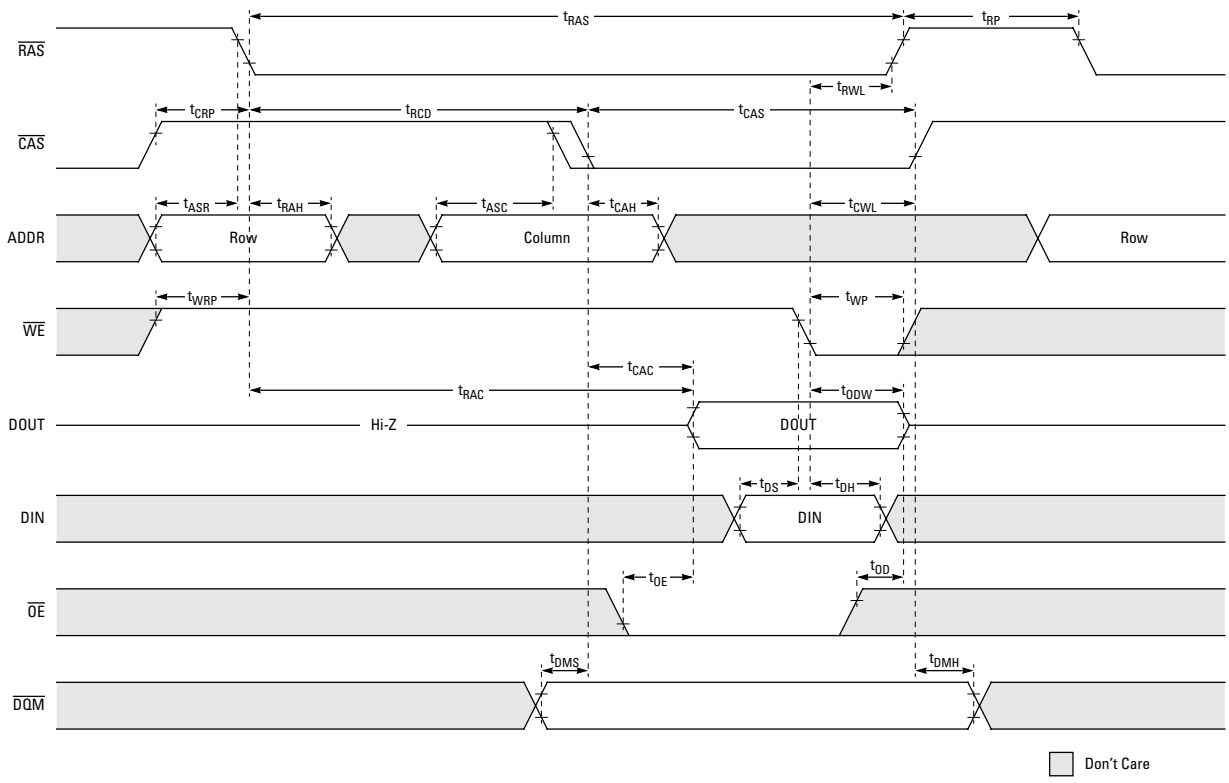

Figure 4. Read/Write Cycle

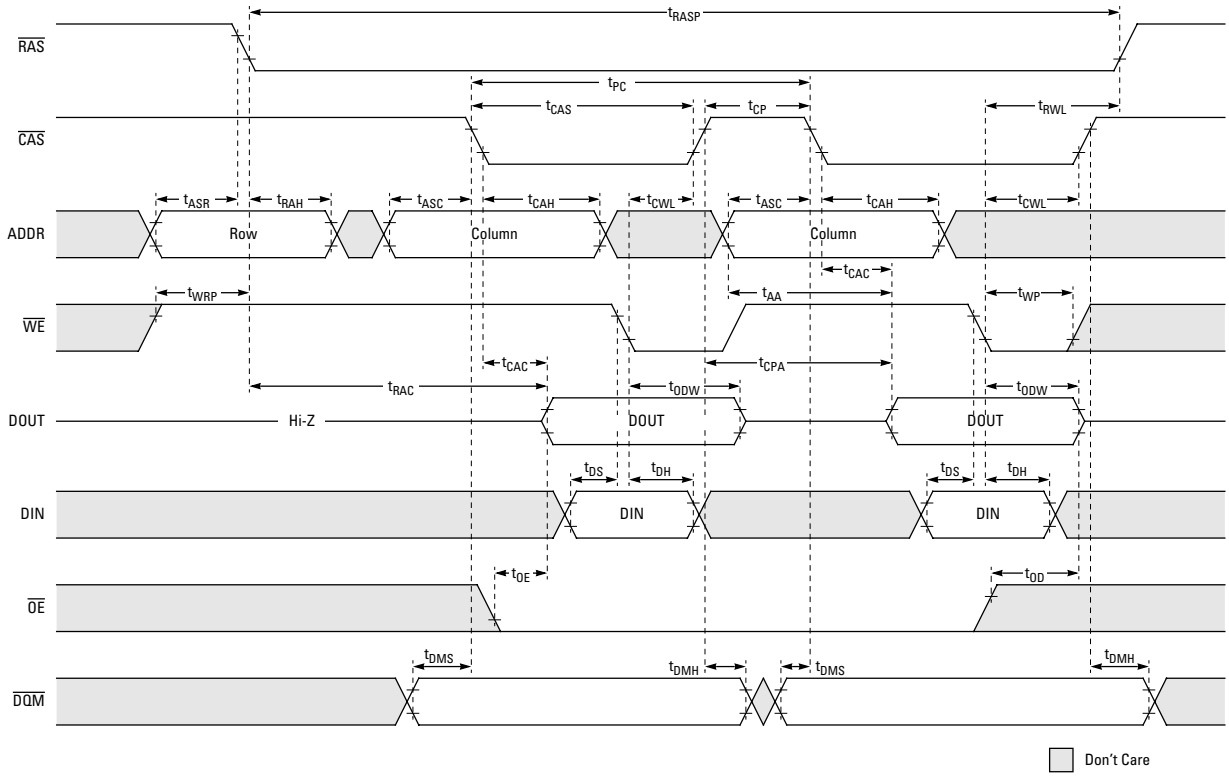

Figure 5. Page Mode Read/Write Cycle

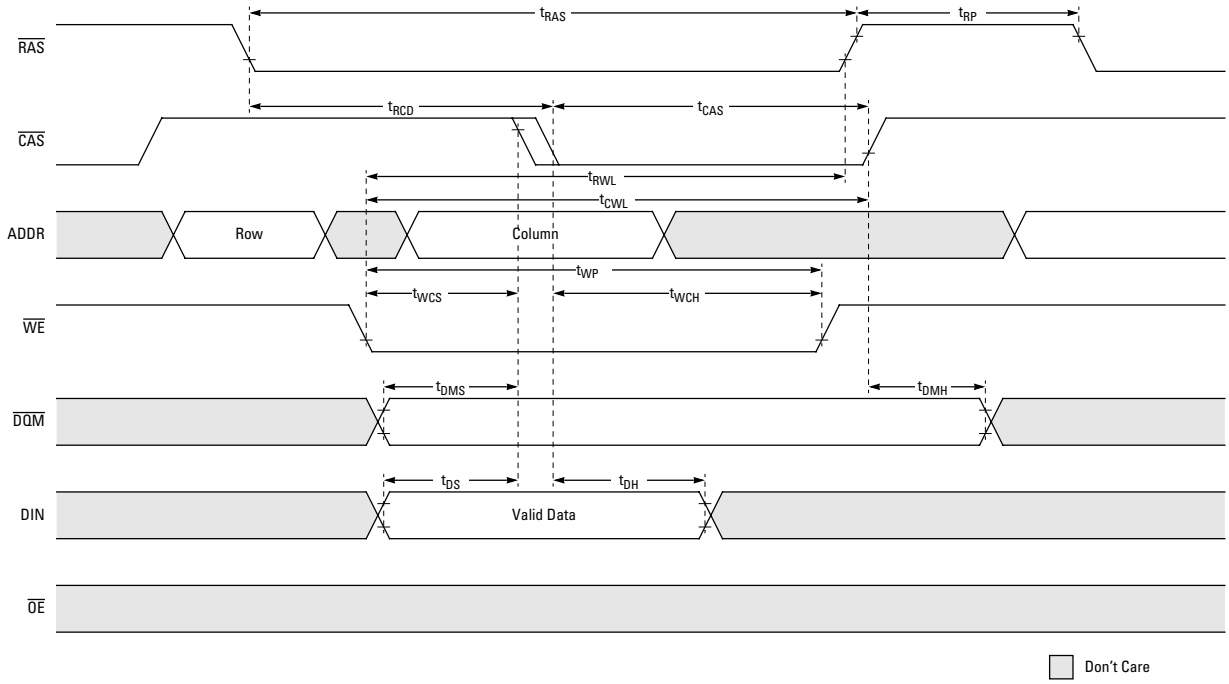

Figure 6. Early Write Cycle

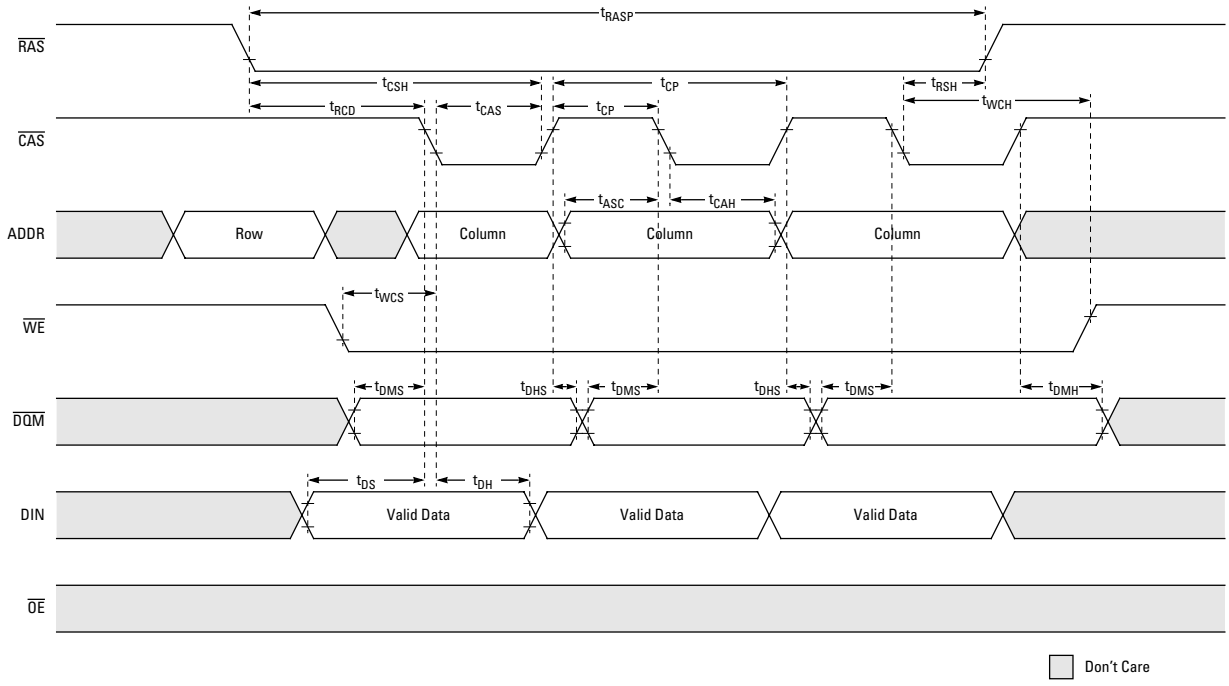

Figure 7. Page Mode Early Write Cycle

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