GLT4160L16

1M X 16 CMOS DYNAMIC RAM WITH EXTENDED DATA OUTPUT

Mar 2000 (Rev.2.0)

Features :

- 1,048,576 words by 16 bits organization.
- Fast access time and cycle time.
- Dual $\overline{CAS}$ Input.
- Low power dissipation.
- Read-Modify-Write, $\overline{RAS}$-Only Refresh, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh, Hidden Refresh and Test Mode Capability.
- 1024 refresh cycles per 16ms.
- Available in 400 mil SOJ / TSOPII Packages.
- Single 3.3V±0.3V Power Supply.
- All inputs and Outputs are TTL compatible.
- Extended Data-Out(EDO) Page Mode operation.
- Self – refresh capability. (S-Version).

Description :

The GLT4160L16 is a 1,048,576 x 16 bit high-performance CMOS dynamic random access memory. The GLT4160L16 offers Fast Page mode with Extended Data Output, and has both BYTE WRITE and WORD WRITE access cycles via two $\overline{CAS}$ pins. The GLT4160L16 has symmetric address and accepts 1024-cycle refresh in 16ms interval.

All inputs are TTL compatible. EDO Page Mode operation allows random access up to 1024 x 16 bits within a page, with cycle times as short as 13ns.

The GLT4160L16 is best suited for graphics, and DSP applications requiring high performance memories.

HIGH PERFORMANCE	35	40	50	60
Max. $\overline{RAS}$ Access Time, (t_{RAC})	35 ns	40 ns	50 ns	60 ns
Max. Column Address Access Time, (t_{CAA})	18 ns	20 ns	25 ns	30 ns
Min. Extended Data Out Page Mode Cycle Time, (t_{PC})	13 ns	15 ns	20 ns	25 ns
Min. Read/Write Cycle Time, (t_{RC})	65 ns	70 ns	85 ns	104 ns
Max. $\overline{CAS}$ Access Time (t_{CAC})	11 ns	12 ns	14 ns	15 ns

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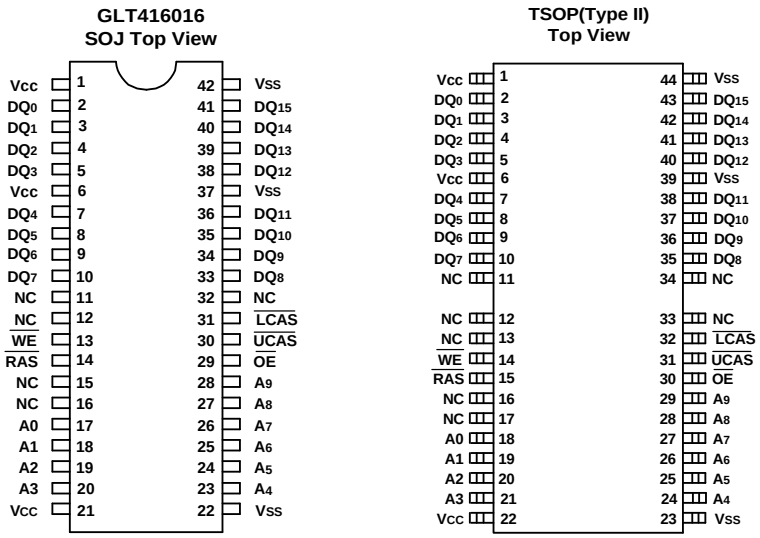
Pin Configuration :



Pin Descriptions:

Name	Function
A_0 - A_9	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Column Address Strobe/Upper Byte Control
$\overline{LCAS}$	Column Address Strobe/Lower Byte Control
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
DQ_0 - DQ_{15}	Data Inputs / Outputs
V_{CC}	+3.3V Power Supply
V_{SS}	Ground
NC	No Connection

Absolute Maximum Ratings*

Operating Temperature, T_A (ambient)
.....0°C to +70°C
Storage Temperature(plastic)....-55°C to +150°C
Voltage Relative to V_{SS}.....-1.0V to + 4.6V
Short Circuit Output Current.....50mA
Power Dissipation.....1.0W

*Note:Operation above Absolute Maximum Ratings can abversely affect device reliability.

Capacitance*

T_A=25°C, V_{CC}=3.3V±0.3V, V_{SS}=0V

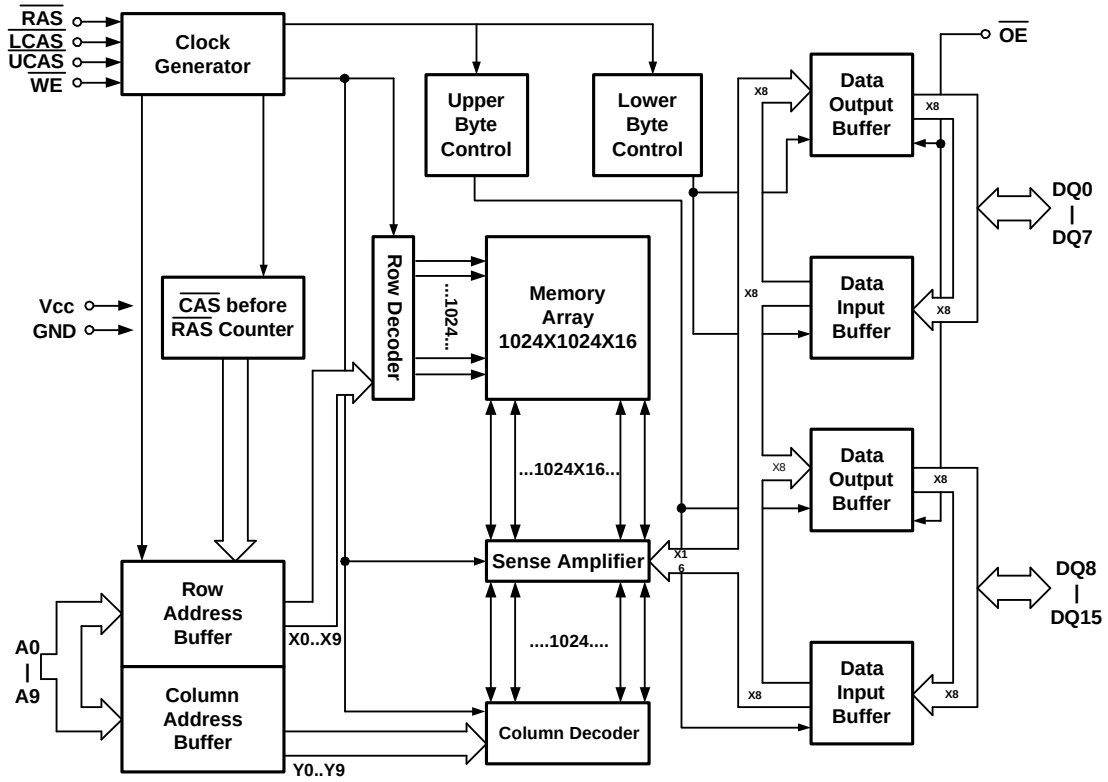
Symbol	Parameter	Max.	Unit
C_{IN1}	Address Input	5	pF
C_{IN2}	$\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, $\overline{WE}$, $\overline{OE}$	7	pF
C_{OUT}	Data Input/Output	7	pF

*Note: Capacitance is sampled and not 100% tested

Electrical Specifications

- $\overline{CAS}$ means $\overline{UCAS}$ and $\overline{LCAS}$.
- All voltages are referenced to GND.
- After power up, wait more than 100µs and then, execute eight $\overline{CAS}$-before-$\overline{RAS}$ or $\overline{RAS}$-only refresh cycles as dummy cycles to initialize internal circuit.

Block Diagram :



DC and Operating Characteristics (1-2)

T_A = 0°C to 70°C, V_{CC}=3.3V±0.3V, V_{SS}=0V, unless otherwise specified.

Sym.	Parameter	Test Conditions	Access Time	Min.	Typ	Max.	Unit	Notes
I_{LI}	Input Leakage Current (any input pin)	0V ≤ V_{IN} ≤ Vcc+0.3V (All other pins not under test=0V)		-5		+5	µA	
I_{LO}	Output Leakage Current (for High-Z State)	0V ≤ V_{out} ≤ Vcc Output is disabled (Hiz)		-5		+5	µA	
I_{CC1}	Operating Current, Random READ/WRITE	t_{RC} = t_{RC} (min.)	t_{RAC} = 35ns t_{RAC} = 40ns t_{RAC} = 50ns t_{RAC} = 60ns			170 160 150 140	mA	1,2
I_{CC2}	Standby Current,(TTL)	$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ at V_{IH} other inputs ≥V_{SS}				1	mA	
I_{CC3}	Refresh Current, $\overline{RAS}$-Only	$\overline{RAS}$ cycling, $\overline{UCAS}$, $\overline{LCAS}$ at V_{IH} t_{RC} = t_{RC} (min.)	t_{RAC} = 35ns t_{RAC} = 40ns t_{RAC} = 50ns t_{RAC} = 60ns			170 160 150 140	mA	2
I_{CC4}	Operating Current, EDO Page Mode	$\overline{RAS}$ at V_{IL}, $\overline{UCAS}$, $\overline{LCAS}$ address cycling:t_{PC}=t_{PC}(min.)	t_{RAC} = 35ns t_{RAC} = 40ns t_{RAC} = 50ns t_{RAC} = 60ns			170 160 150 140	mA	1,2
I_{CC5}	Refresh Current, $\overline{CAS}$ Before $\overline{RAS}$	$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ address cycling: t_{RC}=t_{RC} (min.)	t_{RAC} = 35ns t_{RAC} = 40ns t_{RAC} = 50ns t_{RAC} = 60ns			170 160 150 140	mA	1
I_{CC6}	Standby Current, (CMOS)	$\overline{RAS}$ ≥V_{CC}-0.2V, $\overline{UCAS}$ ≥V_{CC}-0.2V, $\overline{LCAS}$ ≥V_{CC}-0.2V, All other inputs V_{SS}				0.5 200	mA µA	1 1,5
I_{CC7}	Self Refresh Current	$\overline{RAS}$ = $\overline{UCAS}$ = $\overline{LCAS}$ =V_{IL} $\overline{WE}$ = $\overline{OE}$ =A_0~A_9=V_{CC}-0.2V or 0.2V DQ_0~DQ_{15}=V_{CC}-0.2V,0.2V or Open				200	µA	
V_{IL}	Input Low Voltage			-0.3		+0.8	V	3
V_{IH}	Input High Voltage			2.0		V_{CC}+0.3	V	3
V_{OL}	Output Low Voltage	I_{OL} = 2mA				0.4	V	
V_{OH}	Output High Voltage	I_{OH} = -2mA		2.4			V	

Notes:

1.I_{CC} is dependent on output loading when the device output is selected. Specified I_{CC}(max.) is measured with the output open.

2.I_{CC} is dependent upon the number of address transitions specified I_{CC}(max.) is measured with a maximum of one transition per address cycle in random Read/Write and EDO Fast Page Mode.

3.Specified V_{IL}(min.) is steady state operation. During transitions V_{IL}(min.) may undershoot to -1.0V for a period not to exceed 15ns. All AC parameters are measured with V_{IL}(min.)≥V_{SS} and V_{IH}(max.)≤V_{CC}.

4.Specified V_{IH}(max.) is steady state operation. During transitions V_{IH}(max.) may undershoot to +1.0V for a period not to exceed 15ns. All AC parameters are measured with V_{IL}(min.)≥V_{SS} and V_{IH}(max.)≤V_{CC}.

5.S-Version.

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AC Characteristics

T_A = 0°C to 70°C , V_{CC} = 3V ±0.3V, V_{IH} / V_{IL} = 3.0/0 V, V_{OH}/V_{OL} = 2.0/0.8V

An initial pause of 100 µs and 8 $\overline{CAS}$-before-$\overline{RAS}$ or $\overline{RAS}$-only refresh cycles are required after power-up.

		35		40		50		60			
Parameter	**Symbol**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**	**Notes**
Read or Write Cycle Time	t_{RC}	65		70		85		104		ns	
Read Modify Write Cycle Time	t_{RWC}	86		91		106		133		ns	
$\overline{RAS}$ Precharge Time	t_{RP}	25		25		30		40		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	35	100K	40	100K	50	100K	60	100k	ns	
Access Time from $\overline{RAS}$	t_{RAC}		35		40		50		60	ns	1,2,3
Access Time from $\overline{CAS}$	t_{CAC}		11		12		14		15	ns	1,5,10
Access Time from Column Address	t_{AA}		18		20		25		30	ns	1,5,6
$\overline{CAS}$ to Output Low-Z	t_{CLZ}	0		0		0		0		ns	
$\overline{CAS}$ to Output High-Z	t_{CEZ}	3	8	3	8	3	8	3	10	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	12		12		14		13		ns	
$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	t_{ROH}	8		8		9		10		ns	
$\overline{CAS}$ Hold Time	t_{CSH}	30		34		45		40		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	6	10k	6	10k	8	10k	12	10k	ns	
$\overline{RAS}$ to CAS Delay Time	t_{RCD}	17	24	18	28	19	37	18	45	ns	
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	12	17	13	20	14	25	13	30	ns	7
$\overline{CAS}$ to RAS Precharge Time	t_{CRP}	5		5		5		5		ns	
Row Address Set-Up Time	t_{ASR}	0		0		0		0		ns	
Row Address Hold Time	t_{RAH}	7		8		9		10		ns	
Column Address Set-Up Time	t_{ASC}	0		0		0		0		ns	
Column Address Hold Time	t_{CAH}	6		6		7		10		ns	
Column Address to RAS Lead Time	t_{RAL}	18		20		25		30		ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{AR}	30		34		44		55		ns	
Read Command Set-Up Time	t_{RCS}	0		0		0		0		ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	4
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0		0		0		0		ns	4
Write Command Set-Up Time	t_{WCS}	0		0		0		0		ns	8,9
Write Command Hold Time	t_{WCH}	6		6		6		10		ns	
Write Command Pulse Width	t_{WP}	6		6		6		10		ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	11		12		13		13		ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	11		12		13		13		ns	

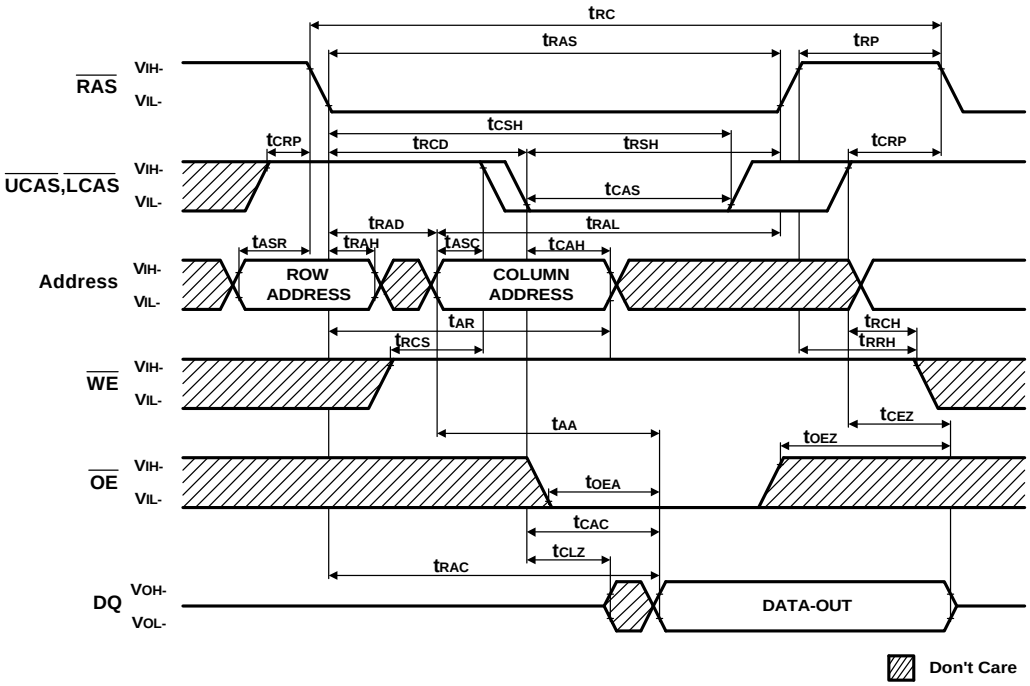
AC Characteristics

Parameter	Symbol	35		40		50		60		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Data Set-Up Time	t_{DS}	0		0		0		0		ns	
Data Hold Time	t_{DH}	7		7		8		10		ns	
Data Hold Time Referenced to $\overline{RAS}$	t_{DHR}	31		36		46		55		ns	
$\overline{RAS}$ to $\overline{WE}$ E Delay Time	t_{RWD}	49		54		64		79		ns	
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	23		24		25		32		ns	
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	30		32		37		47		ns	
$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	t_{RPC}	0		0		0		0		ns	
Access Time from $\overline{CAS}$ Precharge	t_{CPA}		20		22		30		32	ns	
EDO Page Mode Cycle Time	t_{PC}	13		15		20		25		ns	
EDO Page Mode Read-Modify-Write Cycle Time	t_{PRWC}	47		50		59		63		ns	
$\overline{CAS}$ Precharge Time (EDO Page Mode)	t_{CP}	5		5		8		15		ns	
$\overline{RAS}$ Pulse Width (EDO Page Mode Only)	t_{RASP}	35	100K	40	100K	50	100K	60	100k	ns	
Access Time from $\overline{OE}$	t_{OEA}		11		12		14		15	ns	
$\overline{OE}$ to Data Delay Time	t_{OED}	8		8		8		13		ns	
$\overline{OE}$ to Output High-Z	t_{OEZ}	3	8	3	8	3	8	3	8	ns	
$\overline{OE}$ Command Hold Time	t_{OEH}	6		7		7		0		ns	
Data Output Hold after $\overline{CAS}$ low	t_{DOH}	3		3		5		5		ns	
$\overline{RAS}$ to Output High-Z	t_{REZ}	3	8	3	8	3	8	3	8	ns	
$\overline{WE}$ to Output High-Z	t_{WEZ}	3	10	3	10	3	12	3	12	ns	
$\overline{OE}$ to $\overline{CAS}$ Hold Time	t_{OCH}	8		8		8		5		ns	
$\overline{CAS}$ Hold Time to $\overline{OE}$	t_{CHO}	8		8		8		5		ns	
$\overline{OE}$ Precharge Time	t_{OEP}	8		8		8		5		ns	
$\overline{CAS}$ Set-Up Time for $\overline{CAS}$-before-$\overline{RAS}$ Cycle	t_{CSR}	10		10		10		10		ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$-before-$\overline{RAS}$ Cycle	t_{CHR}	8		8		10		10		ns	
Transition Time	t_T	1.5	50	1.5	50	2	50	2	50	ns	
Refresh Period	t_{REF}		16		16		16		16	ms	
$\overline{RAS}$ pulse width ($\overline{CAS}$-before-$\overline{RAS}$ Self refresh)	t_{RASS}	100		100		100		100		µs	
$\overline{RAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ Self refresh)	t_{RPS}	60		70		90		110		ns	
$\overline{CAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ Self refresh)	t_{CHS}	-50		-50		-50		-50		ns	

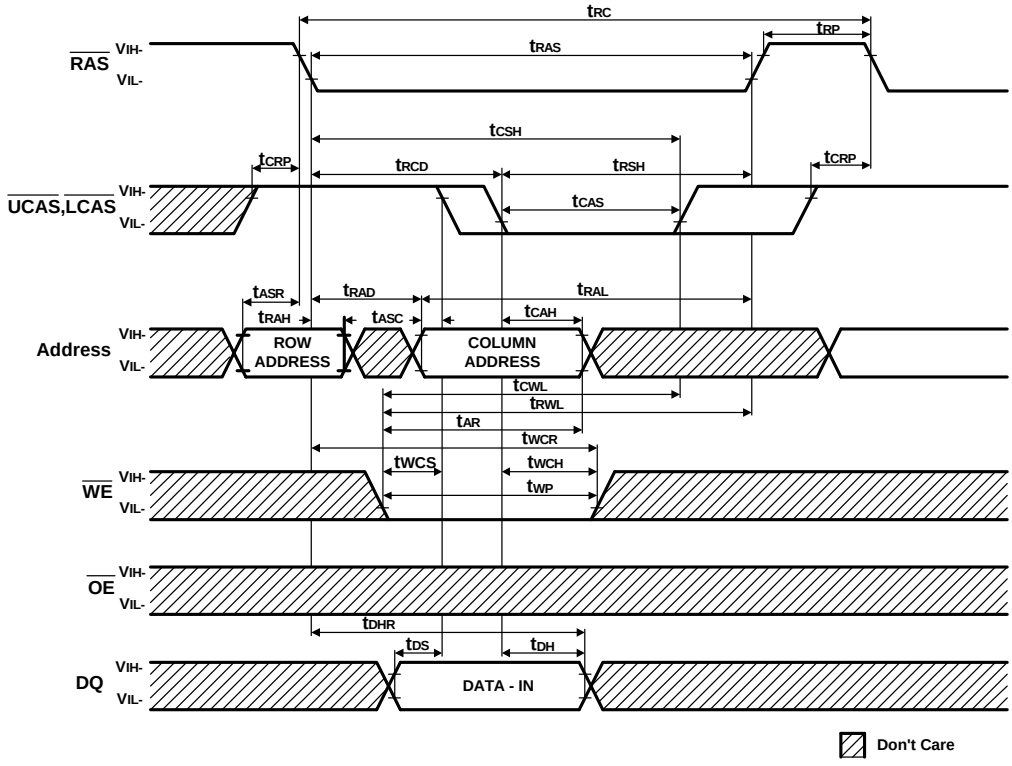
Notes:

1. Measure with a load equivalent to one TTL inputs and 50 pF.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.), access time will be t_{AA} dominant.
3. Assumes that $t_{RAD} \leq t_{RAD}$ (max.). If t_{RAD} is greater than t_{RCD} (max.), access time will be controlled by t_{CAC}.
4. Either t_{RRH} or t_{RCH} must be satisfied for a Read Cycle.
5. Access time is determined by the longest of t_{CAA}, t_{CAC} and t_{CPA}.
6. Assumes that $t_{RAD} \geq t_{RAD}$ (max.).
7. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, the access time is controlled by t_{CAA} and t_{CAC}.
8. t_{WCS}, t_{RWD}, t_{AWD} and t_{CWD} are not restrictive operating parameters.
9. t_{WCS} (min.) must be satisfied in an Early Write Cycle.
10. t_{DS} and t_{DH} are referenced to the latter occurrence of $\overline{CAS}$ of $\overline{WE}$.
11. t_T is measured between V_{IH} (min.) and V_{IL} (max.). AC-measurements assume t_T = 1.5 ns.

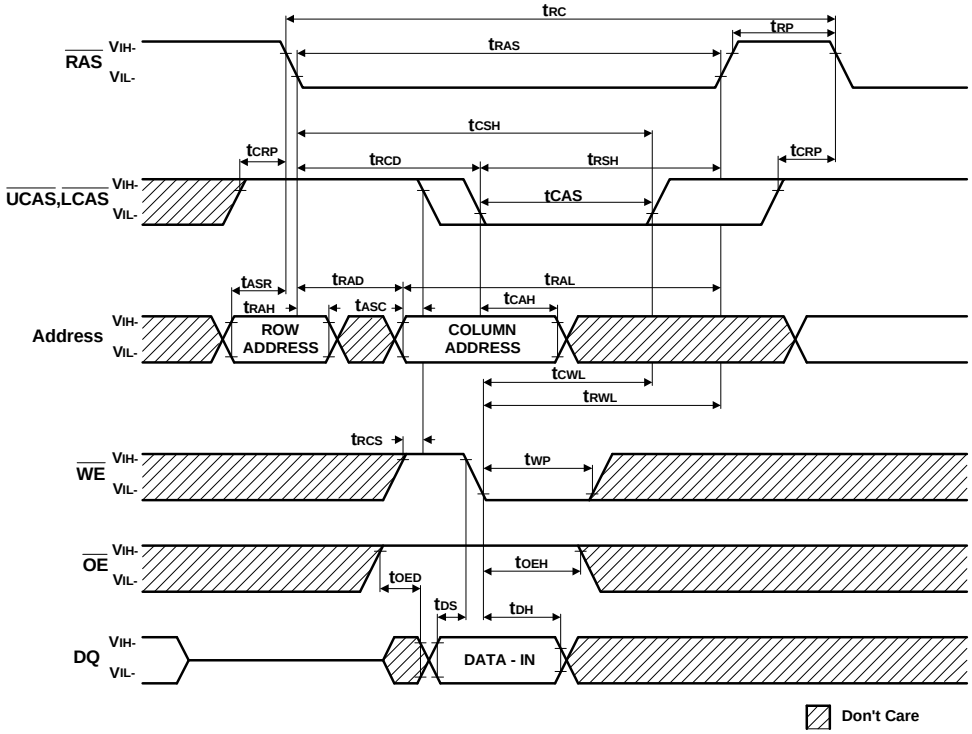
Read CYCLE Note : D_{IN} = OPEN



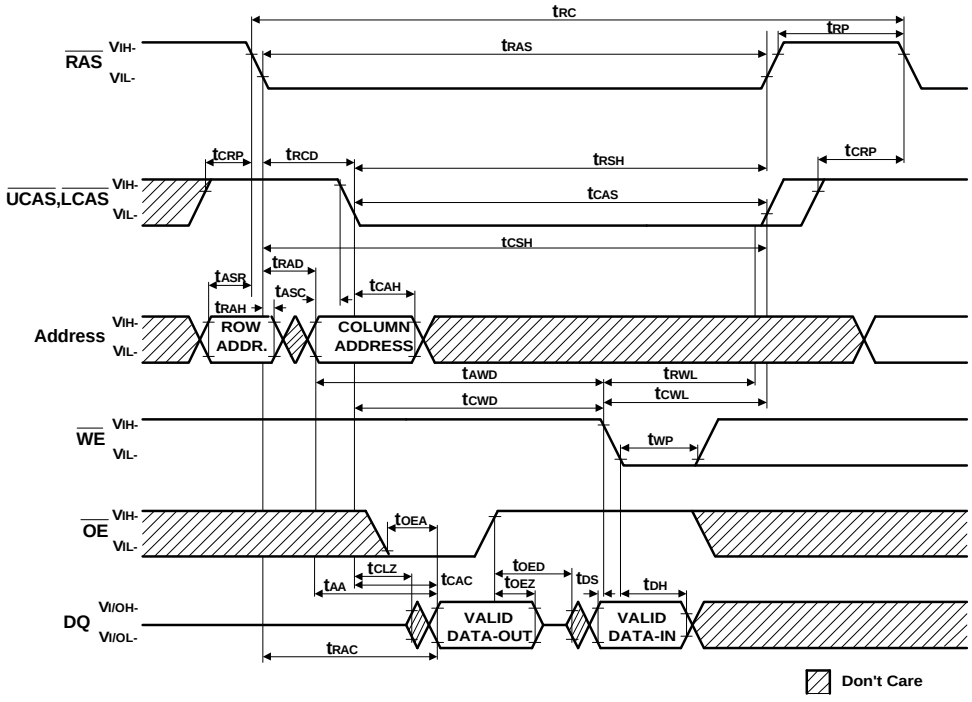
Early Write Cycle NOTE : D_{OUT} = OPEN



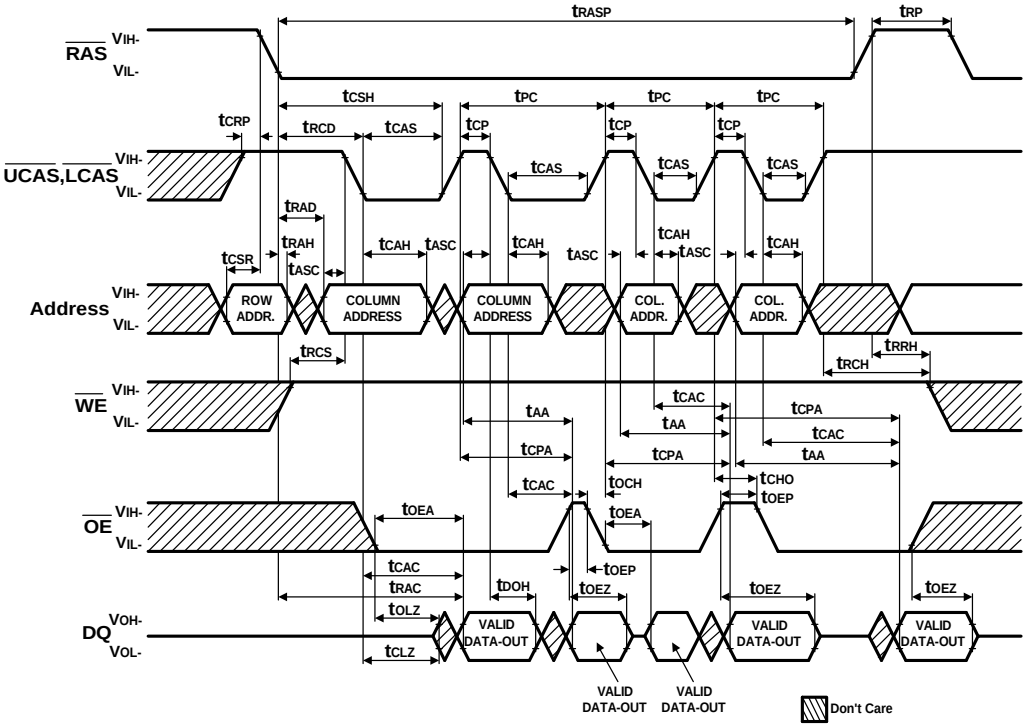
$\overline{OE}$ Controlled Write Cycle NOTE : D_{OUT} = OPEN



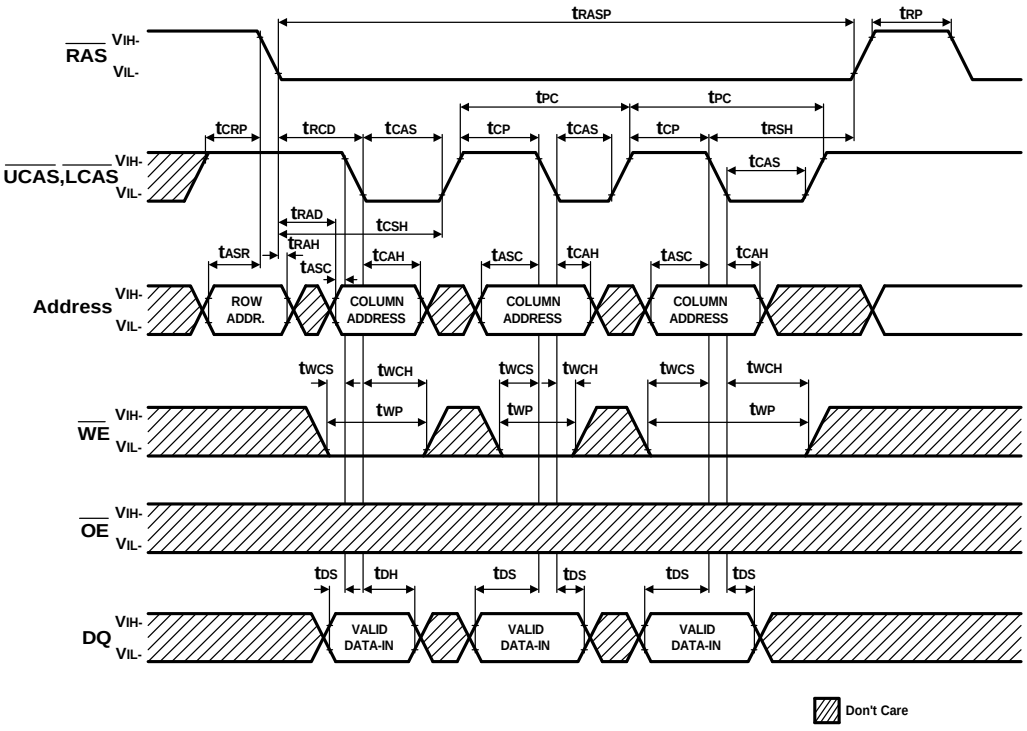
Read - Modify - Write Cycle



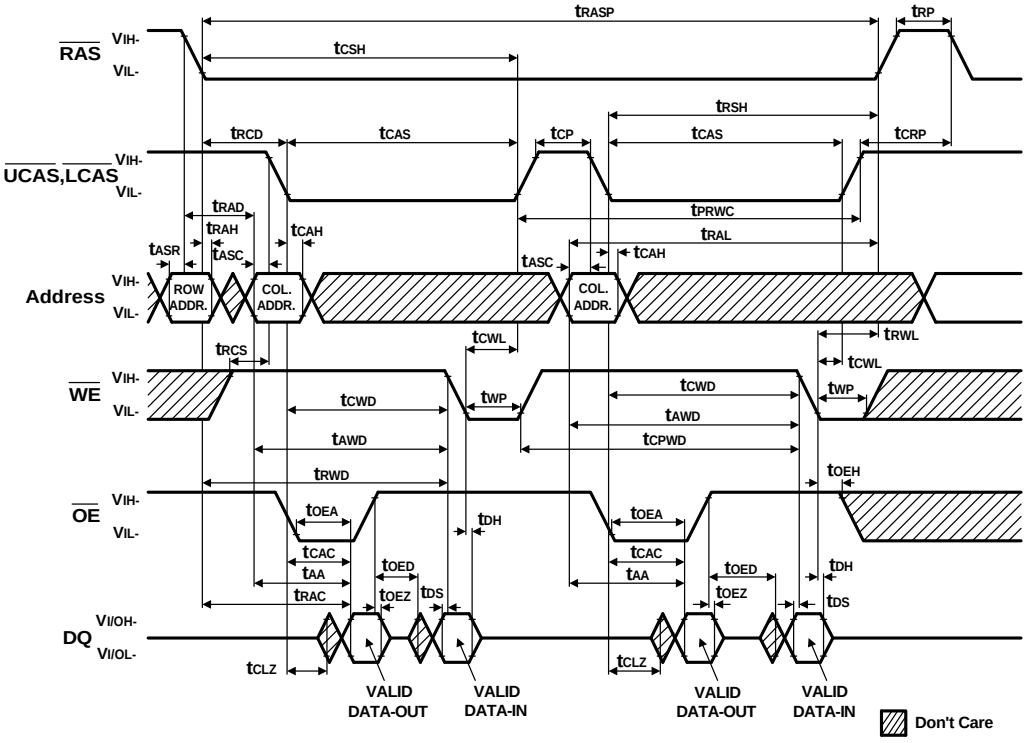
EDO Page Mode Read Cycle



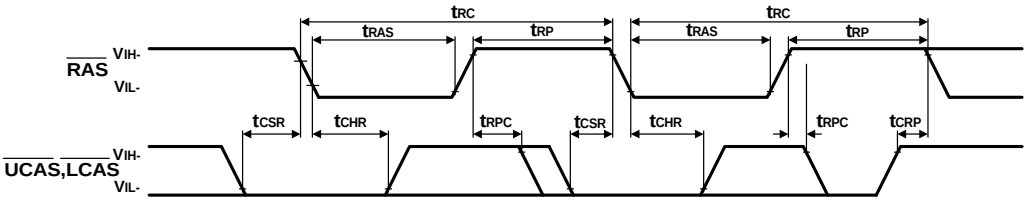
EDO Page Mode Early Write Cycle NOTE : D_{OUT} = OPEN



EDO Page Mode Read - Modify - Write Cycle

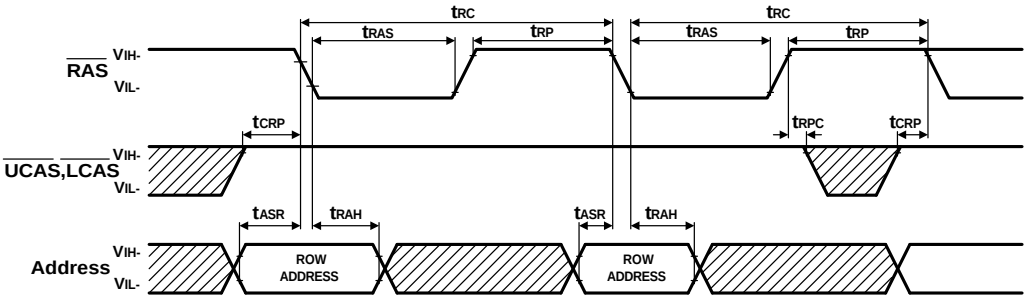


$\overline{\text{CAS}}$ - Before - $\overline{\text{RAS}}$ Refresh Cycle



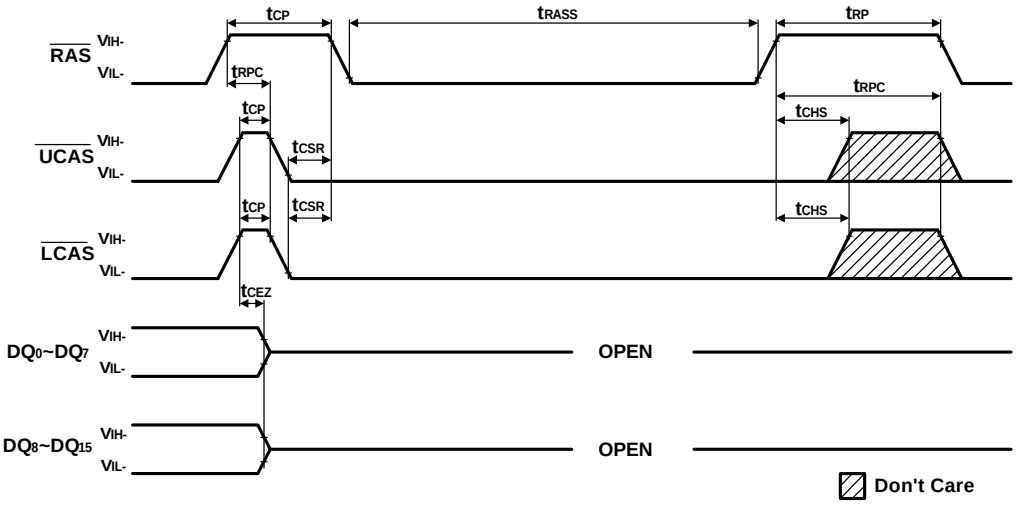
Remark Address, $\overline{\text{WE}}$, $\overline{\text{OE}}$: Don't care DQ : Hi-Z

$\overline{\text{RAS}}$ -Only Refresh Cycle



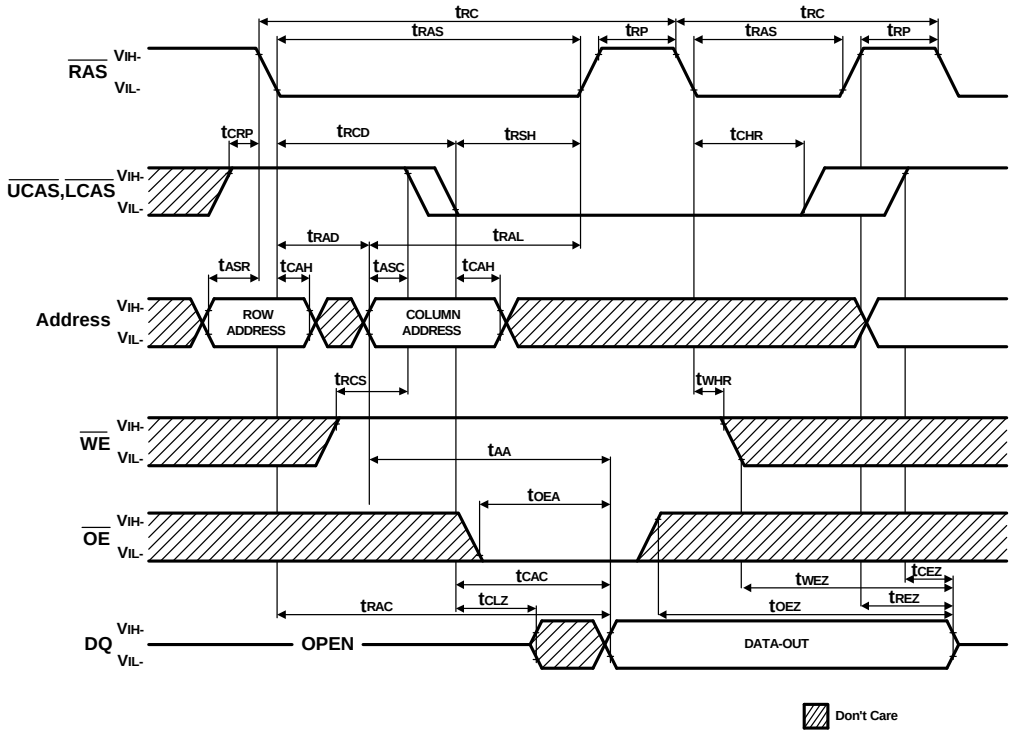
Remark $\overline{\text{WE}}$, $\overline{\text{OE}}$: Don't care DQ : Hi-Z

$\overline{CAS}$ - Before - $\overline{RAS}$ Self Refresh Cycle

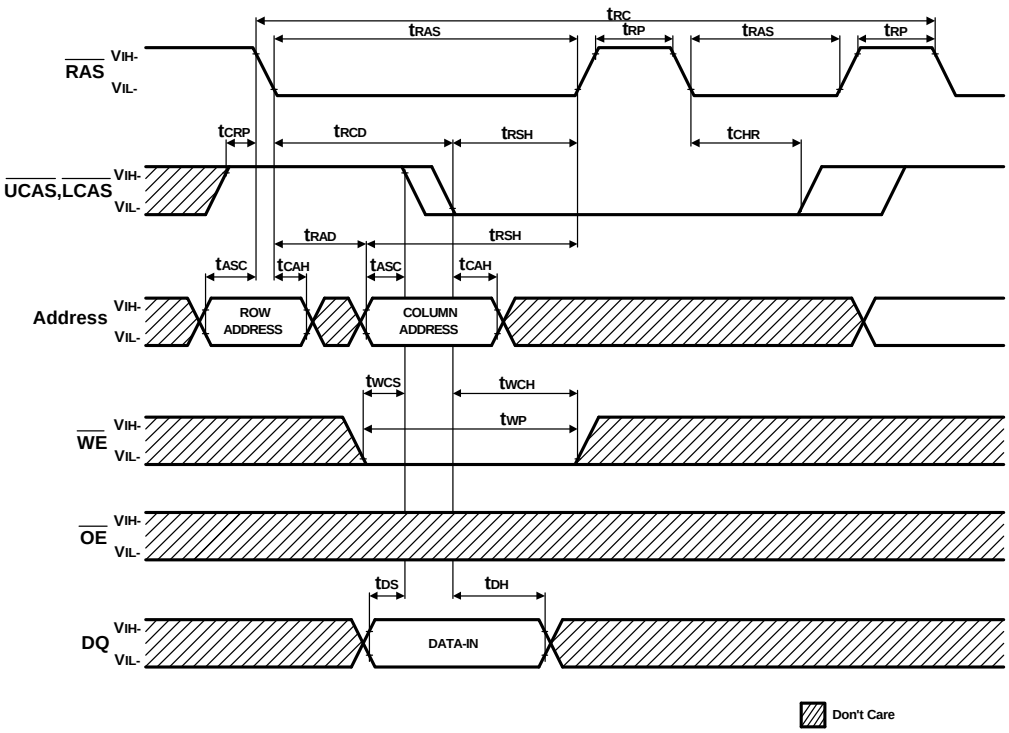


NOTE : $\overline{WE}$, $\overline{OE}$,Address = Don't care.

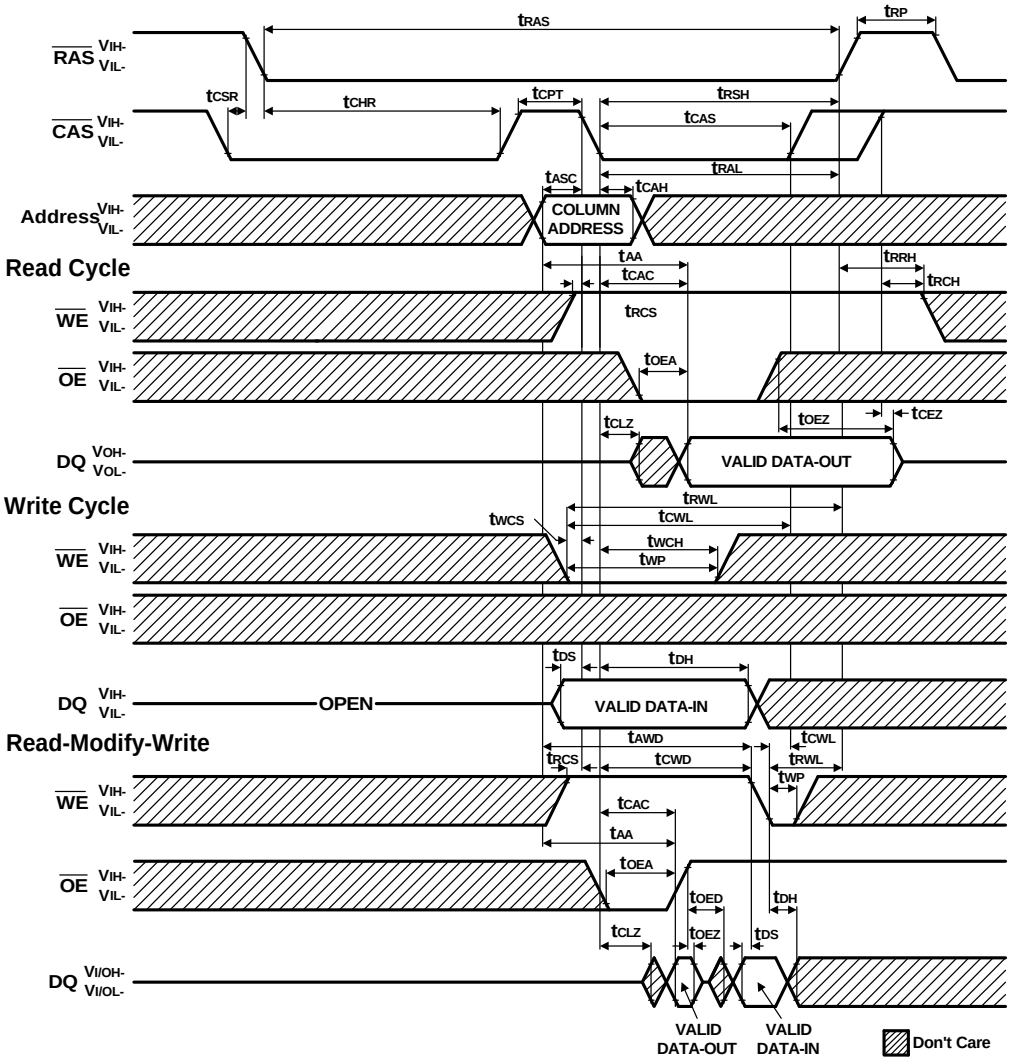
Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Write) NOTE : D_{OUT} = OPEN



$\overline{CAS}$ –Before- $\overline{RAS}$ Refresh Counter Test Cycle



Ordering Information

Part Number	*SPEED*	*POWER*	*FEATURE*	*PACKAGE*
GLT4160L16-35J4	**35ns**	**Normal**	**EDO**	**42L 400mil SOJ**
GLT4160L16-40J4	**40ns**	**Normal**	**EDO**	**42L 400mil SOJ**
GLT4160L16-50J4	**50ns**	**Normal**	**EDO**	**42L 400mil SOJ**
GLT4160L16-60J4	**60ns**	**Normal**	**EDO**	**42L 400mil SOJ**
GLT4160L16-35TC	**35ns**	**Normal**	**EDO**	**44/50L 400mil TSOPII**
GLT4160L16-40TC	**40ns**	**Normal**	**EDO**	**44/50L 400mil TSOPII**
GLT4160L16-50TC	**50ns**	**Normal**	**EDO**	**44/50L 400mil TSOPII**
GLT4160L16-60TC	**60ns**	**Normal**	**EDO**	**44/50L 400mil TSOPII**

Parts Numbers (Top Mark) Definition :

GLT 4 160 L 16 - 40 J4

4 : DRAM
6 : Standard SRAM
7 : Cache SRAM
8 : Synchronous Burst SRAM

-SRAM
064 : 8K
256 : 256K
512 : 512K
100 : 1M
-DRAM
10 : 1M(C/EDO)*
11 : 1M(C/FPM)*
12 : 1M(H/EDO)*
13 : 1M(H/FPM)*
20 : 2M(EDO)
21 : 2M(FPM)
40 : 4M(EDO)
41 : 4M(FPM)
80 : 8M(EDO)
81 : 8M(FPM)
160 : 16M(EDO)
161 : 16M(FPM)
*See note

VOLTAGE
Blank : 5V
L : 3.3V
M : 2.5V
N : 2.1V

CONFIG.
04 : x04
08 : x08
16 : x16
32 : x32

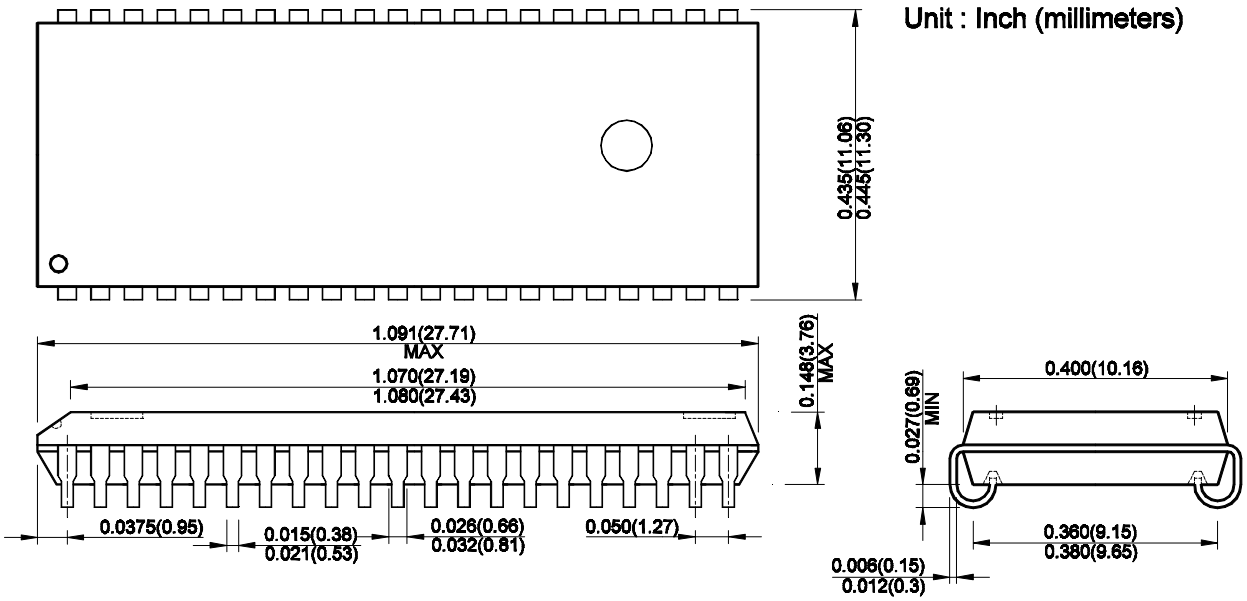
SPEED
-SRAM
12 : 12ns
15 : 15ns
20 : 20ns
70 : 70ns
-DRAM
30 : 30ns
35 : 35ns
40 : 40ns
45 : 45ns
50 : 50ns
60 : 60ns

PACKAGE
T : PDIP(300mil)
TS : TSOP(Type I)
TC : TSOP(Type II)
PL : PLCC
FA : 300mil SOP
FB : 330mil SOP
FC : 445mil SOP
J3 : 300mil SOJ
J4 : 400mil SOJ
P : PDIP(600mil)
Q : PQFP
TQ : TQFP

Note : C➞CDROM , H➞HDD.
Example :
1.GLT710008-15T 1Mbit(128Kx8)15ns 5V SRAM PDIP(300mil)Package type.
2.GLT44016-40J4 4Mbit(256Kx16)40ns 5V DRAM SOJ(400mil)Package type.

Package Information

40/42L 400MIL SOJ



44/50L TSOPII 400MIL