G-LINK

GLT6200L08

Ultra Low Power 256k x 8 CMOS SRAM

Nov 2000(Rev. 1.0)

Features :

- Low-power consumption.
  -active: 30mA at 55ns.
  -stand by :
  10 μA (CMOS input / output)
  2 μA (CMOS input / output, SL)
- Single +2.7 to 3.3V power supply.
- Equal access and cycle time.
- 55/70/85 ns access time.
- 1.0V data retention mode.
- TTL compatible, tri-state input/output.
- Automatic power-down when deselected.
- Industrial grade (-40°C ~ 85°C) available.
- Package available: 32-sTSOP.
  48Ball CSP-BGA

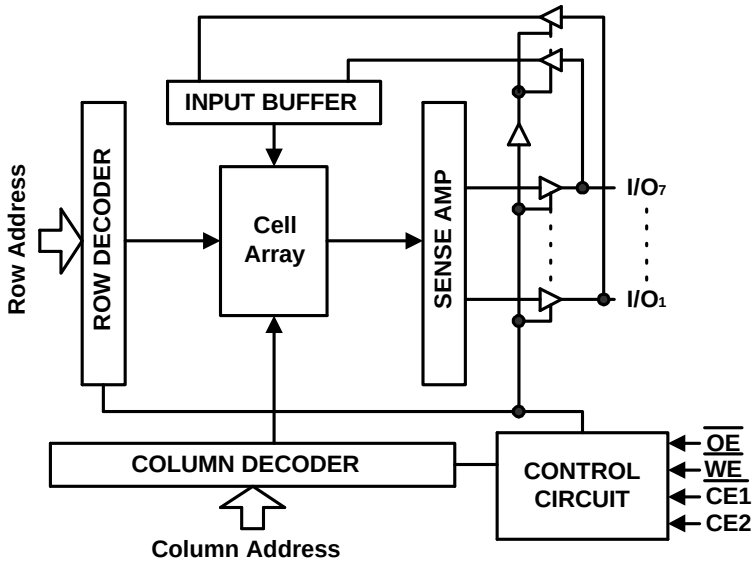
Description :

The GLT6200L08 is a low power CMOS Static RAM organized as 262,144 x 8 bits. Easy memory expansion is provided by an active LOW $\overline{CE1}$ an active LOW $\overline{OE}$, and Tri-state I/O's. This device has an automatic power-down mode feature when deselected.

Writing to the device is accomplished by taking chip Enable 1 ($\overline{CE1}$) with Write Enable ($\overline{WE}$) LOW. Reading from the device is performed by taking Chip Enable 1 ($\overline{CE1}$) with Output Enable ($\overline{OE}$) LOW while Write Enable ($\overline{WE}$) and Chip Enable 2 (CE2) is HIGH. The I/O pins are placed in a high-impedance state when the device is deselected : the outputs are disabled during a write cycle.

The GLT6200L08 comes with a 1V data retention feature and Lower Standby Power. The GLT6200L08 is available in a 32-pin sTSOP packages.

Function Block Diagram :



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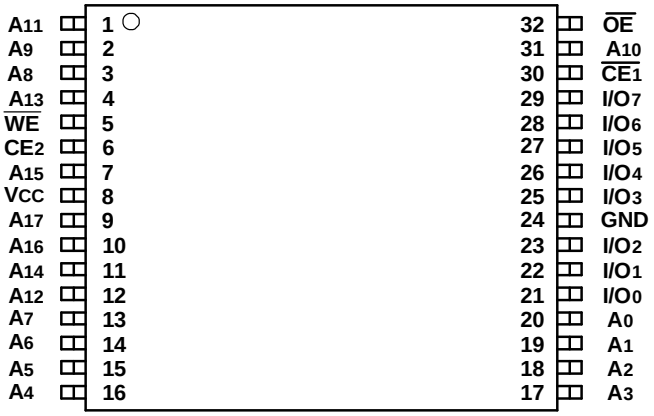
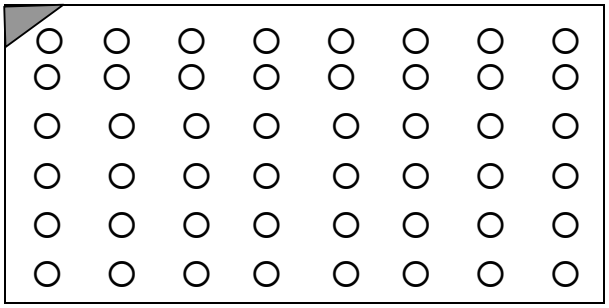
Pin Configurations :

sTSOPI

GLT6200L08



48 Ball fpBGA :



	A	B	C	D	E	F	G	H
1	A0	I/O4	I/O5	VSS	VCC	I/O6	I/O7	A9
2	A1	A2	NC	NC	NC	NC	$\overline{OE}$	A10
3	CE2	$\overline{WE}$	NC	NC	NC	NC	$\overline{CE}$	A11
4	A3	A4	A5	NC	NC	A17	A16	A12
5	A6	A7	NC	NC	NC	NC	A15	A13
6	A8	I/O0	I/O1	VCC	VSS	I/O2	I/O3	A14

Note：NC means no Ball.

Pin Descriptions:

Name	Function
$A_0 – A_{17}$	Address Inputs
$\overline{CE}_1$ and CE2	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
$I/O_0 – I/O_7$	Data Input and Data Output
V_{CC}	3V Power Supply
GND	Ground
NC	No Connection

Truth Table:

$\overline{CE_1}$	$\overline{WE}$	$\overline{OE}$	Data	Mode
H	X	X	High-Z	Standby
X	X	X	High-Z	Standby
L	H	L	Data Out	Active, Read
L	H	H	High-Z	Active, Output Disable
L	L	X	Data Out	Active, Write

*Key : X = Don't Care, L = Low, H = High

Absolute Maximum Ratings*

Parameter	Symbol	Minimum	Maximum	Unit
Voltage on Any Pin Relative to Gnd	Vt	-0.5	Vcc+0.5	V
Power Dissipation	P_T	-	1.0	W
Storage Temperature (Plastic)	Tstg	-55	+150	°C
Temperature Under Bias	Tbias	-40	+85	°C

*Note : Stresses greater than those listed above Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions (T_A = -25°C to + 85°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.7	3	3.3	V
	Gnd	0.0	0.0	0.0	V
Input Voltage	V_{IH}	2.0	-	V_{CC}+0.2	V
	V_{IL}	-0.5*	-	0.6	V

* V_{IL} min = -1.0V for pulse width less than $t_{RC}/2$.

DC Operating Characteristics (Vcc=2.7V to 3.3V, T_A =-25°C to + 85°C)

Parameter	Sym.	Test Conditions	55		70		85		Unit
			Min	Max	Min	Max	Min	Max	
Input Leakage Current	$\|I_{LI}\|$	V_{CC} = Max, Vin = Gnd to V_{CC}		1		1		1	µA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CE}_1$ =V_{IH} V_{CC} = Max, V_{OUT} = Gnd to V_{CC}		1		1		1	µA
Operating Power Supply Current	I_{CC}	$\overline{CE}_1$ =V_{IL} , V_{IN}=V_{IH} or V_{IL}, I_{OUT}=0mA		3		3		3	mA
Average Operating Current	I_{CC1}	$\overline{CE}_1$ =V_{IL} , I_{OUT} = 0mA, Min Cycle, 100% Duty		30		30		25	mA
	I_{CC2}	$\overline{CE}_1$ =0.2V I_{OUT} = 0mA, Cycle Time=1µs, 100% Duty		3		3		3	mA
Standby Power Supply Current(TTL Level)	I_{SB}	$\overline{CE}_1$ =V_{IH}		0.5		0.5		0.5	mA
Standby Power Supply Current (CMOS Level)	I_{SB1}	$\overline{CE}_1$ ≥ V_{CC}-0.2V or f=0 V_{IN} ≤ 0.2V or V_{IN} ≥ V_{CC}-0.2V	10			10		10	µA
			2			2		2	µA
Output Low Voltage	V_{OL}	I_{OL} = 2 mA		0.4		0.4		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4		2.4		2.4		V

Data Retention

Parameter	Sym.	Test Conditions	Min.	Max.	Unit
V_{CC} for Data retention	V_{DR}	$\overline{CE}_1$ ≥ V_{CC} -0.2V or V_{IN} ≥ V_{CC} -0.2V or V_{IN} ≤ 0.2V	1.0	-	V
Data Retention Current	I_{CCDR}		-	2	µA
Chip Deselect to Data Retention Time	t_{CDR}		0	-	ns
Operating Recovery Time(2)	t_R		t_{RC}	-	ns

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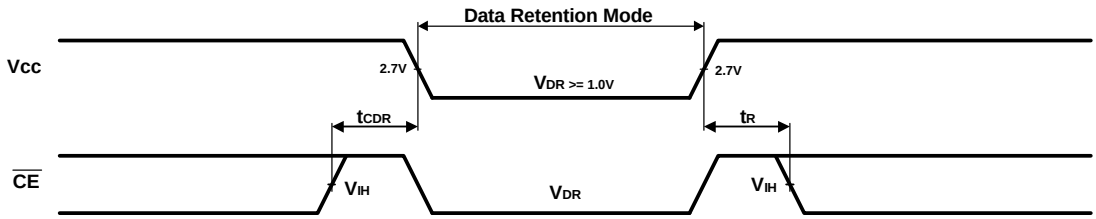
Data Retention Waveform (TA = -25°C to + 85°C)



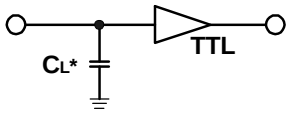
AC Test Conditions

Input Pulse Levels	0.4V to 2.4V
Input Rise and Fall Time	5 ns
Input and Output Timing Reference Level	1.4V

Output Load Condition

C_L = 30pf + 1TTL Load

AC Test Loads and Waveforms

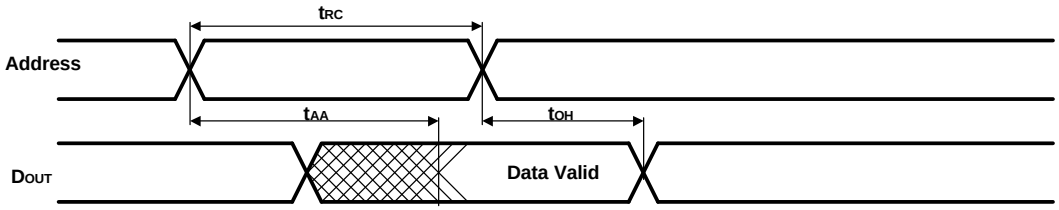


*Including Scope and Jig Capacitance

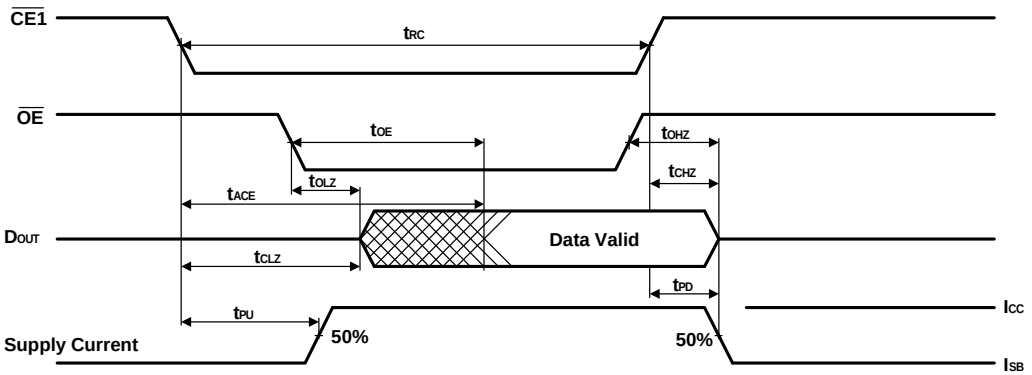
Read Cycle (3,9)(Vcc=2.7V to 3.3V, T_A =-25°C to + 85°C)

Parameter	Symbol	55		70		85		Unit	Note
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{RC}	55		70		85		ns	
Address Access Time	t_{AA}		55		70		85	ns	
Chip Enable Access Time	t_{ACE}		55		70		85	ns	
Output Enable Access Time	t_{OE}		40		40		40	ns	
Output Hold from address Change	t_{OH}	10		10		10		ns	
Chip Enable to Output in Low-Z	t_{CLZ}	10		10		10		ns	4,5
Chip Disable to Output in High-Z	t_{CHZ}		25		30		35	ns	4,5
Output Enable to Output in Low-Z	t_{OLZ}	5		5		5		ns	4,5
Output Disable to Output in High-Z	t_{OHZ}		20		25		30	ns	4,5
Power-Up Time	t_{PU}	0		0		0		ns	5
Power-Down Time	t_{PD}		55		70		85	ns	5

Timing Waveform of Read Cycle 1 (3,6,7,9) (Address Controlled)



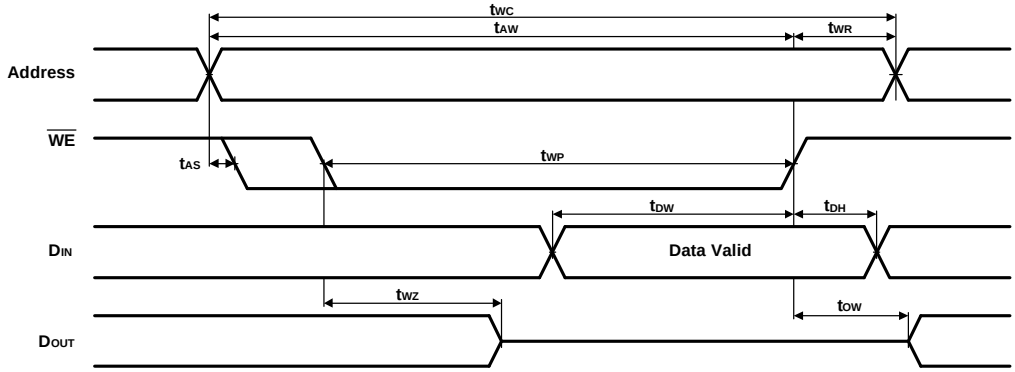
Timing Waveform of Read Cycle 2 (5,6,8,9) ($\overline{CE1}$ Controlled)



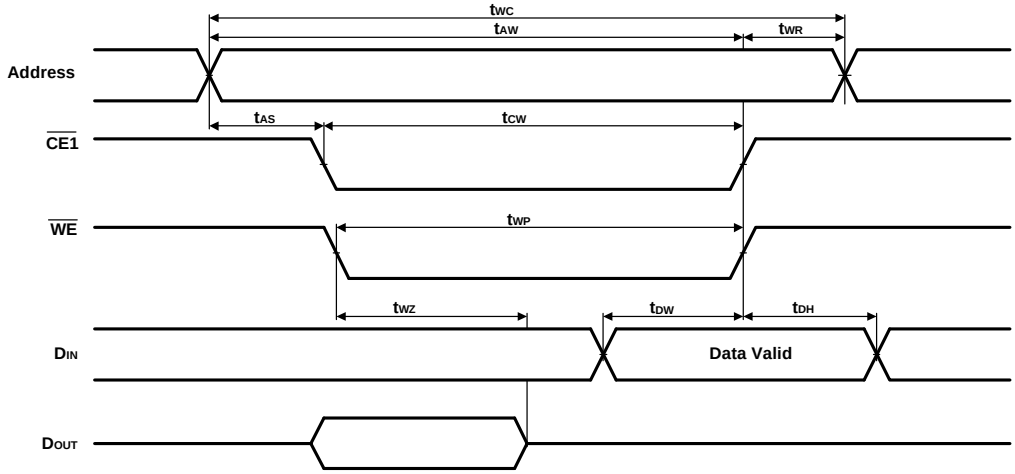
Write Cycle (3,11)(Vcc=2.7V to 3.3V, T_A =-25°C to + 85°C)

Parameter	Symbol	55		70		85		Unit	Note
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{WC}	55		70		85		ns	
Chip Enable to Write End	t_{CW}	40		60		70		ns	
Address Setup to Write End	t_{AW}	40		60		70		ns	
Address Setup Time	t_{AS}	0		0		0		ns	
Write Pulse Width	t_{WP}	40		50		60		ns	
Write Recovering Time	t_{WR}	0		0		0		ns	
Data Valid to Write End	t_{DW}	25		30		35		ns	
Data Hold Time	t_{DH}	0		0		0		ns	
Write Enable to Output in High-Z	t_{WZ}		25		30		35	ns	4,5
Output Active from Write End	t_{OW}	5		5		5		ns	4,5

Timing Waveform of Write Cycle 1 (10,11) ($\overline{WE}$ Controlled)



Timing Waveform of Write Cycle 2 (10,11) ($\overline{CE1}$ Controlled)



Notes :

1. L-version includes this feature.
2. This Parameter is samples and not 100% tested.
3. For test conditions, see AC Test Condition.
4. This parameter is tested with CL = 5pF. Transition is measured ± 500mV from steady – state voltage.
5. This parameter is guaranteed, but is not tested.
6. $\overline{WE}$ is HIGH for read cycle.
7. $\overline{CE1}$ and $\overline{OE}$ are LOW and for read cycle.
8. Address valid prior to or coincident with $\overline{CE1}$ transition LOW .
9. All read cycle timings are referenced from the last valid address to the first transition address.
10. $\overline{CE1}$ or WE must be HIGH during address transition.
11. All write cycle timings are referenced from the last valid address to the first transition address.

Ordering Information

Part Number	*SPEED*	*POWER*	*PACKAGE*
GLT6200L08LL-55 ST	55ns	Normal	sTSOPI 32L
GLT6200L08LL-70 ST	70ns	Normal	sTSOPI 32L
GLT6200L08LL-85 ST	85ns	Normal	sTSOPI 32L
GLT6200L08SL-55 ST	55ns	Normal	sTSOPI 32L
GLT6200L08SL-70 ST	70ns	Normal	sTSOPI 32L
GLT6200L08SL-85 ST	85ns	Normal	sTSOPI 32L
GLT6200L08LLI-55 ST	55ns	Normal	sTSOPI 32L
GLT6200L08LLI-70 ST	70ns	Normal	sTSOPI 32L
GLT6200L08LLI-85 ST	85ns	Normal	sTSOPI 32L
GLT6200L08SLI-55 ST	55ns	Normal	sTSOPI 32L
GLT6200L08SLI-70 ST	70ns	Normal	sTSOPI 32L
GLT6200L08SLI-85 ST	85ns	Normal	sTSOPI 32L
GLT6200L08LL-55 FG	55ns	Normal	fpBGA-48L
GLT6200L08LL-70 FG	70ns	Normal	fpBGA-48L
GLT6200L08LL-85 FG	85ns	Normal	fpBGA-48L
GLT6200L08SL-55 FG	55ns	Normal	fpBGA-48L
GLT6200L08SL-70 FG	70ns	Normal	fpBGA-48L
GLT6200L08SL-85 FG	85ns	Normal	fpBGA-48L
GLT6200L08LLI-55 FG	55ns	Normal	fpBGA-48L
GLT6200L08LLI-70 FG	70ns	Normal	fpBGA-48L
GLT6200L08LLI-85 FG	85ns	Normal	fpBGA-48L
GLT6200L08SLI-55 FG	55ns	Normal	fpBGA-48L
GLT6200L08SLI-70 FG	70ns	Normal	fpBGA-48L
GLT6200L08SLI-85 FG	85ns	Normal	fpBGA-48L

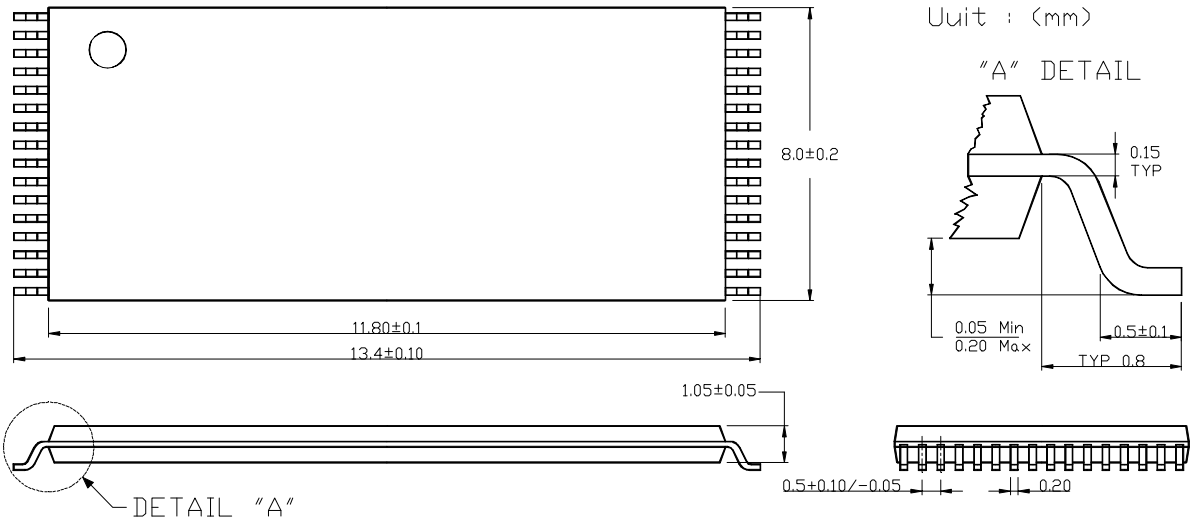
Parts Numbers (Top Mark) Definition :

GLT 6 200 L 08 LL I - 55 TS

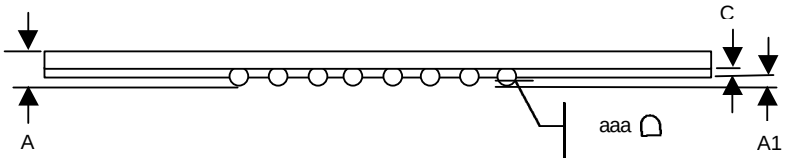
- **6**
  - 4 : DRAM
  - 6 : Standard SRAM
  - 7 : Cache SRAM
  - 8 : Synchronous Burst SRAM
- **200**
  - **-SRAM**
    - 064 : 64K
    - 256 : 256K
    - 512 : 512K
    - 100 : 1M
  - **-DRAM**
    - 10 : 1M(C/EDO)*
    - 11 : 1M(C/FPM)*
    - 12 : 1M(H/EDO)*
    - 13 : 1M(H/FPM)*
    - 20 : 2M(EDO)
    - 21 : 2M(FPM)
    - 40 : 4M(EDO)
    - 41 : 4M(FPM)
    - 80 : 8M(EDO)
    - 81 : 8M(FPM)
    - *See note
- **L**
  - **VOLTAGE**
    - Blank : 5V
    - L : 3.3V
    - M : 2.5V
    - N : 2.1V
- **08**
  - **CONFIG.**
    - 04 : x04
    - 08 : x08
    - 16 : x16
    - 32 : x32
- **LL**
  - LL : Low Low power
  - L : Low power
  - SL : Super Low power
- **I**
  - I : Industrial Temperature
- **-55**
  - **SPEED**
  - **-SRAM**
    - 10 : 10ns
    - 12 : 12ns
    - 15 : 15ns
    - 20 : 20ns
    - 70 : 70ns
  - **-DRAM**
    - 35 : 35ns
    - 40 : 40ns
    - 45 : 45ns
    - 50 : 50ns
    - 60 : 60ns
- **TS**
  - **PACKAGE**
    - T : PDIP(300mil)
    - TS : TSOP(Type I)
    - ST : sTSOP (Type I)
    - TC : TSOP(Type ll)
    - PL : PLCC
    - FA : 300mil SOP
    - FB : 330mil SOP
    - FC : 445mil SOP
    - J3 : 300mil SOJ
    - J4 : 400mil SOJ
    - P : PDIP(600mil)
    - Q : PQFP
    - TQ : TQFP
    - FG : 48-fpBGA

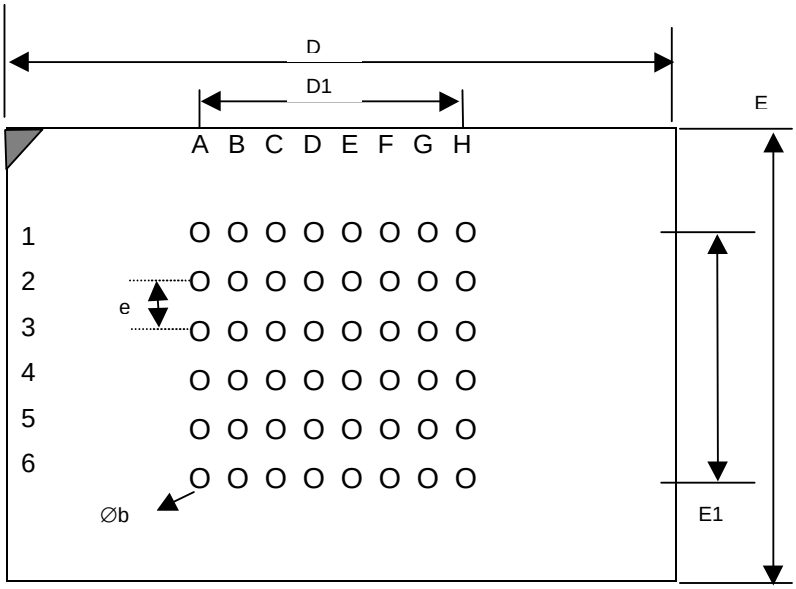
Package Information

32 pin 8x13.4mm Small Outline J-form Package (sTSOP)



GLT6200L08 fpBGA





PACKAGE OUTLINE DWG.

SYMBOL	UNIT : MM
A	1.10±0.1
A1	0.22±0.05
∅b	0.35
C	0.36TYP
D	8.00±0.10
D1	5.25
E	6.00±0.10
E1	3.75
e	0.75TYP
aaa∩	0.10

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