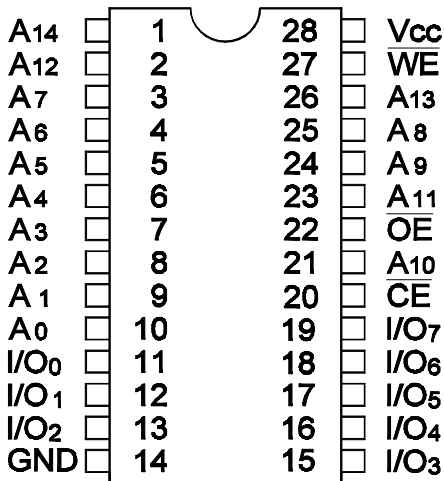
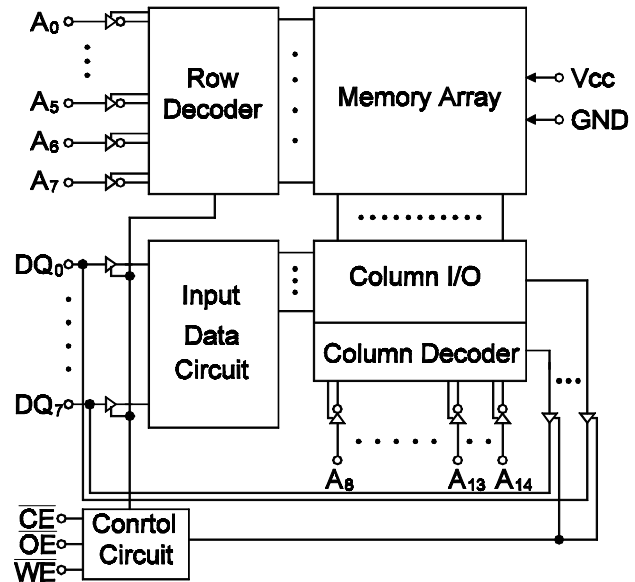


**Features :**

- \* Available in 70/100ns(MAX.)
- \* Automatic power-down when chip disabled
- \* Low power consumption:  
GLT625608  
-467.5mW(Max.) Operating
- \* -500 $\mu$ W(Max.) Standby
- \* TTL compatible interface levels
- \* Single 5V power supply
- \* Fully static operation
- \* Three state outputs
- \* 256K bit EPROM pin compatible
- \* Data Retention as low as 2V
- \* Industrial Grade (-40°C~85°C) available.

**Description :**

GLT625608 is a 262,144-bit static random access memory organized as 32,768 words by 8 bits and operates from a single 5 volt supply. Inputs and three-state outputs are TTL compatible and allow for direct interfacing with system I/O bus. The GLT625608 is available in a standard 330 mil SOP packages. Other packages will also available upon request.

**Pin Configurations:**
**GLT625608**

**Function Block Diagram :**


**Pin Descriptions:**

Name	Function
A <sub>0</sub> - A <sub>14</sub>	Address Inputs
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable
I/O <sub>0</sub> -I/O <sub>7</sub>	Data Input/Output
V <sub>cc</sub>	Power Supply (+5V)
GND	Ground

**Truth Table:**

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O Operation	Supply Current
Not Selected ( Power down )	X	H	X	High Z	I <sub>SB</sub> , I <sub>SB1</sub>
				High Z	I <sub>SB</sub> , I <sub>SB1</sub>
Output Disabled	H	L	H	High Z	I <sub>CC</sub>
Read	H	L	L	D <sub>OUT</sub>	I <sub>CC</sub>
Write	L	L	X	D <sub>IN</sub>	I <sub>CC</sub>

NOTE: X : H or L

**Absolute Maximum Ratings:**

Ambient Temperature

Under Bias.....-10°C to +80°C

Storage Temperature(plastic)....-55°C to +125°C

Voltage Relative to GND.....-0.5V to + 7.0V

Data Output Current.....50mA

Power Dissipation.....1.0W

1.Stresses greater than those listed under ABSOLUTE MAXIMUM RATING may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Operation Range :**

RANGE	AMBIENT TEMPERATURE	V <sub>cc</sub>
Commercial	0°C to + 70°C	5V ± 10%
Industrial	-40°C to 85°C	5V ± 10%

**Capaccitance<sup>(1)</sup>(T<sub>A</sub>=25°C,F=1.0MHz)**

SYMBOL	PARAMETER	CONDIT IONS	MAX.	UNIT
CIN	Input Capacitance	VIN=0V	6	pF
CDQ	Input/Output capacitance	VI/O=0	8	pF

1.This parameter is guaranteed and tested.

**DC Characteristics**

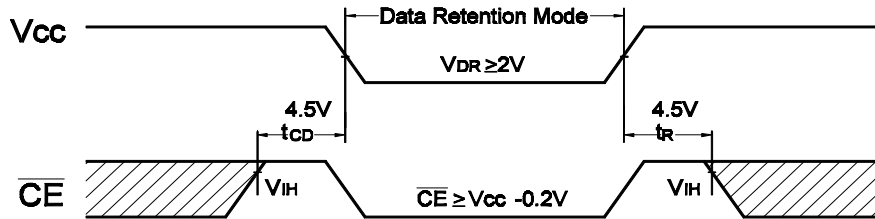
Sym.	Parameter	Test Conditions	Min.	Typ <sup>(1)</sup>	Max.	Unit
V <sub>IL</sub>	Guaranteed Input Low Voltage <sup>(2)(3)</sup>		-0.3	-	+0.8	V
V <sub>IH</sub>	Guaranteed Input High Voltage <sup>(2)</sup>		2.2	-	V <sub>CC</sub> +0.3	V
I <sub>LI</sub>	Input Leakage Current	V <sub>CC</sub> =Max., V <sub>IN</sub> =0V to V <sub>CC</sub>	-5	-	5	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>CC</sub> =Max., $\overline{CE} \geq V_{IH}$	-5	-	5	μA
V <sub>OL</sub>	Output Low Voltage	V <sub>CC</sub> =Min., I <sub>OL</sub> =8mA	-	-	0.4	V
V <sub>OH</sub>	Output High Voltage	V <sub>CC</sub> =Min., I <sub>OH</sub> =-4mA	2.4	-	-	V
I <sub>CC</sub>	Operating Power Supply Current	V <sub>CC</sub> =Max., $\overline{CE} \leq V_{IL}$ , I <sub>I/O</sub> =0mA., F=F <sub>max</sub> <sup>(3)</sup>	-	-	100	mA
I <sub>CCSB</sub>	Standby Power Supply Current	V <sub>CC</sub> =Max., $\overline{CE} \geq V_{IH}$ , I <sub>I/O</sub> =0mA., F=F <sub>max</sub> <sup>(3)</sup>	-	-	20	mA
I <sub>CCSB1</sub>	Power Down Power Supply Current	V <sub>CC</sub> =Max., $\overline{CE} \geq V_{CC} - 0.2V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or	-	10	10	mA

1. Typical characteristics are at V<sub>CC</sub>=5V, T<sub>A</sub>=25°C.
2. These are absolute values with repeat to device ground and all overshoots due to system or tester noise are included.
3. F<sub>MAX</sub>=1/t<sub>RC</sub>.

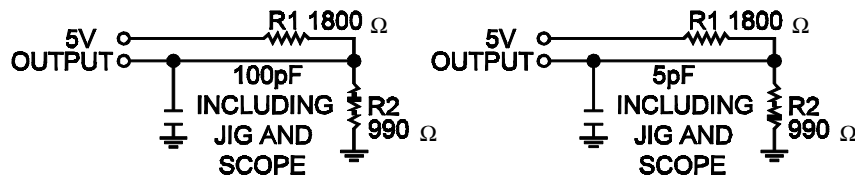
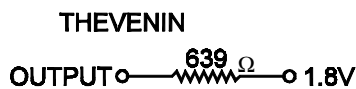
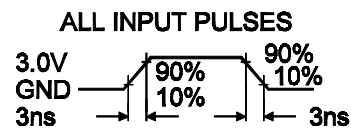
**Data Retention**

Sym.	Parameter	Test Conditions	Min.	Typ	Max.	Unit
V <sub>DR</sub>	V <sub>CC</sub> for Data retention	$\overline{CE} \geq V_{CC} - 0.2V$ V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V	2.0	-	-	V
I <sub>CCDR</sub>	Data Retention Current	$\overline{CE} \geq V_{DR} - 0.2V$ V <sub>IN</sub> ≥ V <sub>DR</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V	-	2	50	μA <sup>(1)</sup>
t <sub>CDR</sub>	Chip Deselect to Data Retention Time	See Retention Waveform	0	-	-	ns
t <sub>R</sub>	Operating Recovery Time		t <sub>RC</sub> <sup>(2)</sup>	-	-	ns

1. V<sub>DR</sub> = 3V, T<sub>A</sub> = Specified
2. t<sub>RC</sub> = Read Cycle Time

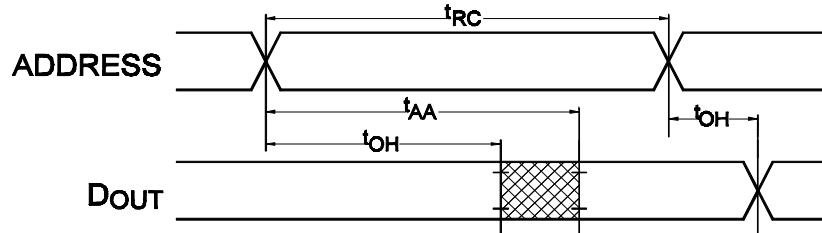
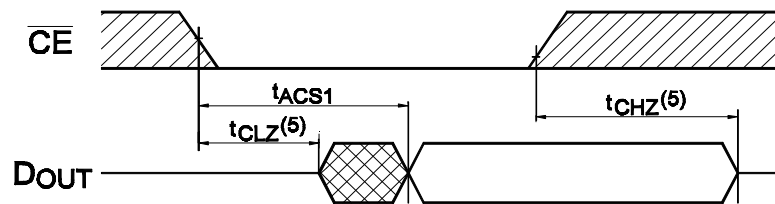
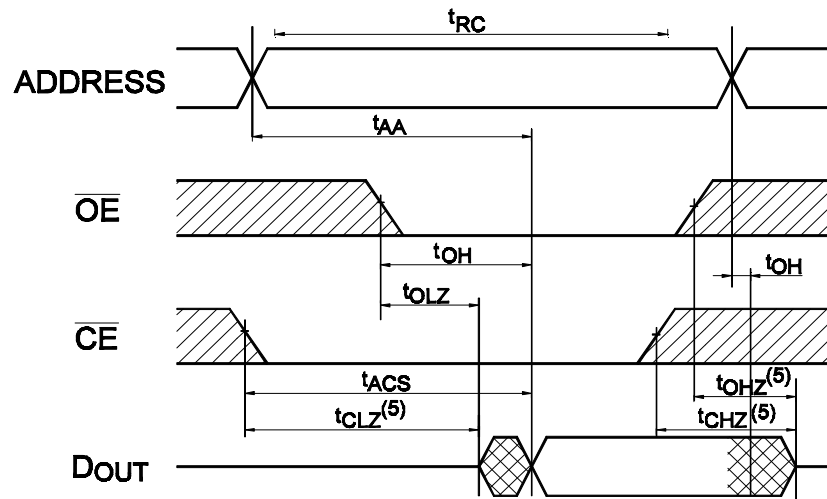
**Low  $V_{CC}$  Data Retention Waveform ( $\overline{CE}$  Controlled)**

**AC Test Conditions**

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Level	1.5V

**AC Test Loads and Waveforms**

**Figure 1a**
**Figure 1b**

**THEVENIN**

**Figure 2**

**AC Electrical Characteristics**  
**Read Cycle**

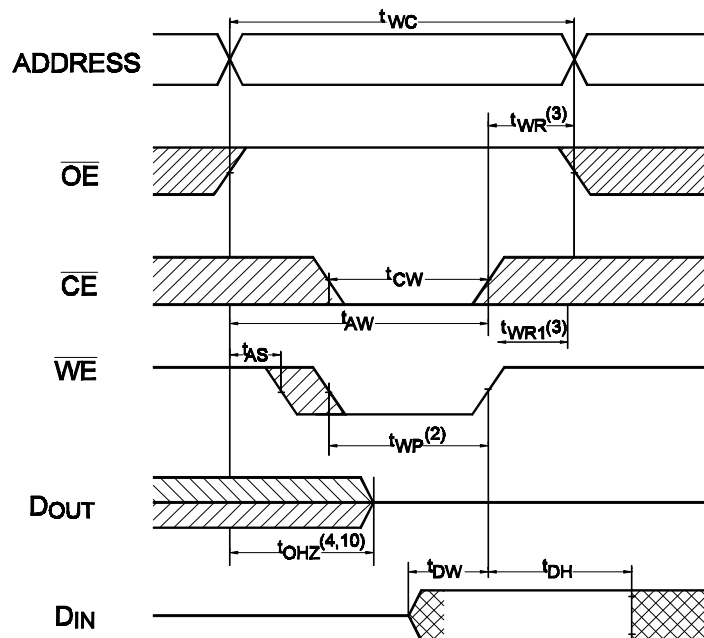
JEDEC Parameter Name	Parameter Name	Parameter	625608-70		625608-10		Unit
			Min.	Max.	Min.	Max.	
t <sub>AVAX</sub>	t <sub>RC</sub>	Read Cycle Time	70	-	100	-	ns
t <sub>AVQV</sub>	t <sub>AA</sub>	Address Access Time	-	70	-	100	ns
t <sub>ELQV</sub>	t <sub>ACS</sub>	Chip Select Access Time	-	70	-	100	ns
t <sub>GLQV</sub>	t <sub>OE</sub>	Output Enable to Output Valid	-	40	-	50	ns
t <sub>ELQZ</sub>	t <sub>CLZ</sub>	Chip Deselect to Output in Low Z	5	-	10	-	ns
t <sub>GLQX</sub>	t <sub>OLZ</sub>	Output Enable to Output in Low Z	5	-	5	-	ns
t <sub>EHQZ</sub>	t <sub>CHZ</sub>	Chip Deselect to Output in High Z	0	30	0	35	ns
t <sub>GHQZ</sub>	t <sub>OHZ</sub>	Output Disable to Output in High Z	0	30	0	35	ns
t <sub>AXQX</sub>	t <sub>OH</sub>	Output Hold from Address Change	5	-	10	-	ns

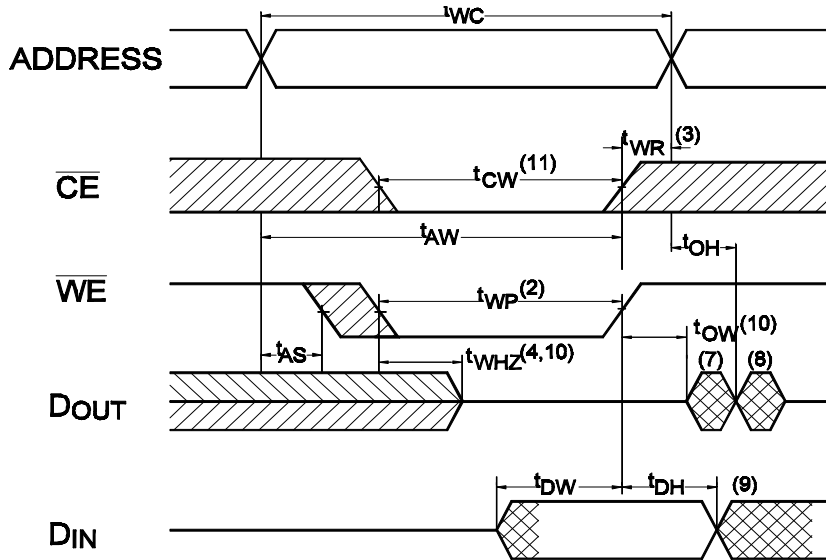
**Switching Waveforms (Read Cycle)**
**READ CYCLE 1<sup>(1,2,4)</sup>**

**READ CYCLE 2<sup>(1,3,4)</sup>**

**READ CYCLE 3<sup>(1)</sup>**

**Notes:**

1.  $\overline{WE}$  is High for READ Cycle.
2. Device is continuously selected  $\overline{OE} = V_{IL}$ .
3. Address valid prior to or coincident with  $\overline{CE}$  transition low.
4.  $\overline{CE} = V_{IL}$ .
5. Transition is measured  $\pm 500\text{mV}$  from steady state with  $C_L = 5\text{pF}$  as shown in Figure 1b. This parameter is guaranteed but not 100% tested.

**AC Electrical Characteristics**  
**Write Cycle**

JEDEC Parameter Name	Parameter Name	Parameter	625608-70		625608-10		Unit
			Min.	Max.	Min.	Max.	
$t_{AVAX}$	$t_{WC}$	Write Cycle Time	70	-	100	-	ns
$t_{ELWH}$	$t_{CW}$	Chip Enable to End of Write	65	-	90	-	ns
$t_{AVWL}$	$t_{AS}$	Address Set up Time	0	-	0	-	ns
$t_{AVWH}$	$t_{AW}$	Address Valid to End of Write	65	-	90	-	ns
$t_{WLWH}$	$t_{WP}$	Write Pulse Width	55	-	75	-	ns
$t_{WHAX}$	$t_{WR1}$	Write Recovery Time	5	-	5	-	ns
$t_{WLQZ}$	$t_{WHZ}$	Data to Write Time Overlap	0	30	0	35	ns
$t_{DVWH}$	$t_{DW}$	Data to Write Time Overlap	35	-	40	-	ns
$t_{WHDX}$	$t_{DH}$	Data Hold from Write Time	0	-	0	-	ns
$t_{GHQZ}$	$t_{OHZ}$	Output Disable to Output in High Z	0	30	0	40	ns
$t_{WHQX}$	$t_{OW}$	End of Write to Output Active	5	-	5	-	ns

**Switching Waveforms (Write Cycle)**  
**WRITE CYCLE 1<sup>(1)</sup>**


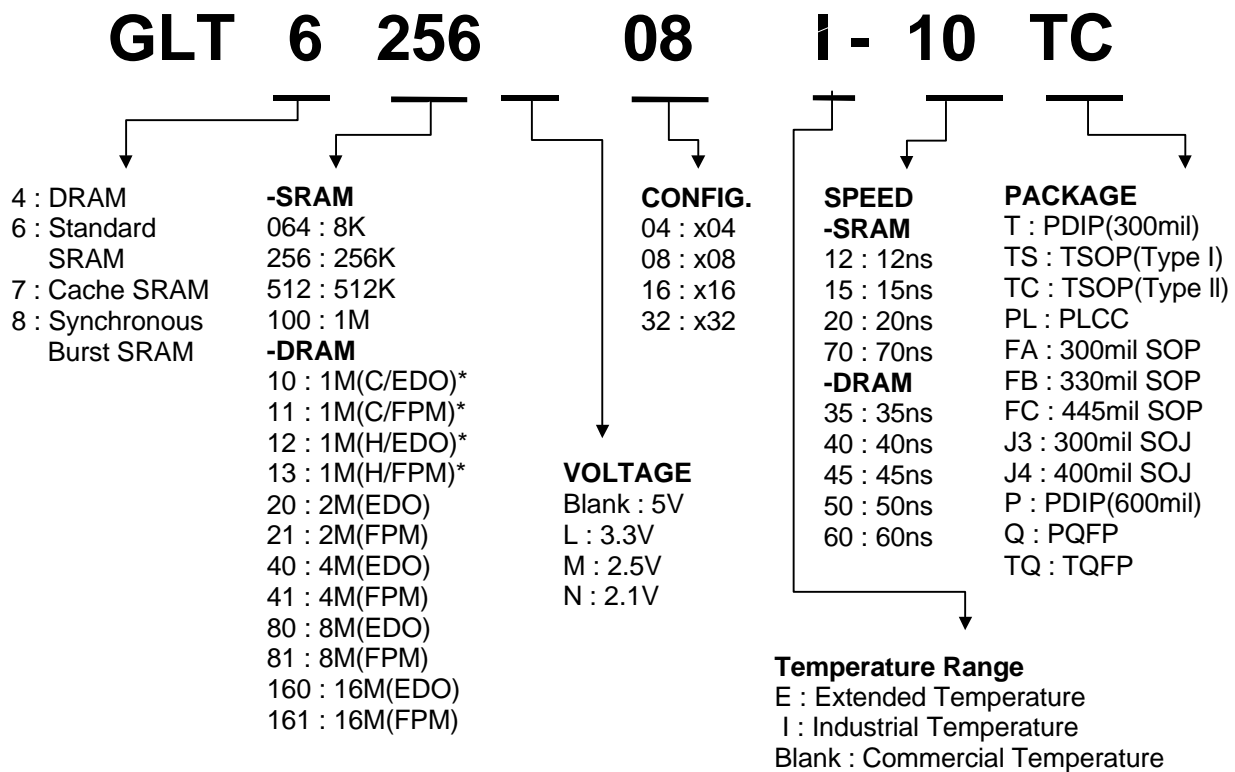
**WRITE CYCLE 2<sup>(1,6)</sup>**

**Note:**

1.  $\overline{WE}$  must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of  $\overline{CE}$  active and  $\overline{WE}$  low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3.  $T_{WR}$  is measured from the earlier of  $\overline{CE}$  or  $\overline{WE}$  going high at the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the  $\overline{CE}$  low transition occurs simultaneously with the  $\overline{WE}$  low transitions or after the  $\overline{WE}$  transition, outputs remain in a high impedance state.
6.  $\overline{OE}$  is continuously low ( $\overline{OE} = V_{IL}$ ).
7.  $D_{OUT}$  is the same phase of write data of this write cycle.
8.  $D_{OUT}$  is the read data of next address.
9. If  $\overline{CE}$  is low is high during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured  $\pm 200\text{mV}$  from steady state with  $C_L = 5\text{pF}$ .
11.  $t_{CW}$  is measured from  $\overline{CE}$  going low to the end of write.



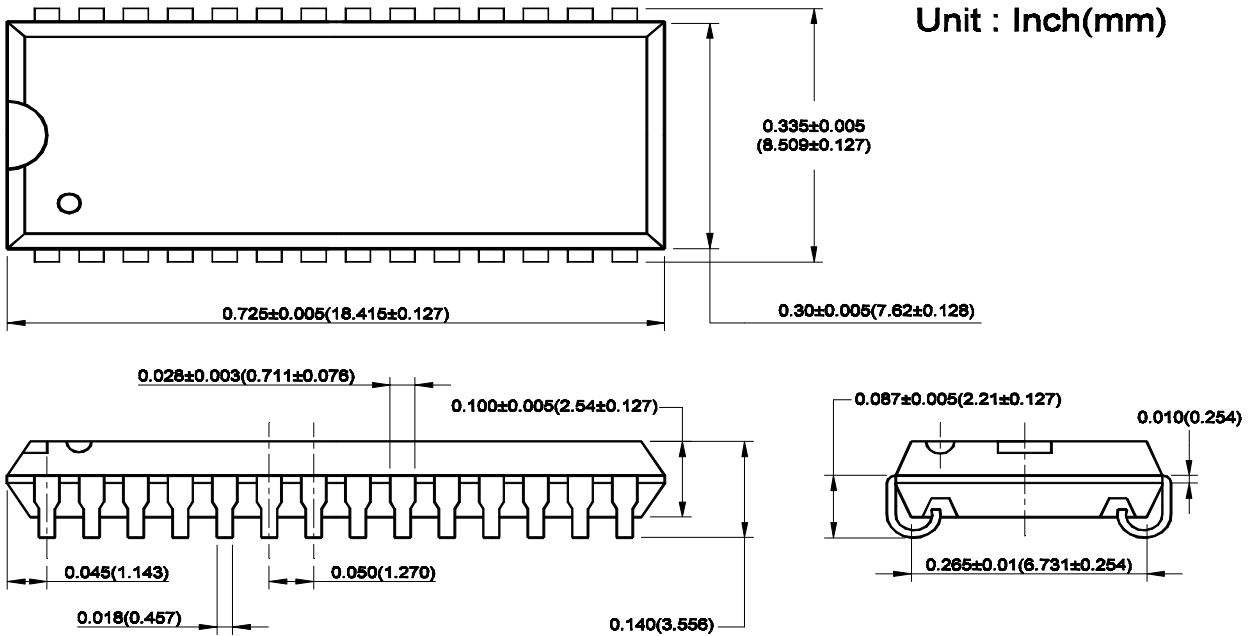
**Ordering Information**

<b>Part Number</b>	<b>SPEED</b>	<b>POWER</b>	<b>PACKAGE</b>
GLT625608-10J3	10ns	Normal	SOJ 300mil 28L
GLT625608-70J3	70ns	Normal	SOJ 300mil 28L
GLT625608-10TS	10ns	Normal	TSOPI 28L
GLT625608-70TS	70ns	Normal	TSOPI 28L
GLT625608-10TC	10ns	Normal	TSOPII 28L
GLT625608-70TC	70ns	Normal	TSOPII 28L
GLT625608-10FB	10ns	Normal	SOP 330mil 28L
GLT625608-70FB	70ns	Normal	SOP 330mil 28L

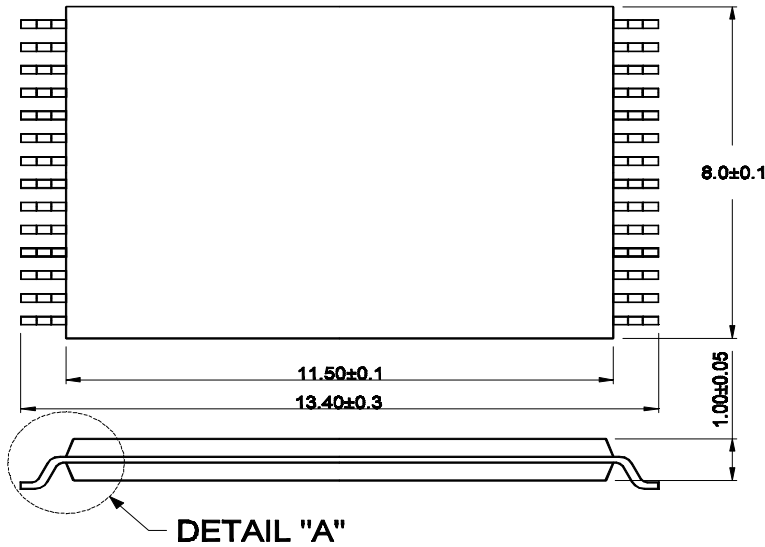
**Parts Numbers (Top Mark) Definition :**


**Package Information**

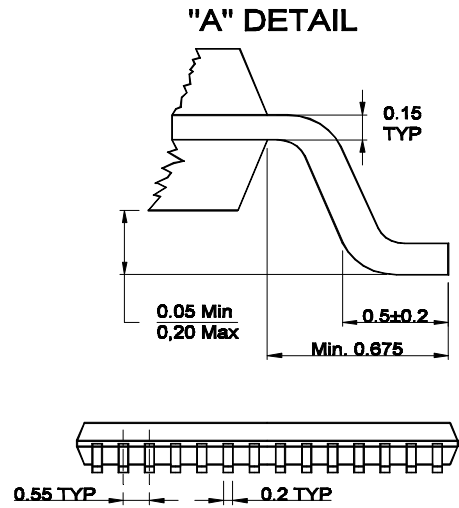
300mil 28 Lead Small Outline J-form Package (SOJ)



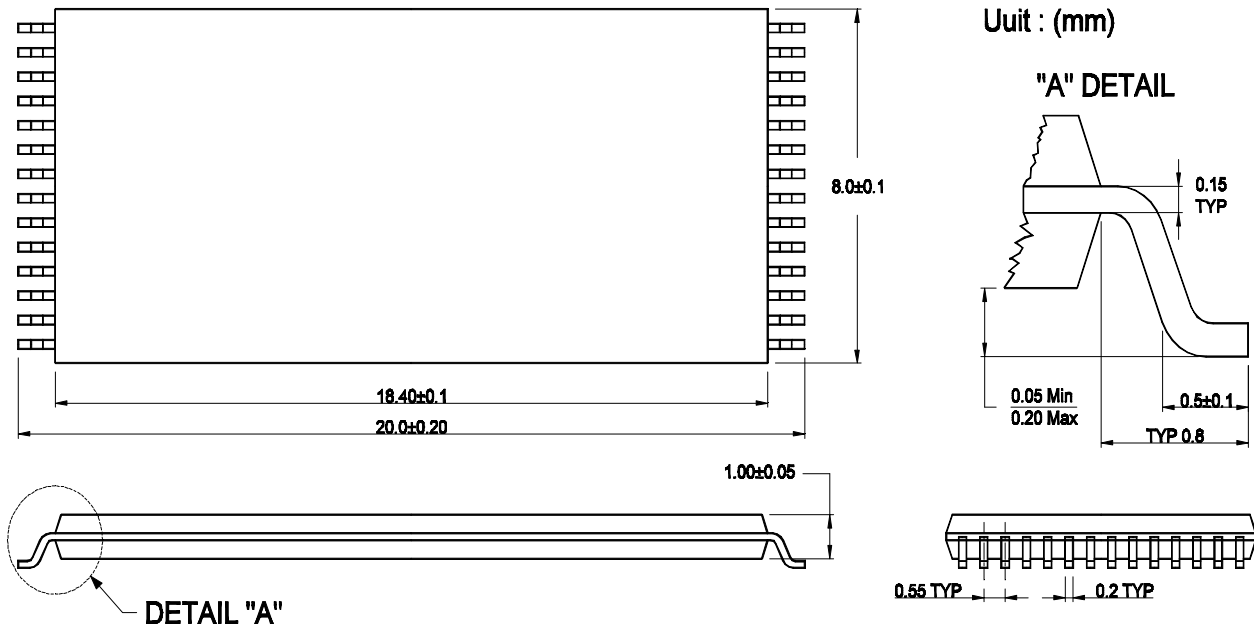
28 L (8 × 13.4 mm ) Thin Small Outline Package (TSOP) Type I



Unit : (mm)



28 L (8 × 20 mm ) Thin Small Outline Package (TSOP) Type I



330mil 28 Lead Thin Small Outline(Gull-Wing) Package (SOP)

Unit : Inch

