GLT7256L08

Ultra High Performance 3.3V 32K x 8 Bit CMOS STATIC RAM

Mar 2000(REV. 2.0)

Features :

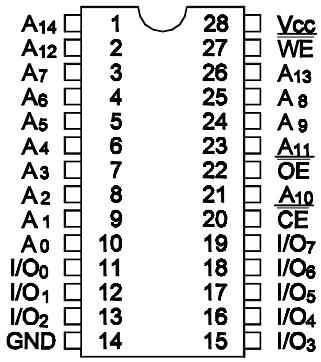
* 32K x 8-bit organization.
* Very high speed – 8,10,12,15 ns.
* Low standby power.
  Maximum 2mA for GLT7256L08.
* Fully static operation
* 3.3V±5% power supply.
* TTL compatible I/O.
* Three state output.
* Chip enable for simple memory expansion.
* Available in 28 PIN 300 mil SOJ and TSOP packages.

Description :

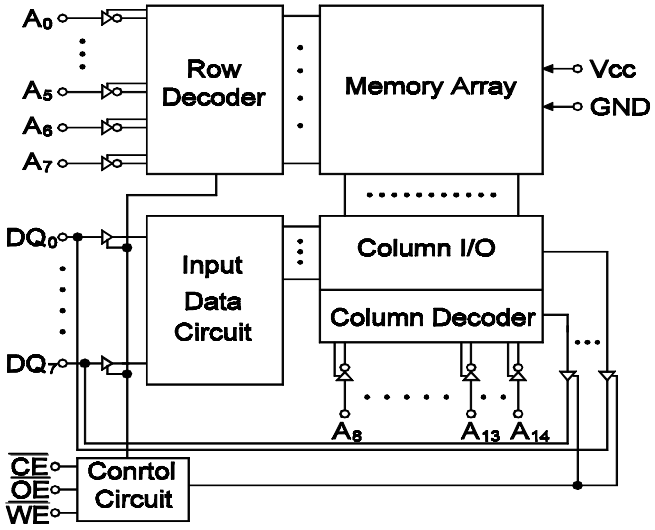
GLT7256L08 are high performance 256K bit static random access memories organized as 32K by 8 bits and operate at a single 3.3 volt supply. Fabricated with G-Link Technology's very advanced CMOS sub-micron technology, GLT7256L08 offer a combination of features: very high speed and very low stand-by current. In addition, this device also supports easy memory expansion with an active LOW chip enable ($\overline{CE}$) as well as an active LOW output enable ($\overline{OE}$) and three state outputs.

Pin Configurations :

GLT7256L08



Function Block Diagram :



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Pin Descriptions:

Name	Function
A_0 - A_{14}	Address Inputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O_O - I/O_7	Data Input and Data Output
V_{CC}	+3.3V Power Supply
GND	Ground

Truth Table:

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O Operation	V_{CC} Current
Not Selected (Power Down)	X	H	X	High Z	I_{CCSB} ,I_{CCSB1}
Output Disabled	H	L	H	High Z	I_{CC}
Read	H	L	L	D_{OUT}	I_{CC}
Write	L	L	X	D_{IN}	I_{CC}

Absolute Maximum Ratings:

Ambient Temperature

Under Bias.....-10°C to +80°C

Storage Temperature(plastic)....-55°C to +125°C

Voltage Relative to GND.....-0.5V to + 4.6V

Data Output Current.....50mA

Power Dissipation.....1.0W

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATING may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operation Range:

Range	Temperature	V_{CC}
Commercial	$0^{o}C$ to $+70^{o}C$	3.3V±5%

Capacitance[(1)] T_A=25°C,f=1.0MHZ :

Sym.	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN}=0V	8	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$=0V	10	pF

DC Characteristics

Sym.	Parameter	Test Conditions	Min.	Typ[1]	Max.	Unit
V_{IL}	Guaranteed Input Low Voltage [2]		-0.3	-	+0.8	V
V_{IH}	Guaranteed Input High Voltage [2]		2.0	-	V_{CC}+0.3	V
I_{LI}	Input Leakage Current	V_{CC}=Max., V_{IN}=0V to V_{CC}	-5	-	5	μA
I_{LO}	Output Leakage Current	V_{CC}=Max., $\overline{CE} \geq V_{IH}$	-5	-	5	μA
V_{OL}	Output Low Voltage	V_{CC}=Min.,I_{OL} =8mA	-	-	0.4	V
V_{OH}	Output High Voltage	V_{CC}=Min., I_{OH} =-4mA	2.4	-	-	V
I_{CC}	Operating Power Supply Current	V_{CC}=Max., $\overline{CE} \leq V_{IL}$, $I_{I/O}$=0mA., F=F_{max} [3]	-	-	-8 -10 -12 -15 110 100 90 90	mA
I_{CCSB}	Standby Power Supply Current	V_{CC}=Max., $\overline{CE} \geq V_{IH}$, $I_{I/O}$=0mA., F=F_{max} [3]	-	-	15	mA
I_{CCSB1}	Power Down Power Supply Current	V_{CC}=Max., $\overline{CE} \geq V_{CC}$.-0.2V, $V_{IN} \geq V_{CC}$. -0.2V or	-	-	2	mA

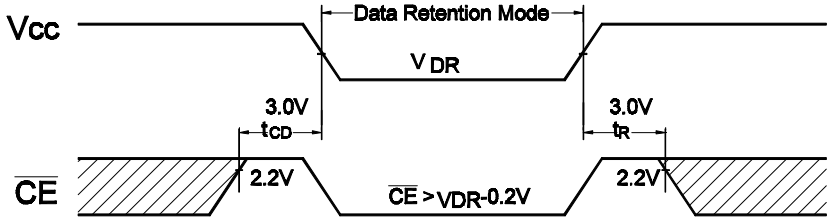
1. Typical characteristics are at V_{CC}=3.3V, T_A=25°C.
2. These are absolute values with repeat to device ground and all overshoots due to system or tester noise are included.
3. $F_{MAX}=1/t_{RC}$.

Data Retention (L version only)

Sym.	Parameter	Test Conditions	Min.	Typ[1]	Max.	Unit
V_{DR}	V_{CC} for Data retention	$\overline{CE} \geq V_{CC}$ -0.2V, $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq 0.2V$	2.0	-	3.6	V
I_{CCDR}[1]	Data Retention Current	V_{DR}=2.0V			30	μA
t_{CDR}	Chip Deselect to Data Retention Time	Retention Waveform	0	-	-	ns
t_R	Operating Recovery Time		t_{RC}[2]	-	-	ns

1. $\overline{CE} \geq V_{DR}$ -0.2V, $V_{IN} \geq V_{DR}$ -0.2V or $V_{IN} \leq 0.2V$.
2. t_{RC} =Read Cycle Time.

Low V_{CC} Data Retention Waveform (CE Controlled)



AC Test Conditions

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	3 ns
Timing Reference Level	1.5V

AC Test Loads and Waveforms

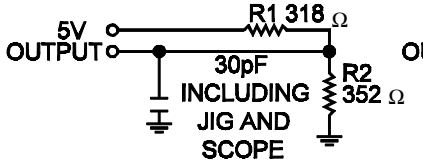


Figure 1a

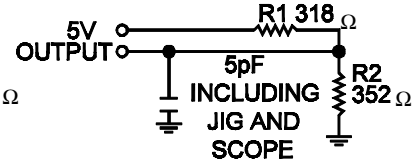
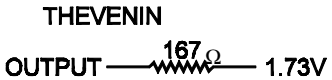


Figure 1b



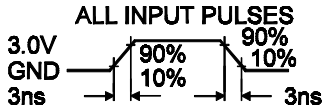


Figure 2

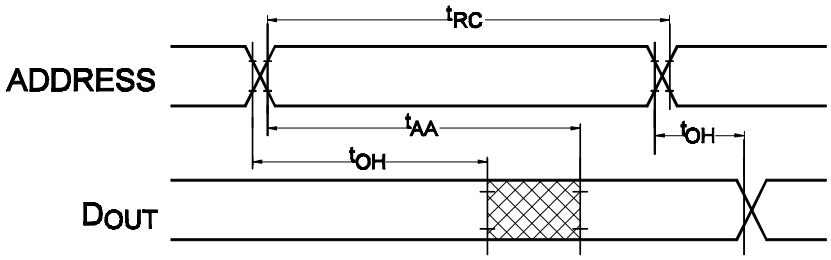
AC Electrical Characteristics (over the commercial operating range)

Read Cycle

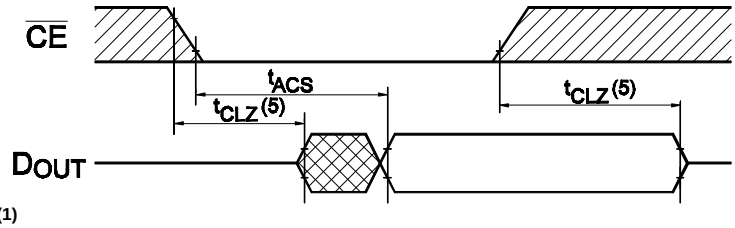
Parameter Name	Parameter	-8		-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	8		10		12		15		ns
t_{AA}	Address Access Time		8		10		12		15	ns
t_{ACS}	Chip Select Access Time,		8		10		12		15	ns
t_{OE}	Output Enable to Output Valid		5		6		7		8	ns
t_{CLZ}	Chip Select to Output Low Z, $\overline{CE}$	3		3		3		3		ns
t_{OLZ}	Output Enable to Output in Low Z	0		0		0		0		ns
t_{CHZ}	Chip Deselect to Output in High Z, $\overline{CE}$		4	0	5	0	6	0	6	ns
t_{OHZ}	Output Disable to Output in High Z		4	0	5	0	6	0	6	ns
t_{OH}	Output Hold from Address Change	3		3		3		3		ns

Switching Waveform (Read Cycle)

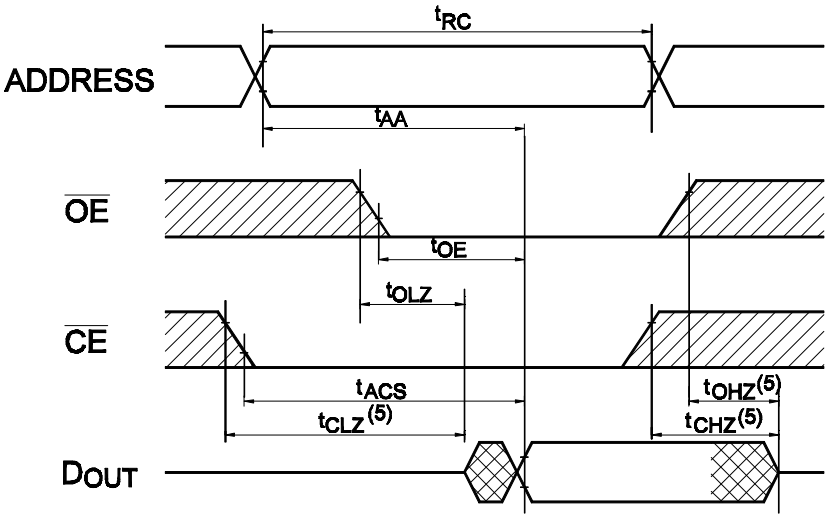
READ CYCLE1 (1,2,4)



READ CYCLE 2 (1,3,4)



READ CYCL E 3 (1)



Notes:

1. $\overline{WE}$ is High for READ Cycle.
2. Device is continuously selected $\overline{CE} \leq V_{IL}$.
3. Address valid prior to or coincident with $\overline{CE}$ transition low and/or transition high.
4. $\overline{OE} \leq V_{IL}$.
5. Transition is measured 200mV from steady state with C_L=5pF.

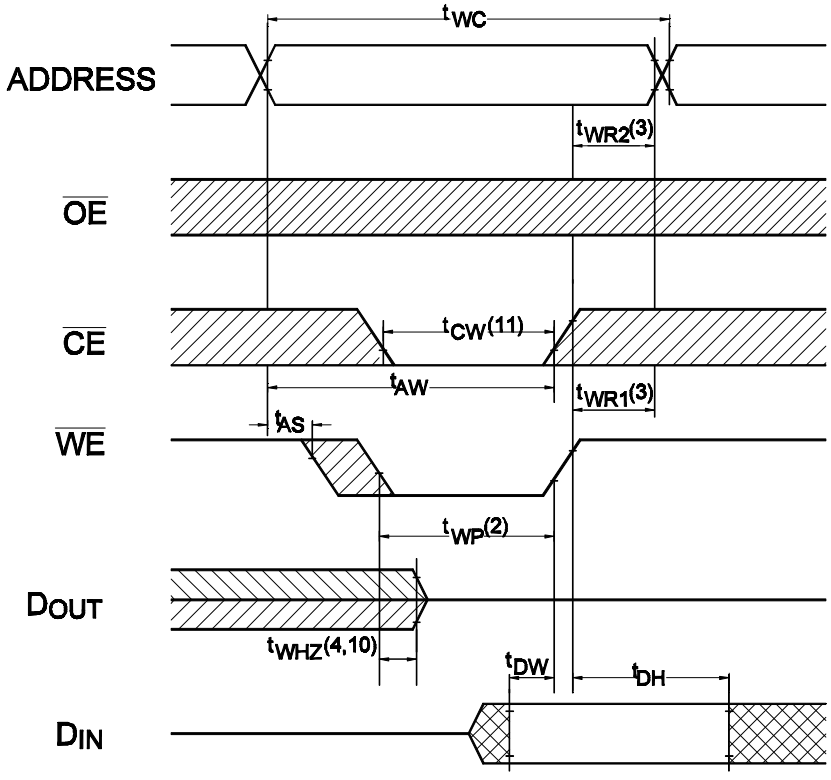
AC Electrical Characteristics (over the commercial operating range)

Write Cycle

Parameter Name	Parameter	-8		-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	8		10		12		15		ns
t_{CW}	Chip Select to End of Write	6		8		10		12		ns
t_{AS}	Address Set up Time	0		0		0		0		ns
t_{AW}	Address Valid to End of Write	6		8		10		12		ns
t_{WP}	Write Pulse Width	6		8		10		12		
t_{WR}	Write Recovery Time	0		0		0		0		ns
t_{WHZ}	Write to Output in High Z	0	4	0	5	0	6	0		ns
t_{DW}	Data to Write Time Overlap	5		6		8		10	6	ns
t_{DH}	Data Hold from Write Time	0		0		0		0		ns
t_{OW}	End of Write to Output Active	0		0		0		0		ns

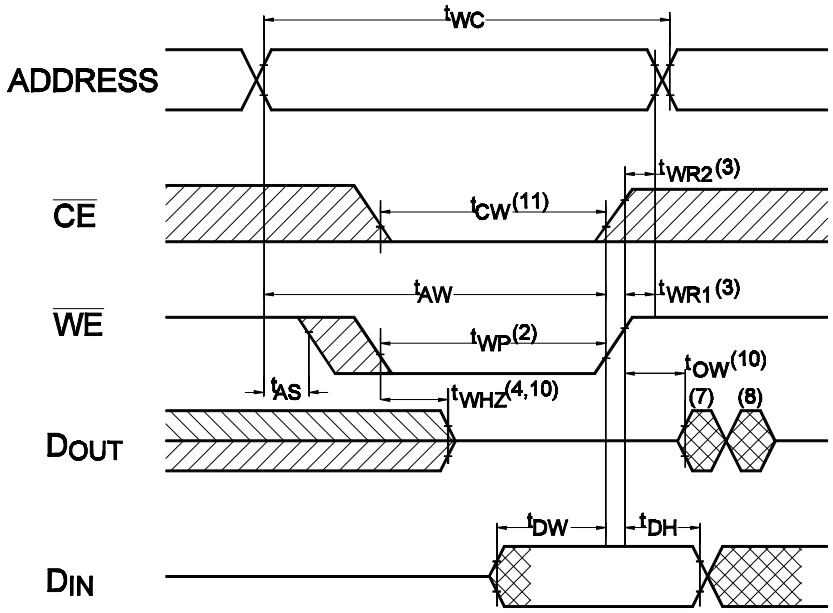
Switching Waveforms(Write Cycle)

WRITE CYCLE 1(1)



Switching Waveform (Write Cycle)

WRITE CYCLE 2[1,6]



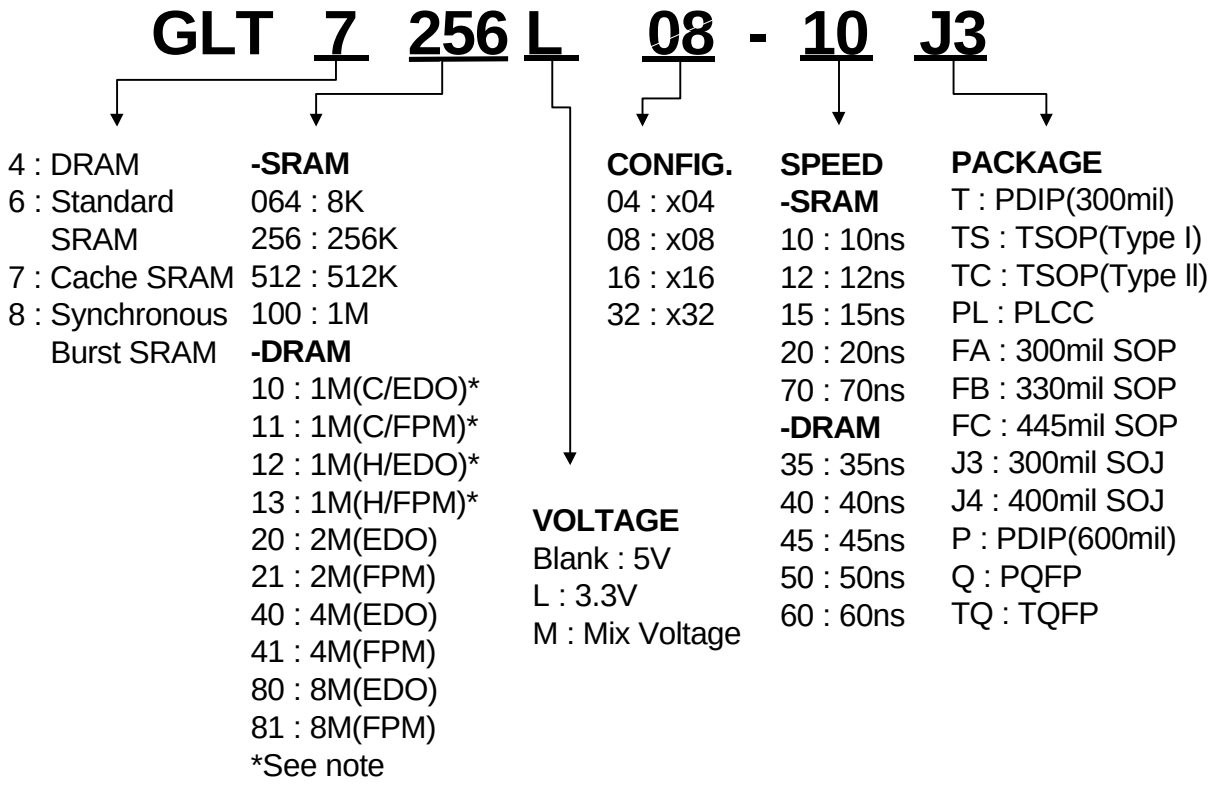
Note:

1. $\overline{WE}$ must be high during address transitions.
2. The internal write time of the memory is defined by the overlap $\overline{CE}$ low and WE low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. T_{WR} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high at the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE}=V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{CE}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ±200mV from steady state with C_L=5pF.
11. t_{CW} is measured from $\overline{CE}$ going low to the end of write.

Ordering Informstion

Part Number	Cycle Time	Power	Package
GLT7256L08-8J3	8ns	Low Power	SOJ 300mil 28L
GLT7256L08-10J3	10ns	Low Power	SOJ 300mil 28L
GLT7256L08-12J3	12ns	Low Power	SOJ 300mil 28L
GLT7256L08-15J3	15ns	Low Power	SOJ 300mil 28L
GLT7256L08-8TS	8ns	Low Power	TSOP
GLT7256L08-10TS	10ns	Low Power	TSOP
GLT7256L08-12TS	12ns	Low Power	TSOP
GLT7256L08-15TS	15ns	Low Power	TSOP

Parts Numbers (Top Mark) Definition :



Note : C→CDROM , H→HDD.

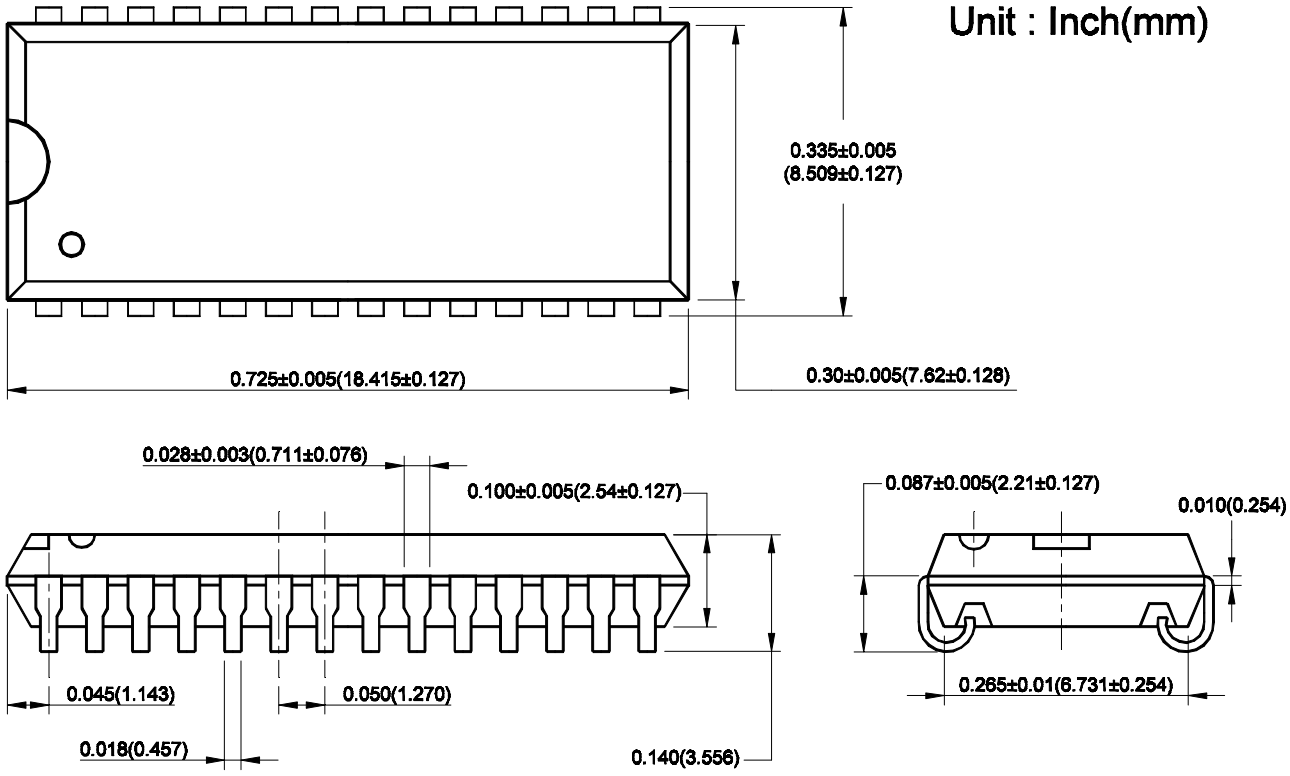
Example :

1.GLT710008-15T 1Mbit(128Kx8)15ns 5V SRAM PDIP(300mil)Package type.

2.GLT44016-40J4 4Mbit(256Kx16)40ns 5V DRAM SOJ(400mil)Package type.

Package Information

300mil 28 pin Small Outline J-form Package (SOJ)



TSOP 28 pin Plastic Dual Inline Package