Remote/Local Temperature Sensor, 2 Fan Controllers with SMBus Serial Interface and System Reset Circuit

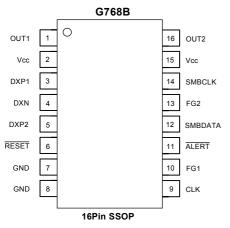
Features

- Measures Two Remote and One Local Temperatures
- No Calibration Required
- SMBus 2-Wire Serial Interface
- Programmable Under/Over-temperature Alarms
- Supports SMBus Alert Response
- Accuracy: ±5°C (-40°C to + 125°C, remote) ±3°C (+60°C to + 100°C, remote)
- +4.5V to +5.5V Supply Range
- Constant Fan Speed Control
- Built-in MOSFET switch
- Internal short-circuit protection
- PWM control for stable operation
- Watchdog for fan control
- Precision Monitoring of 5V Power-Supply Voltage
- 140ms Min Power-On Reset Pulse Width RESET Output
- Guaranteed RESET Valid to V_{cc}=1V
- Power Supply Transient Immunity
- No External Components needed for reset function
- Small, 16-Pin SSOP Package

Applications

- Desktop and Notebook
- Central Office Computers
- Telecom Equipment
- Smart Battery Packs
- Test and Measurement
- LAN Servers
- Multi-Chip Modules
- Industrial Controls

Pin Configuration



General Description

The G768B contains a precise digital thermometer, 2 fan controllers, and a system-reset circuit.

The G768B is backward compatible with G768, Except that there is an additional watchdog function. This function prevents fan from being out of control when system fails.

The thermometer reports the temperature of 2 remote sensors and its own package. The remote sensors are diode-connected transistors typically a low-cost, easily mounted 2N3904 NPN type that replace conventional thermistors or thermocouples. Remote accuracy is $\pm 5^{\circ}$ C for multiple transistor manufacturers, with no calibration needed. The remote channel can also measure the die temperature of other ICs, such as microprocessors, that contain an on-chip, diode-connected transistor.

The 2-wire serial interface accepts standard System Management Bus (SMBusTM) Write Byte, Read Byte, Send Byte, and Receive Byte commands to program the alarm thresholds and to read temperature data. The data format is 7 bits plus sign, with each bit corresponding to 1° C, in two's-complement format. Measurements can be done automatically and autonomously, with the conversion rate programmed by the user or programmed to operate in a single-shot mode. The adjustable rate allows the user to control the supply-current drain.

G768B also contains a 2-channel fan speed controller. It connects directly to the fans and performs closed-loop control of the fan speed independently. The only external component required is a 10μ F capacitor per channel. It determines the current fan speed based on the fan rotation pulses and an externally supplied clock. (*To be continued*)

Ordering Information

PART*	TEMP. RANGE	PIN-PACKAGE
G768B	-10°C to +85°C	16SSOP

<u>G768B</u>

It uses pulse width modulation (PWM) method and an on-chip MOSFET to control the fan speed to $\pm 2\%$ of the programmed speed.

The desired fan speed is also programmed via $SMBus^{TM}$. The actual fan speed and fan status can be read via the $SMBus^{TM}$. Short-circuit protection is implemented to prevent damages to the fan and this IC itself. The G768B also turns on the fans by hardware watchdog system. The fan controller would fully turn on both fans when one of the following conditions happens.

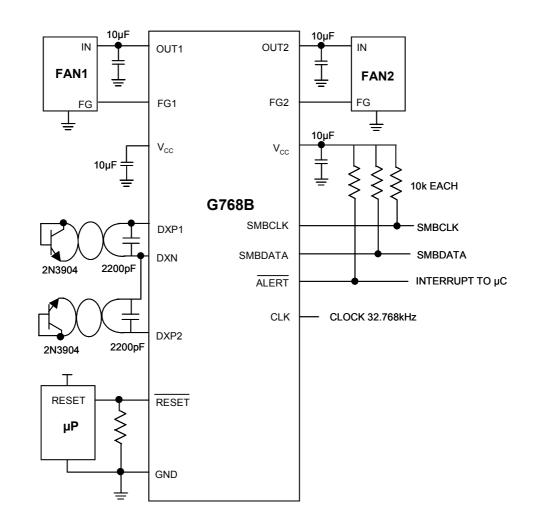
1.when either of the remote temperature is higher than its own $T_{\text{MAX}}.$

2.when either of these two remote diodes is open.

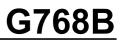
3.when both remote diodes are short

The G768B also contains a microprocessor (μ P) supervisory circuit used to monitor the power supplies in μ P and digital systems. They provide excellent circuit reliability and low cost by eliminating external components and adjustments when used with 5V-powered circuits. This circuit asserts a reset signal whenever the V_{CC} supply voltage declines below a preset threshold, keeping it asserted for at least 140ms after V_{CC} has risen above the reset threshold. The G768B has an active-low RESET output. The reset comparator is designed to ignore fast transients on V_{CC}. Reset threshold of this circuit is set to 4.38V.

The G768B is available in a small, 16-pin SSOP surface-mount package.



Typical Operating Circuit



Absolute Maximum Ratings

Vcc to GND0.3V to +6V
DXP1, DXP2 to GND0.3V to (Vcc + 0.3V)
DXN to GND0.3V to +0.8V
SMBCLK, SMBDATA, ALERT to GND0.3V to +6V
SMBDATA, ALERT Current1mA to +50mA
DXN Current±1mA
ESD Protection (SMBCLK, SMBDATA, ALERT , hu- man body model)4000V

ESD Protection (other pins, human body model) 2000//

model).2000V
Continuous Power Dissipation (T_A = +70°C) SSOP
(de-rate 8.30mW/°C above +70°C)667mW
Operating Temperature Range10°C to +85°C
Junction Temperature+150°C
Storage temperature Range65°C to +165°C
Lead Temperature (soldering,10sec)+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(Vcc = + 5V, T_A = 60°C, unless otherwise noted.)

PARAMETER	CONDI	TIONS	MIN	TYP	MAX	UNITS
Temperature Sensor	·					
Temperature Resolution(Note 1)	Monotonicity guaranteed		8			Bits
Temperature Error, Remote Diode (Notes 2	T _R = 0°C to +125°C		-5		5	°C
and 3)	T _R = 60°C to +100°C		-3		3	ι, C
Temperature Error, Local Diode (Notes 1 and 2)	Including long-term drift $T_A = +60^{\circ}C$ to $+100^{\circ}C$		-3.5		3.5	°C
Supply-Voltage Range			4.5	5	5.5	V
Under-voltage Lockout Threshold	Vcc input, disables A/D conve	ersion, rising edge	2.6	2.8	2.95	V
Under-voltage Lockout Hysteresis				50		mV
Power-On Reset Threshold	Vcc , falling edge		1.0	1.7	2.5	V
POR Threshold Hysteresis				50		mV
	Logic inputs forced to Vcc or	SMBus static		3	10	
Standby Supply Current	GND	Hardware or software standby, SMBCLK at 10kHz		200		μA
	Auto-convert mode, average	0.25 conv/sec		250	300	
Average Operating Supply Current	measured over 4sec. Logic inputs forced to Vcc or GND	2.0 conv/sec		300	350	μA
Conversion Time	From stop bit to conversion c	omplete(all channels)	94	125	156	ms
Conversion Rate Timing Error	Auto-convert mode		-25		25	%
		High level	120	160	200	
Remote-Diode Source Current	DXP forced to 1.5V	Low level	15	20	25	μA
Fan Controller						
Supply voltage	Vc	C	4.5	5	5.5	V
Shutdown current	Both fans' sp	peed = 0rpm		2	5	μA
MOSFET on resistance	Each cl	hannel		0.2	0.25	Ω
Short-circuit current limit	Each channel			0.5		А
Input logic low	VIL				0.8	V
Input logic high	VIH		2.4			V
Average Output current	Each cl	hannel			350	mA
FG input Positive-going threshold voltage	V _{CC} =	=5V		1.8		V
FG input Negative-going threshold voltage	V _{CC} =	=5V		0.7		V
FG input Hysteresis voltage	V _{CC} =	=5V		1.1		V

Electrical Characteristics (continued)

(Vcc = + 5V, T_A = 60°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SMBus Interface					
Logic Input High Voltage	SMBCLK, SMBDATA; Vcc = 4.5V to 5.5V	2.4			V
Logic Input Low Voltage	SMBCLK, SMBDATA; Vcc = 4.5V to 5.5V			0.8	V
Logic Output Low Sink Current	ALERT , SMBDATA forced to 0.4V	6			mA
ALERT Output High Leakage Current	ALERT forced to 5.5V			1	μA
Logic Input Current	Logic inputs forced to Vcc or GND	-2		2	μA
SMBus Input Capacitance	SMBCLK, SMBDATA		5		pF
SMBus Clock Frequency	(Note 4)	DC		100	kHz
SMBCLK Clock Low Time	t _{LOW} , 10% to 10% points	4.7			μs
SMBCLK Clock High Time	t _{ніGH} , 90% to 90% points	4			μs
SMBus Start-Condition Setup Time		4.7			μs
SMBus Repeated Start-Condition	t _{SU: STA} , 90% to 90% points	500			ns
Setup Time					
SMBus Start-Condition Hold Time	$t_{HD: STA}$, 10% of SMBDATA to 90% of SMBCLK	4			μs
SMBus Start-Condition Setup Time	$t_{\text{SD: STO}}$, 90% of SMBDATA to 10% of SMBDATA	4			μs
SMBus Data Valid to SMBCLK Ris-	$t_{\text{SU: DAT}}$, 10% or 90% of SMBDATA to 10% of	800			ns
ing-Edge Time	SMBCLK				
SMBus Data-Hold Time	t _{HD : DAT} (Note 5)	0			μs
SMBCLK Falling Edge to SMBus	Master clocking in data			1	μs
Data-Valid Time					

Electrical Characteristics (continued)

(V_{cc} =full range, T_A= 60°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Reset Threshold	V _{TH}		4.2	4.4	4.5	V
Reset Active Timeout Period				340		ms
RESET Output Voltage Low	Vol	$V_{CC}=V_{TH}$ min $I_{SINK}=3.2$ mA			0.4	V
RESET Output Voltage High	V _{OH}	V _{CC} >V _{TH} max I _{SOURCE} =5.0mA	V _{cc} -1.5			V

Note 1: Guaranteed but not 100% tested.

- Note 2: Quantization error is not included in specifications for temperature accuracy. For example, if the G768B device temperature is exactly +66.7°C, or +68°C (due to the quantization error plus the +1/2°C offset used for rounding up) and still be within the guaranteed ±3°C error limits for the +60°C to +100°C temperature range. See Table3.
- Note 3: A remote diode is any diode-connected transistor from Table1. T_R is the junction temperature of the remote diode. See Remote Diode Selection for remote diode forward voltage requirements.
- Note 4: The SMBus logic block is a static design that works with clock frequencies down to DC. While slow operation is possible, it violates the 10kHz minimum clock frequency and SMBus specifications, and may monopolize the bus.
- Note 5: Note that a transition must internally provide at least a hold time in order to bridge the undefined region (300ns max) of SMBCLK's falling edge.

Pin Description

PIN	NAME	FUNCTION
1	OUT1	PWM output, connect to fan 1
2,15	Vcc	Supply Voltage Input , 4.5V to 5.5V. Bypass to GND with a 0.1µF capacitor.
3	DXP1	Combined Current Source and A/D Positive Input for remote-diode channel 1. Do not leave DXP1 floating; tie DXP1 to DXN if no remote diode on channel 1 is used. Place a 2200pF capacitor between DXP1 and DXN for noise filtering.
4	DXN	Combined Current Sink and A/D Negative Input. DXN is common negative node of both remote diodes on channel 1 and 2. The traces of DXP1-DXN and DXP2-DXN pairs should be routed independently. The common DXN should be connected together as close as possible to the IC. DXN is internally connected to the GND pin for signal ground use.
5	DXP2	Combined Current Source and A/D Positive Input for remote-diode channel 2. Do not leave DXP2 floating; tie DXP2 to DXN if no remote diode on channel 2 is used. Place a 2200pF capacitor between DXP2 and DXN for noise filtering.
6	RESET	$\overline{\text{RESET}}$ Output remains low while V _{CC} is below the reset threshold, and for 240ms after V _{CC} rises above the reset threshold.
7,8	GND	Ground
9	CLK	Clock input for fan speed measurement.
10	FG1	Fan1 pulse input.
11	ALERT	SMBus Alert (interrupt) Output, open drain.
12	SMBDATA	SMBus Serial-Data Input / Output, open drain.
13	FG2	Fan2 pulse input.
14	SMBCLK	SMBus Serial-Clock Input.
16	OUT2	PWM output, connect to fan 2.

Detailed Description

The G768B (patents pending) is a 4-in-1 IC. It consists of one temperature sensor, 2 fan speed controllers and provides system-reset function.

The temperature sensor is designed to work in conjunction with an external micro-controller (μ C) or other intelligence in thermostatic, process-control, or monitoring applications. The μ C is typically a power-management or keyboard controller, generating SMBus serial commands by "bit-banging" general-purpose input-output (GPIO) pins or via a dedicated SMBus interface block.

Essentially a 12-bit serial analog-to-digital converter (ADC) with a sophisticated front end, the G768B contains a switched current source, a multiplexer, an ADC, an SMBus interface, 2 fan controllers, a reset circuit and associated control logic (Figure 1).

Temperature data from the ADC is loaded into two data registers, where it is automatically compared with data previously stored in four over/under-temperature alarm registers.

ADC and Multiplexer

The ADC is an averaging type that integrates over a 60ms period (each channel, typical), with excellent noise rejection.

The multiplexer automatically steers bias currents through the remote and local diodes, measures their forward voltages, and computes their temperatures. All channels are converted automatically once the conversion process has started, either in free-running or single-shot mode. If one of the three channels is not used, the device still performs all measurements, and the user can simply ignore the results of the unused channel. If the remote diode channel is unused, tie DXPx to DXN rather than leaving the pins open.

The DXN input is internally connected to the ground node inside the chip to set up the analog to digital (A/D) inputs for a differential measurement. The worst-case DXP-DXN differential input voltage range is 0.25V to 0.95V.

Excess resistance in series with the remote diode causes about +1/2°C error per ohm. Likewise, 200μ V of offset voltage forced on DXP-DXN causes about 1°C error.

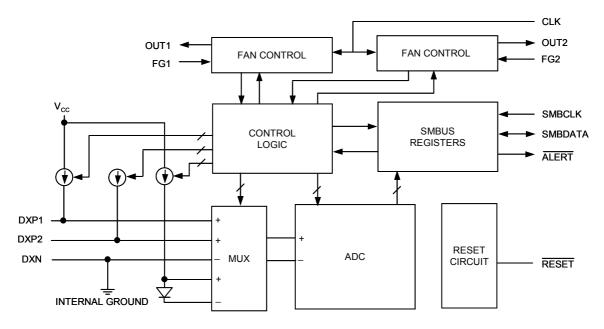


Fig 1. Functional Diagram

A/D Conversion Sequence

If a Start command is written (or generated automatically in the free-running auto-convert mode), all three channels are converted, and the results of all measurements are available after the end of conversion. A BUSY status bit in the status byte shows that the device is actually performing a new conversion; however, even if the ADC is busy, the results of the previous conversion are always available.

Remote-Diode Selection

Temperature accuracy depends on having a good-quality, diode-connected small-signal transistor. Accuracy has been experimentally verified for all of the devices listed in Table 1. The G768B can also directly measure the die temperature of CPUs and other integrated circuits having on-board temperature-sensing diodes. The transistor must be a small-signal type with a relatively high forward voltage; otherwise, the A/D input voltage range can be violated. The forward voltage must be greater than 0.25V at 10µA; check to ensure this is true at the highest expected temperature. The forward voltage must be less than 0.95V at 200A; check to ensure this is true at the lowest expected temperature. Large power transistors don't work at all. Also, ensure that the base resistance is less than 100 Ω . Tight specifications for forward current gain (+50 to +150, for example) indicate that the manufacturer has good process controls and that the devices have consistent VBE characteristics.

Thermal Mass and Self-Heating

Thermal mass can seriously degrade the G768B's effective accuracy. The thermal time constant of the SSOP-16 package is about 140sec in still air. For the G768B junction temperature to settle to within +1°C after a sudden +100°C change requires about five time constants or 12 minutes. The use of smaller packages for remote sensors, such as SOT23s, improves the situation. Take care to account for thermal gradients between the heat source and the sensor, and ensure that stray air current across the sensor package do not interfere with measurement accuracy.

Self-heating can significantly affect the measurement accuracy. Remote-sensor self-heating due to the diode current source is negligible. For the local diode, the worst-case error occurs when auto converting at the fastest rate and simultaneously sinking maximum current at the ALERT output, and both fans are working at low speeds.

Table 1. Remote-Sensor Transistor Manufacturers

MANUFACTURER	MODEL NUMBER
Philips	PMBS 3904
Motorola(USA)	MMBT3904
National Semiconductor(USA)	MMBT3904

Note:Transistors must be diode-connected (base short -ed to collector).

<u>G768B</u>

ADC Noise Filtering

The ADC is an integrating type with inherently good noise rejection, especially of low-frequency signals such as 60Hz/120Hz power-supply hum. Micro-power operation places constraints on high-frequency noise rejection; therefore, careful PC board layout and proper external noise filtering are required for high-accuracy remote measurements in electrically noisy environments.

High-frequency EMI is best filtered at DXP and DXN with an external 2200pF capacitor. This value can be increased to about 3300pF(max), including cable capacitance. Higher capacitance than 3300pF introduces errors due to the rise time of the switched current source.

Nearly all noise sources tested cause the ADC measurements to be higher than the actual temperature, typically by +1°C to 10°C, depending on the frequency and amplitude (see Typical Operating Characteristics).

PC Board Layout

Place the G768B as close as practical to the remote diode. In a noisy environment, such as a computer motherboard, this distance can be 4 in. to 8 in. (typical) or more as long as the worst noise sources (such as CRTs, clock generators, memory buses, and ISA/PCI buses) are avoided.

Do not route the DXP-DXN lines next to the deflection coils of a CRT. Also, do not route the traces across a fast memory bus, which can easily introduce +30°C error, even with good filtering, Otherwise, most noise sources are fairly benign.

Route the DXP and DXN traces in parallel and in close proximity to each other, away from any high-voltage traces such as +12VDC. Leakage currents from PC board contamination must be dealt with carefully, since a $20M\Omega$ leakage path from DXP to ground causes about +1°C error.

Route the 2 pairs of DXP1-DXN and DXP2-DXN traces independently (Figure 2a). Connect the common DXN as close as possible to the DXN pin on IC (Figure 2a).

Connect guard traces to GND on either side of the DXP-DXN traces (Figure 2b). With guard traces in place, routing near high-voltage traces is no longer an issue.

Route through as few vias and crossunders as possible to minimize copper/solder thermocouple effects.

When introducing a thermocouple, make sure that both the DXP and the DXN paths have matching thermocouples. In general, PC board- induced thermocouples are not a serious problem, A copper-solder thermocouple exhibits $3\mu V/^{\circ}C$, and it takes about $200\mu V$ of voltage error at DXP-DXN to cause a +1°C measurement error. So, most parasitic thermocouple

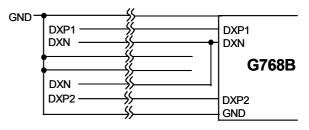
errors are swamped out.

Use wide traces. Narrow ones are more inductive and tend to pick up radiated noise. The 10 mil widths and spacing recommended on Figure 2 aren't absolutely necessary (as they offer only a minor improvement in leakage and noise), but try to use them where practical.

Keep in mind that copper can't be used as an EMI shield, and only ferrous materials such as steelwork will. Placing a copper ground plane between the DXP-DXN traces and traces carrying high-frequency noise signals do not help reduce EMI.

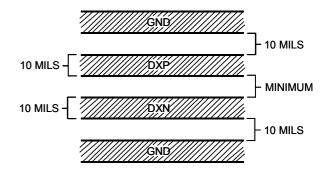
PC Board Layout Checklist

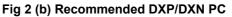
- Place the G768B close to a remote diode.
- Keep traces away from high voltages (+12V bus).
- Keep traces away from fast data buses and CRTs.
- Use recommended trace widths and spacing.
- Place a ground plane under the traces
- Use guard traces flanking DXP and DXN and connecting to GND.
- Route two DXPx-DXN pairs independently
- Connect the common DXN as close as possible to the DXN pin on IC.
- Place the noise filter and the 0.1F Vcc bypass capacitors close to the G768B.



Chip Boundary

 Fig 2(a) Connect the common DXN as close as possible to the DXN pin on IC.





Twisted Pair and Shielded Cables

For remote-sensor distances longer than 8 in., or in particularly noisy environments, a twisted pair is recommended. Its practical length is 6 feet to 12feet (typical) before noise becomes a problem, as tested in a noisy electronics laboratory. For longer distances, the best solution is a shielded twisted pair like that used for audio microphones. Connect the twisted pair to DXP and DXN and the shield to GND, and leave the shield's remote end unterminated.

Excess capacitance at DX_limits practical remote sensor distances (see Typical Operating Characteristics), For very long cable runs, the cable's parasitic capacitance often provides noise filtering, so the 2200pF capacitor can often be removed or reduced in value. Cable resistance also affects remote-sensor accuracy; 1Ω series resistance introduces about + 1°C error.

Low-Power Standby Mode

Standby mode disables the ADC and reduces the supply-current drain to less than 10 μ A. Enter standby mode via the RUN/STOP bit in the configuration byte register. In standby mode, all data is retained in memory, and the SMB interface is alive and listening for reads and writes. This is valid for temperature sensor only.

Standby mode is not a shutdown mode. With activity on the SMBus, extra supply current is drawn (see Typical Operating Characteristics). In software standby mode, the G768B can be forced to perform temperature measurement via the one-shot command, despite the RUN/STOP bit being high.

Supply-current drain during the 125ms conversion period is always about 500 μ A. Slowing down the conversion rate reduces the average supply current (see Typical Operating Characteristics). In between conversions, the instantaneous supply current is about 25 μ A due to the current consumed by the conversion rate timer. In standby mode, supply current drops to about 3 μ A. at very low supply voltages (under the power-on-reset threshold).

Fan Controller

The fan speed is measured by counting the number of the CLK pin period between the rising edges of two fan speed pulses on FG pin. In this way, we are actually measuring the period of the fan speed. To avoid the cost of doing division to obtain the speed, this count number, N, is used in the PWM control algorithm, thus, the desired fan speed should be programmed by writing the corresponding count number. The count number is given by: N = (CLK x 30) / (rpm x P)

N : Count Number P : FG pulses number per revolution of fan. For CLK = 32768Hz, P = 2 \Rightarrow N = 491520 / rpm For CLK = 16384Hz, P = 2 \Rightarrow N = 245762 / rpm Some selected count numbers are shown below

Table 2. Count numbers for P=2

rpm	CLK=32768Hz	CLK=16384Hz
968		254
1935	35 254 1	
2000	246	123
3000	164	82
4000	123	61
5000	98	49
6000	82	41
7000	70	35
8000	61	31
9000	55	27
10000	49	25
20000	25	12
30000	16	8

To stop the fan, program the fan speed register to 255. This also makes the fan controller into power saving mode.

Controlling Fan at Lower Speed

For stably controlling fans at lower rotataion speed, three schemes are recommended as below:

- 1.Use larger decoupling capacitors between FAN_OUT and GND.
- 2.Shunt a capacitor of 1µF-2µF on FG pin to GND.
- 3.Use fans with open-collector FG outputs.

When controlling fans under lower rotation speed, the output voltage of FAN_OUT would be too low for fan to generate recognizable FG signals.

Using decouple capacitors on FAN_OUT and FG is to increase the SNR on FG pins. While Using fans with open-collector FG outputs can thoroughly solve the problem, because the logic high level of FG would be fixed to 5V.

Reset Immunity Negative-Going V_{cc} Transients

In addition to issuing a reset to the microprocessor (μ P) during power-up, power-down, and brownout conditions, the G768B is relatively immune to short duration negative-going V_{CC} transients (glitches).

Typically, for the G768B, a V_{CC} transient that goes 100mV below the reset threshold and lasts 20µs or less will not cause a reset pulse. A 0.1μ F bypass capacitor mounted as close as possible to the V_{CC} pin provides additional transient immunity.

<u>G768B</u>

Ensuring a Valid Reset Output Down to $V_{cc} = 0V$

When V_{CC} falls below 1V, the G768B RESET output no longer sinks current-it becomes an open circuit. Therefore, high-impedance CMOS logic inputs connected to RESET can drift to undetermined voltages. This presents no problem in most applications, since most μ P and other circuitry is inoperative with V_{CC} below 1V. However, in applications where RESET must be valid down to 0V, adding a pull-down resistor to RESET causes any stray leakage currents to flow to ground, holding RESET low (Figure 3). R1's value is not critical; 100k Ω is large enough not to load RESET and small enough to pull RESET to ground.

Interfacing to Ps with Bi-directional Reset Pins

Ps with bi-directional reset pins (such as the Motorola 68HC11 series) can connect to the G768B reset output. If, for example, the G768B RESET output is asserted high and the μ P wants to pull it low, indeterminate logic levels may result. To correct this, connect a 4.7k Ω resistor between the G768B RESET output and the μ P reset I/O (Figure 4). Buffer the G768B RESET output to other system components.

Benefits of Highly Accurate Reset Threshold

Most μ P supervisor Ics have reset threshold voltages between 5% and 10% below the value of nominal supply voltages. This ensures a reset will not occur within 5% of the nominal supply, but will occur when the supply is 10% below nominal.

When using Ics rated at only the nominal supply $\pm 5\%$ this leaves a zone of uncertainty where the supply is between 5% and 10% low, and where the reset may or may not be asserted.

The G768B use highly accurate circuitry to ensure that reset is asserted close to the 5% limit, and long before the supply has declined to 10% below nominal.

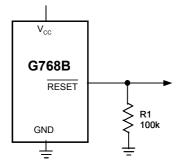


Fig 3. RESET Valid to V_{cc} = Ground Circuit

SMBus Digital Interface

From a software perspective, the G768B appears as a set of byte-wide registers that contain temperature data, alarm threshold values, fan speed data, or control bits, A standard SMBus 2-wire serial interface is used to read temperature data and write control bits and alarm threshold data. Each A/D and fan control channel within the device responds to the same SMBus slave address for normal reads and writes.

The G768B employs four standard SMBus protocols: Write Byte, Read Byte, Send Byte, and Receive Byte (Figure 5). The shorter Receive Byte protocol allows quicker transfers, provided that the correct data register was previously selected by a Read Byte instruction. Use caution with the shorter protocols in multi-master systems, since a second master could over-write the command byte without informing the first master.

The temperature data format is 7bits plus sign in twos-complement form for each channel, with each data bit representing $1^{\circ}C$ (Table3), transmitted MSB first. Measurements are offset by $+1/2^{\circ}C$ to minimize internal rounding errors; for example, $+99.6^{\circ}C$ is reported as $+100^{\circ}C$.

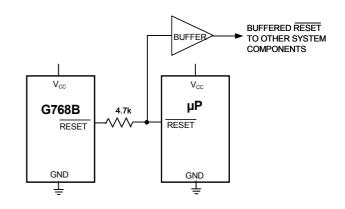


Fig 4. Interfacing to µPs with Bi-directional Reset I/O

S	Add	ress	WR	ACK	Con	nmand	ACK	DA	ATA	ACK		Ρ
	71	oits			8	bits		8	bits			1
ave Ad	dress:	equivale	ent to chip	o-select line of	f a 3-wi	re interf	ace					
		•	•	egister you, ar								
	•			ster set by the		•	(to set three	holds,	configu	ration mas	sks, an	d
-	samp	ling rate)	2					Ū			
ad Du	o Eorm	- -										
	e Form ddress	at WR	ACK	Command	ACK	S	Address	RD	ACK	DATA		Р
<u>5</u> A	7 bits	VVIN	ACK	8 bits	ACK	3			ACK			F
				p- select line			7 bits			8 bits		
ave Ad ata byt	ldress: e: reads	repeate from th	d due to	egister you, a change in dat r set by the co	a-flow o	directior						
lave Ad ata byt end By	ldress:	repeate from th at	d due to le registe	change in dat r set by the co	a-flow o omman	directior d byte	1	and		CK I)
lave Ad ata byt	ldress: e: reads	repeate from th at Addre	d due to le registe ss	change in dat	a-flow o omman	directior	Comm		A	СК	F	>
lave Ac ata byt end By S	Idress: e: reads te Form	repeate from th aat Addre 7 bits	d due to le registe ss	change in dat r set by the co WR	a-flow o omman	direction d byte	Comm 8 bit	3		СК	F	9
lave Ac ata byt end By S	Idress: e: reads te Form	repeate from th aat Addre 7 bits	d due to le registe ss	change in dat r set by the co	a-flow o omman	direction d byte	Comm 8 bit	3		СК	F)
lave Ac eata byte end By S S	Idress: e: reads te Form	repeate from th at Addre 7 bits sends	d due to le registe ss	change in dat r set by the co WR	a-flow o omman	direction d byte	Comm 8 bit	3		СК	F	9
lave Ac eata byte end By S S	Idress: e: reads te Form	repeate from th at Addre 7 bits sends	d due to le registe ss command	change in dat r set by the co WR	a-flow o omman usually	direction d byte	Comm 8 bit	comma	and	СК	F	
ata byt end By S commar	Idress: e: reads te Form	repeate from th at Addre 7 bits sends ormat	d due to le registe ss command ss	change in dat r set by the co WR d with no data	a-flow o omman usually	directior d byte ACK y used f	Comm 8 bits or one-shot	s comma	and		-	
ata byt end By S commar ecceive S	Idress: e: reads te Form nd Byte: Byte Fo	repeate from th at Addre 7 bits sends ormat Addre 7 bits	d due to se registe ss command ss	change in dat r set by the co WR d with no data	a-flow opmman pmman usually A	directior d byte ACK y used f	Comm 8 bits or one-shot Data 8 bits	s comma a	and		-	
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TEMP.	ROUND	DIGIT	AL OUTP	UT
(°C)	TEMP.	DA	ATA BITS	
(0)	(°C)	SIGN	MSB	LSB
+130.00	+127	0	111	1111
+127.00	+127	0	111	1111
+126.50	+127	0	111	1111
+126.00	+126	0	111	1110
+25.25	+25	0	001	1001
+0.50	+1	0	000	0001
+0.25	+0	0	000	0000
+0.00	+0	0	000	0000
-0.25	+0	0	000	0000
-0.50	+0	0	000	0000
-0.75	-1	1	111	1111
-1.00	-1	1	111	1111
-25.00	-25	1	110	0111
-25.50	-25	1	110	0110
-54.75	-55	1	100	1001
-55.00	-55	1	100	1001
-65.00	-65	1	011	1111
-70.00	-65	1	011	1111

Table 3. Data Format (Twos-Complement)

Alarm Threshold Registers

Four registers store alarm threshold data, with high-temperature (THIGH) and low-temperature (TLOW) registers for each A/D channel. If either measured temperature equals or exceeds the corresponding alarm threshold value, an ALERT interrupt is asserted.

The power-on-reset (POR) state of both THIGH registers is full scale (0111 1111, or +127°C). The POR state of both TLOW registers is 1100 1001 or -55°C.

Diode Fault Alarm

There is a continuity fault detector at DXP that detects whether the remote diode has an open-circuit condition. At the beginning of each conversion, the diode fault is checked, and the status byte is updated. This fault detector is a simple voltage detector; if DXP rises above V_{CC} - 1V (typical) due to the diode current source, a fault is detected. Note that the diode fault isn't checked until a conversion is initiated, so immediately after power-on reset the status byte indicates no fault is present, even if the diode path is broken.

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If the remote channel is shorted (DXP to DXN or DXP to GND), the ADC reads 0000 0000 so as not to trip either the THIGH or TLOW alarms at their POR settings. In applications that are never subjected to 0°C in normal operation, a 0000 0000 result can be checked to indicate a fault condition in which DXP is accidentally short circuited. Similarly, if DXP is short circuited to V_{CC}, the ADC reads +127°C for both remote and local channels, and the device alarms.

ALERT Interrupts

The ALERT interrupt output signal is latched and can only be cleared by reading the Alert Response address. Interrupts are generated in response to THIGH and TLOW comparisons and when the remote diode is disconnected (for continuity fault detection). The interrupt does not halt automatic conversions; new temperature data continues to be available over the SMBus interface after ALERT is asserted. The interrupt output rupt output pin is open-drain so that device can share a common interrupt line. The interrupt rate can never exceed the conversion rate.

The interface responds to the SMBus Alert Response address, an interrupt pointer return-address feature (see Alert Response Address section). Prior to taking corrective action, always check to ensure that an interrupt is valid by reading the current temperature.

Alert Response Address

The SMBus Alert Response interrupt pointer provides quick fault identification for simple slave devices that lack the complex, expensive logic needed to be a bus master. Upon receiving an $\overrightarrow{\text{ALERT}}$ interrupt signal, the host master can broadcast a Receive Byte transmission to the Alert Response slave address (0001 100). Then any slave device that generated an interrupt attempts to identify itself by putting its own address on the bus.

Table 4.	. Command-Byte Bit Ass	ignments
----------	------------------------	----------

REGISTER	COMMAND	POR STATE	FUNCTION	
RRTE2	00h	0000 0000b	Read 2nd remote temperature: returns latest temperature	
RRTE1	01h	0000 0000b	Read 1st remote temperature: returns latest temperature	
RSL	02h	N/A	Read status byte (flags, busy signal)	
RCL	03h	0000 0000b	Read configuration byte	
RCRA	04h	0000 0010b	Read conversion rate byte	
RRHI2	05h	0111 1111b (127)	Read 2nd remote THIGH limit	
RRLS2	06h	1100 1001b(-55)	Read 2nd remote TLOW limit	
RRHI1	07h	0111 1111b (127)	Read 1st remote THIGH limit	
RRLS1	08h	1100 1001b (-55)	Read 1st remote TLOW limit	
WCA	09h	N/A	Write configuration byte	
WCRW	0Ah	N/A	Write conversion rate byte	
WRHA2	0Bh	N/A	Write 2nd remote THIGH limit	
WRLN2	0Ch	N/A	Write 2nd remote TLOW limit	
WRHA1	0Dh	N/A	Write 1st remote THIGH limit	
WRLN1	0Eh	N/A	Write 1st remote TLOW limit	
OSHT	0Fh	N/A	One-shot command (use send-byte format)	
SET_CNT1	10h	1111 1111b	Write 1st fan programmed speed register	
ACT_CNT1	11h	1111 1111b	Read 1st fan actual speed register	
FAN_STA1	12h	10b	Read 1st fan status register	
SET_CNT2	20h	1111 1111b	Write 2nd fan programmed speed register	
ACT_CNT2	21h	1111 1111b	Read 2nd fan actual speed register	
FAN_STA2	22h	10b	Read 2nd fan status register	
CHIP_TMP	30h	0000 0000b	On-chip temperature	
TMAX1	31h	0100 0110b (70)	1st remote Tmax	
THYST1	32h	0011 1100b (60)	1st remote Thyst	
TMAX2	33h	0100 0110b (70)	2nd remote Tmax	
THYST2	34h	0011 1100b (60)	2nd remote Thyst	

The Alert Response can activate several different slave devices simultaneously, similar to the SMBus General Call. If more than one slave attempts to respond, bus arbitration rules apply, and the device with the lower address code wins. The losing device does

not generate an acknowledge and continues to hold the $\overline{\text{ALERT}}$ line low until serviced (implies that the host interrupt input is level sensitive). Successful reading of the alert response address clears the interrupt latch.

Command Byte Functions

The 8-bit command byte register (Table 4) is the master index that points to the various other registers within the G768B. The register's POR state is 0000 0000, so that a Receive Byte transmission (a protocol that lacks the command byte) that occurs immediately after POR returns the current local temperature data.

The one-shot command immediately forces a new conversion cycle to begin. In software standby mode ($\overline{\text{RUN}}/\text{STOP}$ bit = high), a new conversion is begun, after which the device returns to standby mode. If a conversion is in progress when a one-shot command is received in auto-convert mode (RUN/STOP bit = low) between conversions, a new conversion begins, the conversion rate timer is reset, and the next automatic conversion takes place after a full delay elapses.

Thermal Configuration Byte Functions

The configuration byte register (Table 5) is used to mask (disable) interrupts and to put the device in software standby mode. The lower six bits are internally set to (XX1111), making them "don't care" bits. Write

zeros to these bits. This register's contents can be read back over the serial interface.

Thermal Status Byte Functions

The thermal status byte register (02h) (Table 6) indicates which (if any) temperature thresholds have been exceeded. This byte also indicates whether or not the ADC is converting and whether there is an open circuit in the remote diode DXPx-DXN path. After POR, the normal state of all the flag bits is zero, assuming none of the alarm conditions are present. The status byte is cleared by any successful read of the status, unless the fault persists. Note that the ALERT interrupt latch is not automatically cleared when the status flag bit is cleared.

When reading the status byte, you must check for internal bus collisions caused by asynchronous ADC timing, or else disable the ADC prior to reading the status byte (via the RUN/STOP bit in the configuration byte). In one-shot mode, read the status byte only after the conversion is complete, which is 150ms max after the one-shot conversion is commanded.

BIT	NAME	POR STATE	FUNCTION		
7 (MSB)	MASK	0	Masks all ALERT interrupts when high.		
6	RUN / STOP	0	Standby mode control bit. If high, the device immediately stops converting and enters standby mode. If low, the device converts in either one-shot or timer mode.		
5-0	RFU	0	Reserved for future use		

Table 5. Configuration-Byte Bit Assignments

Table 6. Status-Byte Bit Assignments

BIT	NAME	FUNCTION			
7(MSB)	BUSY	A high indicates that the ADC is busy converting.			
6	RHIGH2*	A high indicates that the 2 nd diode high-temperature alarm has activated.			
5	RLOW2*	A high indicates that the 2 nd diode low-temperature alarm has activated.			
4	RHIGH1*	A high indicates that the 1 st diode high-temperature alarm has activated.			
3	RLOW1*	A high indicates that the 1 st diode low-temperature alarm has activated.			
2	OPEN*	A high indicates a remote-diode continuity (open-circuit) fault.			
1	RFU	Reserved for future use (returns 0)			
0(LSB)	RFU	Reserved for future use (returns 0)			

*These flags stay high until cleared by POR, or until the status byte register is read.

Table 7. Conversion-Rate Control Byte

DATA	CONVERSION RATE (Hz)	Temperature Sensor Average Supply Current (μΑ TYP, at Vcc = 5V)		
00h	0.0625	30		
01h	0.125	33		
02h	0.25	35		
03h	0.5	48		
04h	1	70		
05h	2	128		
06h	4	225		
07h	8	425		
08h to FFh	RFU	-		



OPERATING MODE	CONVERSION INITIATED BY:	NEW CONVERSION RATE (CHANGED VIA WRITE TO CRW)	TIME UNTIL RLTS AND RRTE ARE UPDATED
Auto-Convert	Power-on reset	N/A (0.25Hz)	156ms max
Auto-Convert	1-shot command, while idling between automatic conversions	N/A	156ms max
Auto-Convert	1-shot command that occurs during a conversion	N/A	When current conversion is complete (1-shot is ignored)
Auto-Convert	Rate timer	0.0625Hz	20sec
Auto-Convert	Rate timer	0.125Hz	10sec
Auto-Convert	Rate timer	0.25Hz	5sec
Auto-Convert	Rate timer	0.5Hz	2.5sec
Auto-Convert	Rate timer	1Hz	1.25sec
Auto-Convert	Rate timer	2Hz	625ms
Auto-Convert	Rate timer	4Hz	312.5ms
Auto-Convert	Rate timer	8Hz	237.5ms
Software Standby	RUN/STOP bit	N/A	156ms
Software Standby	1-shot command	N/A	156ms

Table 8. RLTS and RRTE Temp Register Update Timing Chart

To check for internal bus collisions, read the status byte. If the least significant seven bits are ones, discard the data and read the status byte again. The status bits LHIGH, LLOW, RHIGH, and RLOW are refreshed on the SMBus clock edge immediately following the stop condition, so there is no danger of losing temperature-related status data as a result of an internal bus collision. The OPEN status bit (diode continuity fault) is only refreshed at the beginning of a conversion, so OPEN data is lost. The ALERT interrupt latch is independent of the status byte register, so no false alerts are generated by an internal bus collision.

When auto-converting, if the THIGH and TLOW limits are close together, it's possible for both high-temp and low-temp status bits to be set, depending on the amount of time between status read operations (especially when converting at the fastest rate). In these circumstances, it's best not to rely on the status bits to indicate reversals in long-term temperature changes and instead use a current temperature reading to establish the trend direction.

Temperature Conversion Rate Byte

The conversion rate register (Table 7) programs the time interval between conversions in free running auto-convert mode. This variable rate control reduces the supply current in portable-equipment applications. The conversion rate byte's POR state is 02h (0.25Hz). The G768B looks only at the 3 LSB bits of this register, so the upper 5 bits are "don't care" bits, which should be set to zero. The conversion rate tolerance is $\pm 25\%$ at any rate setting.

Valid A/D conversion results for all channels are available one total conversion time (125ms nominal, 156ms

156ms maximum) after initiating a conversion, whether conversion is initiated via the RUN/STOP bit, one-shot command, or initial power-up. Changing the conversion rate can also affect the delay until new results are available. See Table 8.

Programmed fan speed register

The programmed fan speed registers (10h for fan 1, 20h for fan 2) are read/write registers. They contain the count number of the desired fan speed. Power up default is FFh.

Actual fan speed register

The actual fan speed registers (11h for fan 1, 21h for fan 2) are read only. They contain the count number of the actual fan speed. Power up default is FFh.

Fan status register

The fan status registers (12h for fan1, 22h for fan 2) are read only. Its bit 0 is set to 1 when the actual fan speed is $\pm 20\%$ outside the desired speed. Its bit 1 is set to 1 when fan speed is below 1920 rpm. Power up default is 0000_0010b.

Watchdog for fan control

Four temperature threshold registers intervene the control of fans. Both pin OUT1 and pin OUT2 go high when one of the remote temperature, DX1 and DX2, rises above the respective Tmax. The control is not released until both temperature values drop below their Thyst. Besides, the fan controller also fully turns on both fans when either of the two remote diodes is open or both are short.

The power-up default values for Tmax and Thyst are $+70^{\circ}$ C and $+60^{\circ}$ C, respectively. This allows the G768B to be used in the occasion when system fails and loses the fan control of G768B.

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Slave Addresses

The G768B appears to the SMBus as one device having a common address for all the ADC and fan control channels. The device address is fixed to be 7Ah for write and 7Bh for read.

The G768B also responds to the SMBus Alert Response slave address (see the Alert Response Address section).

POR and UVLO

The G768B has a volatile memory. To prevent ambiguous power-supply conditions from corrupting the

Power-Up Defaults:

- Interrupt latch is cleared.
- ADC begins auto /converting at a 0.25Hz rate.
- Command byte is set to 00h to facilitate quick re-

data in memory and causing erratic behavior, a POR voltage detector monitors Vcc and clears the memory if Vcc falls below 1.7V (typical, see Electrical Characteristics table). When power is first applied and Vcc rises above 1.75V (typical), the logic blocks begin operating, although reads and writes at V_{CC} levels below 3V are not recommended. A second Vcc comparator, the ADC UVLO comparator, prevents the ADC from converting until there is sufficient headroom (Vcc = 2.8V typical).

mote Receive Byte queries.

 THIGH and TLOW registers are set to max and min limits, respectively.

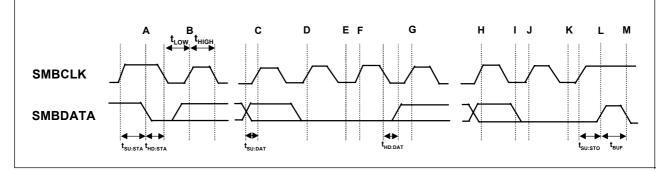


Figure 6. SMBus Write Timing Diagram

- A = start condition
- B = MSB of address clocked into slave
- C = LSB of address clocked into slave
- D = R / W bit clocked into slave
- E = slave pulls SMBData line low
- F = acknowledge bit clocked into master
- G = MSB of data clocked into slave

- H = LSB of data clocked into slave
- I = slave pulls SMBDATA line low
- J = acknowledge clocked into master
- K = acknowledge clocked pulse
- L = stop condition data executed by slave
- M = new start condition

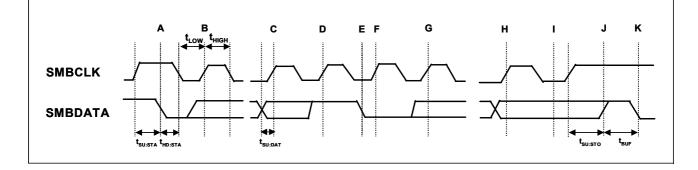
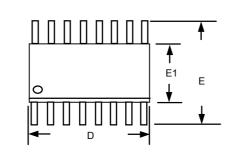


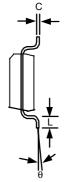
Figure 7. SMBus Read Timing Diagram

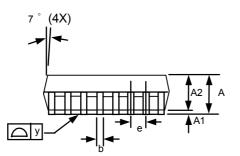
- A = start condition
- B = MSB of address clocked into slave
- C = LSB of address clocked into slave
- $D = R / \overline{W}$ bit clocked into slave
- E = slave pulls SMBDATA line low
- F =acknowledge bit clocked into master
- G = MSB of data clocked into master H = LSB of data clocked into master
 - I = acknowledge clocked pulse
 - J = stop condition
 - K= new start condition



Package Information





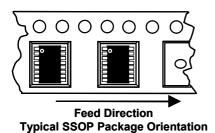


Note:

- 1. Package body sizes exclude mold flash and gate burrs
- 2. Dimension L is measured in gage plane
- 3. Tolerance 0.10mm unless other wise specified
- 4. Controlling dimension is millimeter converted inch dimensions are not necessarily exact.

SYMBOLS	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
А	1.35	1.60	1.75	0.053	0.064	0.069
A1	0.10		0.25	0.004		0.010
A2		1.45			0.057	
b	0.20	0.25	0.30	0.008	0.010	0.012
С	0.19		0.25	0.007		0.010
D	4.80		5.00	0.189		0.197
E	5.80		6.20	0.228		0.244
E1	3.80		4.00	0.150		0.157
e		0.64			0.025	
L	0.40		1.27	0.016		0.050
у			0.10			0.004
θ	0°		8°	0°		8°

Taping Specification



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