**TSOP**
**Commercial Temp**
**Industrial Temp**

# 64K x 16
# 1Mb Asynchronous SRAM

**8, 9ns**
**3.3V $V_{DD}$**
**Center $V_{DD}$ & $V_{SS}$**

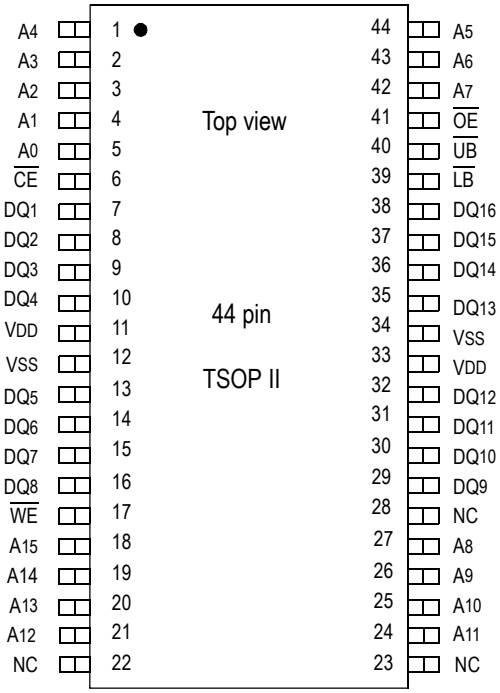
## Features

- Fast access time: 8, 9ns
- CMOS low power operation: 150/150 mA at min. cycle time.
- Single 3.3V ± 0.3V power supply
- All inputs and outputs are TTL compatible
- Byte control
- Fully static operation
- Industrial Temperature Option: -40° to 85°C
- Package line up
  TP: 400mil, 44 pin TSOP Type II package

## Description

The GS71216 is a high speed CMOS static RAM organized as 65,536-words by 16-bits. Static design eliminates the need for external clocks or timing strobes. Operating on a single 3.3V power supply and all inputs and outputs are TTL compatible. The GS71216 is available in a 400 mil TSOP Type-II package.

## TSOP-II 64K x 16 Pin Configuration

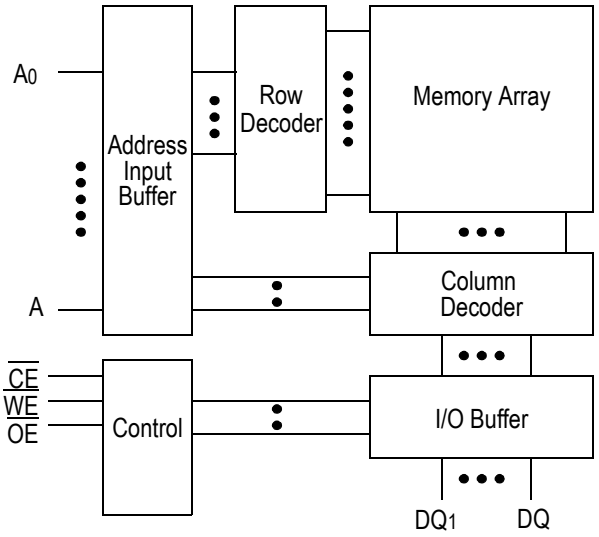



### Pin Descriptions

| Symbol | Description |
|---|---|
| $A_0$ to $A_{15}$ | Address input |
| $DQ_1$ to $DQ_{16}$ | Data input/output |
| $\overline{CE}$ | Chip enable input |
| $\overline{LB}$ | Lower byte enable input (DQ1 to DQ8) |
| $\overline{UB}$ | Upper byte enable input (DQ9 to DQ16) |
| $\overline{WE}$ | Write enable input |
| $\overline{OE}$ | Output enable input |
| $V_{DD}$ | +3.3V power supply |
| $V_{SS}$ | Ground |
| NC | No connect |

## Block Diagram




### Truth Table

| $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | $\overline{LB}$ | $\overline{UB}$ | DQ1 to DQ8 | DQ9 to DQ16 | VDD Current |
|---|---|---|---|---|---|---|---|
| H | X | X | X | X | Not Selected | Not Selected | ISB1, ISB2 |
| L | L | H | L | L | Read | Read | IDD |
| | | | L | H | Read | High Z | |
| | | | H | L | High Z | Read | |
| L | X | L | L | L | Write | Write | |
| | | | L | H | Write | Not Write, High Z | |
| | | | H | L | Not Write, High Z | Write | |
| L | H | H | X | X | High Z | High Z | |
| L | X | X | H | H | High Z | High Z | |

Note: X: “H” or “L”

## Absolute Maximum Ratings

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Supply Voltage | $V_{DD}$ | -0.5 to +4.6 | V |
| Input Voltage | $V_{IN}$ | -0.5 to $V_{DD}$+0.5 (≤ 4.6V max.) | V |
| Output Voltage | $V_{OUT}$ | -0.5 to $V_{DD}$+0.5 (≤ 4.6V max.) | V |
| Allowable power dissipation | PD | 0.7 | W |
| Storage temperature | $T_{STG}$ | -55 to 150 | °C |

Note:
Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation shall be restricted to Recommended Operating Conditions. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

## Recommended Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply Voltage for -9 | $V_{DD}$ | 3.0 | 3.3 | 3.6 | V |
| Supply Voltage for -8 | $V_{DD}$ | 3.135 | 3.3 | 3.6 | V |
| Input High Voltage | $V_{IH}$ | 2.0 | - | $V_{DD}$+0.3 | V |
| Input Low Voltage | $V_{IL}$ | -0.3 | - | 0.8 | V |
| Ambient Temperature, Commercial Range | $T_{Ac}$ | 0 | - | 70 | °C |
| Ambient Temperature, Industrial Range | $T_{AI}$ | -40 | - | 85 | °C |

Note:
1. Input overshoot voltage should be less than $V_{DD}$+2V and not exceed 20ns.
2. Input undershoot voltage should be greater than -2V and not exceed 20ns.

## Capacitance

| Parameter | Symbol | Test Condition | Max | Unit |
|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | $V_{IN}$=0V | 5 | pF |
| Output Capacitance | $C_{OUT}$ | $V_{OUT}$=0V | 7 | pF |

Notes:
1. Tested at $T_A$=25°C, f=1MHz
2. These parameters are sampled and are not 100% tested

## DC I/O Pin Characteristics

| Parameter | Symbol | Test Conditions | Min | Max |
|---|---|---|---|---|
| Input Leakage Current | $I_{IL}$ | $V_{IN}$ = 0 to $V_{DD}$ | -1uA | 1uA |
| Output Leakage Current | $I_{LO}$ | Output High Z<br>$V_{OUT}$ = 0 to $V_{DD}$ | -1uA | 1uA |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = - 4mA | 2.4 | |
| Output Low Voltage | $V_{OL}$ | $I_{LO}$ = + 4mA | | 0.4V |

## Power Supply Currents

| Parameter | Symbol | Test Conditions | 0 to 70°C | | -40 to 85°C | |
|---|---|---|---|---|---|---|
| | | | 8ns | 9ns | 8ns | 9ns |
| Operating Supply Current | $I_{DD}$ | $\overline{CE} \leq V_{IL}$<br>All other inputs<br>$\geq V_{IH}$ or $\leq V_{IL}$<br>Min. cycle time<br>$I_{OUT}$ = 0 mA | 150mA | 150mA | 160mA | 160mA |
| Standby Current | $I_{SB1}$ | $\overline{CE} \geq V_{IH}$<br>All other inputs<br>$\geq V_{IH}$ or $\leq V_{IL}$<br>Min. cycle time | 55mA | 55mA | 65mA | 65mA |
| Standby Current | $I_{SB2}$ | $CE \geq V_{DD}$ - 0.2V<br>All other inputs<br>$\geq V_{DD}$ - 0.2V or $\leq$ 0.2V | 15mA | | 25mA | |

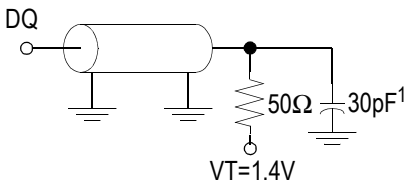
  

## AC Test Conditions

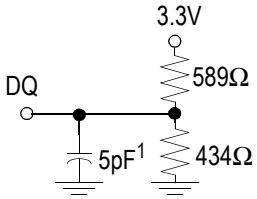
| Parameter | Conditions |
|---|---|
| Input high level | $V_{IH}$=2.4V |
| Input low level | $V_{IL}$=0.4V |
| Input rise time | tr=1V/ns |
| Input fall time | tf=1V/ns |
| Input reference level | 1.4V |
| Output reference level | 1.4V |
| Output load | Fig. 1& 2 |

Note:
1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in Fig. 1 unless otherwise noted
3. Output load 2 for $t_{LZ}$, $t_{HZ}$, $t_{OLZ}$ and $t_{OHZ}$.

Output Load 1




Output Load 2



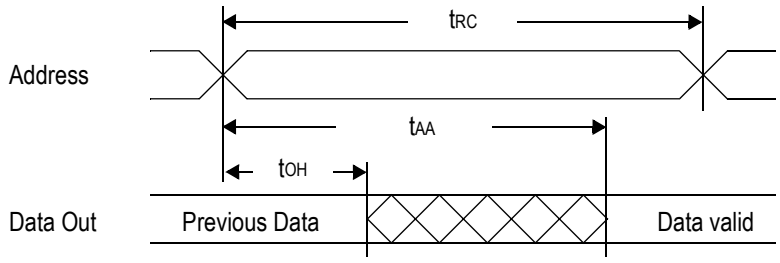
## AC Characteristics

### Read Cycle

| Parameter | Symbol | -8 | | -9 | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| Read cycle time | $t_{RC}$ | 8 | --- | 9 | --- | ns |
| Address access time | $t_{AA}$ | --- | 8 | --- | 9 | ns |
| Chip enable access time ($\overline{CE}$) | $t_{AC}$ | --- | 8 | --- | 9 | ns |
| Byte enable access time ($\overline{UB}$, $\overline{LB}$) | $t_{AB}$ | --- | 3.5 | --- | 3.5 | ns |
| Output enable to output valid ($\overline{OE}$) | $t_{OE}$ | --- | 3.5 | --- | 3.5 | ns |
| Output hold from address change | $t_{OH}$ | 3 | --- | 3 | --- | ns |
| Chip enable to output in low Z ($\overline{CE}$) | $t_{LZ}$* | 3 | --- | 3 | --- | ns |
| Output enable to output in low Z ($\overline{OE}$) | $t_{OLZ}$* | 0 | --- | 0 | --- | ns |
| Byte enable to output in low Z ($\overline{UB}$, $\overline{LB}$) | $t_{BLZ}$* | 0 | --- | 0 | --- | ns |
| Chip disable to output in High Z ($\overline{CE}$) | $t_{HZ}$* | --- | 4 | --- | 4 | ns |
| Output disable to output in High Z ($\overline{OE}$) | $t_{OHZ}$* | --- | 3.5 | --- | 3.5 | ns |
| Byte disable to output in High Z ($\overline{UB}$, $\overline{LB}$) | $t_{BHZ}$* | --- | 3.5 | --- | 3.5 | ns |

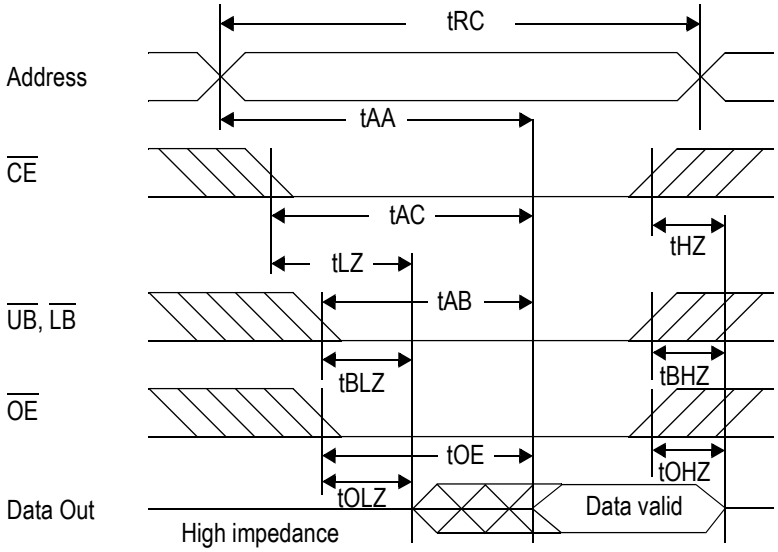
* These parameters are sampled and are not 100% tested

### Read Cycle 1: $\overline{CE}$ = $\overline{OE}$ = $V_{IL}$, $\overline{WE}$ = $V_{IH}$, $\overline{UB}$ and, or $\overline{LB}$ = $V_{IL}$



## Read Cycle 2: $\overline{WE} = V_{IH}$



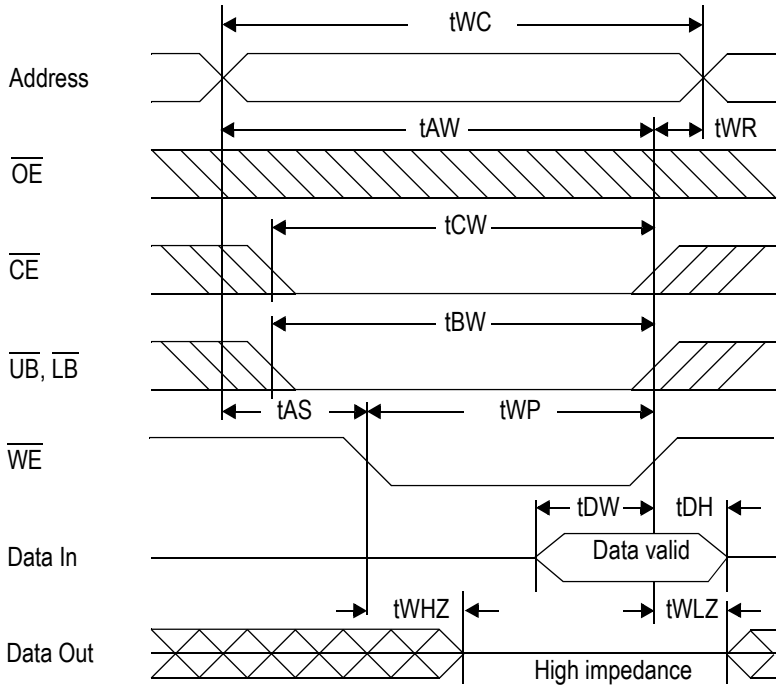

## Write Cycle

| Parameter | Symbol | -8 | | -9 | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| Write cycle time | tWC | 8 | --- | 9 | --- | ns |
| Address valid to end of write | tAW | 5.5 | --- | 5.5 | --- | ns |
| Chip enable to end of write | tCW | 5.5 | --- | 5.5 | --- | ns |
| Byte enable to end of write | tBW | 5.5 | --- | 5.5 | --- | ns |
| Data set up time | tDW | 4 | --- | 4 | --- | ns |
| Data hold time | tDH | 0 | --- | 0 | --- | ns |
| Write pulse width | tWP | 5.5 | --- | 5.5 | --- | ns |
| Address set up time | tAS | 0 | --- | 0 | --- | ns |
| Write recovery time ($\overline{WE}$) | tWR | 0 | --- | 0 | --- | ns |
| Write recovery time ($\overline{CE}$) | tWR1 | 0 | --- | 0 | --- | ns |
| Output Low Z from end of write | tWLZ* | 3 | --- | 3 | --- | ns |
| Write to output in High Z | tWHZ* | --- | 3.5 | --- | 3.5 | ns |

* These parameters are sampled and are not 100% tested

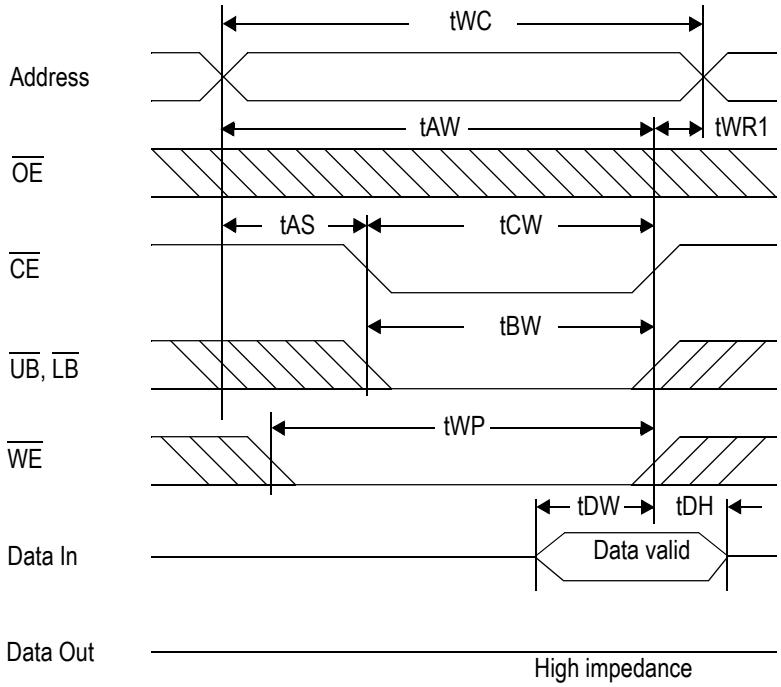
  

**Write Cycle 1: $\overline{WE}$ control**

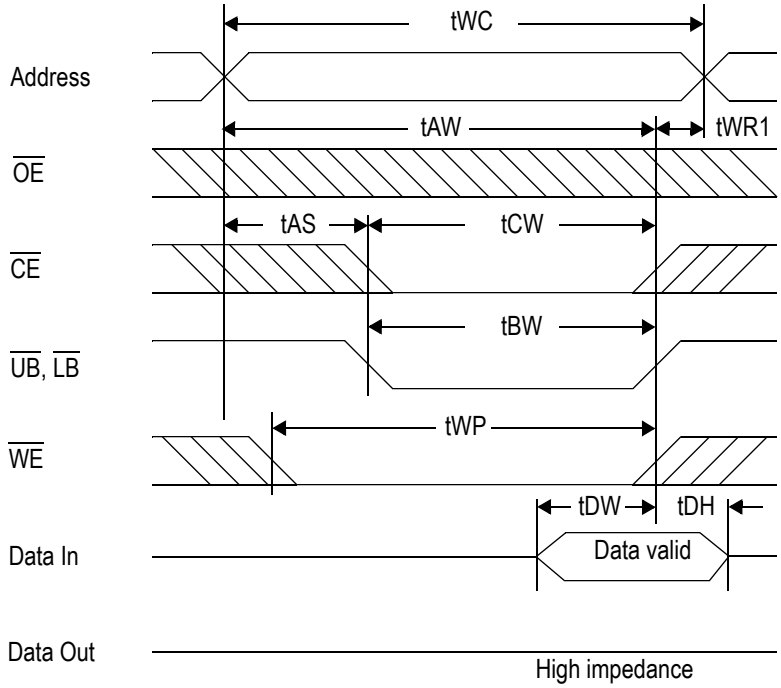


### Write Cycle 2: $\overline{CE}$ control

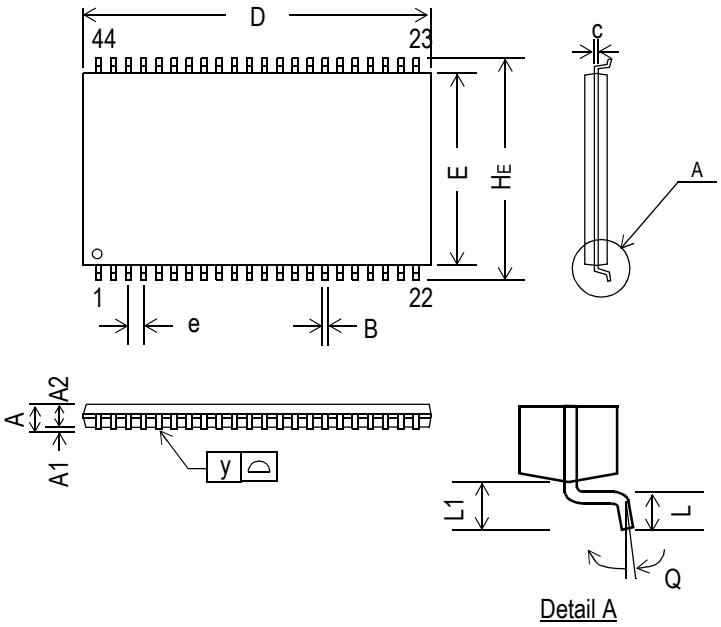



### Write Cycle 3: $\overline{UB}$, $\overline{LB}$ control



## 44 Pin, 400 mil TSOP-II




| Symbol | Dimension in inch | | | Dimension in mm | | |
|---|---|---|---|---|---|---|
| | min | nom | max | min | nom | max |
| A | - | - | 0.047 | - | - | 1.20 |
| A1 | 0.002 | - | - | 0.05 | - | - |
| A2 | 0.037 | 0.039 | 0.041 | 0.95 | 1.00 | 1.05 |
| B | 0.01 | 0.014 | 0.018 | 0.25 | 0.35 | 0.45 |
| c | - | 0.006 | - | - | 0.15 | - |
| D | 0.721 | 0.725 | 0.729 | 18.31 | 18.41 | 18.51 |
| E | 0.396 | 0.400 | 0.404 | 10.06 | 10.16 | 10.26 |
| e | - | 0.031 | - | - | 0.80 | - |
| HE | 0.455 | 0.463 | 0.471 | 11.56 | 11.76 | 11.96 |
| L | 0.016 | 0.020 | 0.024 | 0.40 | 0.50 | 0.60 |
| L1 | - | 0.031 | - | - | 0.80 | - |
| y | - | - | 0.004 | - | - | 0.10 |
| Q | 0° | - | 5° | 0° | - | 5° |

Note:
1. Dimension D& E do not include interlead flash
2. Dimension B does not include dambar protrusion / intrusion
3. Controlling dimension: mm

## Ordering Information

| Part Number* | Package | Access Time | Temp. Range | Status |
|---|---|---|---|---|
| GS71216TP-8 | 400 mil TSOP-II | 8 ns | Commercial | |
| GS71216TP-10 | 400 mil TSOP-II | 9 ns | Commercial | |
| GS71216TP-8I | 400 mil TSOP-II | 8 ns | Industrial | |
| GS71216TP-10I | 400 mil TSOP-II | 9 ns | Industrial | |

* Customers requiring delivery in Tape and Reel should add the character “T” to the end of the part number. For example: GS71216TP-8T