

BGA
Commercial Temp
Industrial Temp

512K x 16

8Mb Asynchronous SRAM

10, 12, 15 ns
3.3 V V_{DD}

Features

- Fast access time: 10, 12, 15 ns
- CMOS low power operation: 300/250/220/180 mA at minimum cycle time
- Single 3.3 V \pm 0.3 V power supply
- All inputs and outputs are TTL-compatible
- Fully static operation
- Industrial Temperature Option: -40° to 85° C
- 14 mm x 22 mm, 119-Bump, 1.27 mm Pitch Ball Grid Array package

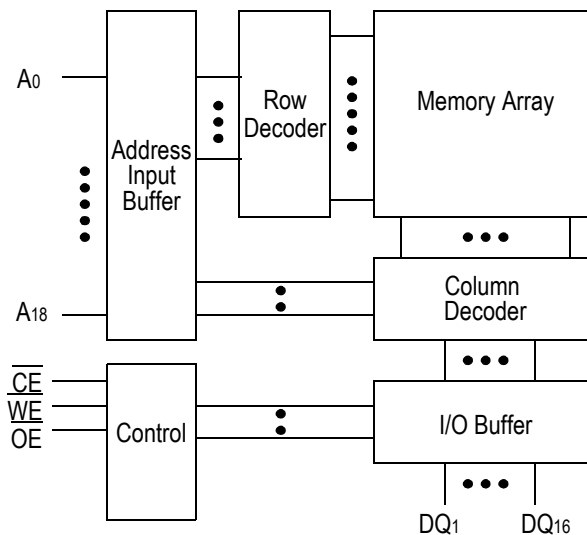
Description

The GS78116 is a high speed CMOS static RAM organized as 524,288-words by 16-bits. Static design eliminates the need for external clocks or timing strobes. The GS78116 operates on a single 3.3 V power supply and all inputs and outputs are TTL-compatible. The GS78116 is available in 14 mm x 22 mm BGA package.

Pin Descriptions

Symbol	Description
A ₀ to A ₁₈	Address input
DQ ₁ to DQ ₁₆	Data input/output
$\overline{\text{CE}}$	Chip enable input
$\overline{\text{WE}}$	Write enable input
$\overline{\text{OE}}$	Output enable input
V _{DD}	+3.3 V power supply
V _{SS}	Ground
NC	No connect

Block Diagram



512K x 16 Async SRAM in 119-Bump, 14 mm x 22 mm
Top View

	1	2	3	4	5	6	7
A	NC	A15	A14	A16	A13	A12	NC
B	NC, V _{SS}	A11	A10	$\overline{\text{CE}}$	A9	A8	NC
C	NC	NC	V _{DD} , NC	A17	V _{SS} , NC	NC	NC
D	NC	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	NC
E	DQ1	NC	V _{DD}	V _{SS}	V _{DD}	NC	DQ16
F	DQ2	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	DQ15
G	DQ3	NC	V _{DD}	V _{SS}	V _{DD}	NC	DQ14
H	DQ4	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	DQ13
J	V _{DD}	V _{SS}	V _{DD}	V _{SS}	V _{DD}	V _{SS}	V _{DD}
K	DQ5	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	DQ12
L	DQ6	NC	V _{DD}	V _{SS}	V _{DD}	NC	DQ11
M	DQ7	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	DQ10
N	DQ8	NC	V _{DD}	V _{SS}	V _{DD}	NC	DQ9
P	NC	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	NC
R	NC	NC	NC	A18	NC	NC	NC
T	NC	A7	A6	$\overline{\text{WE}}$	A5	A4	NC, V _{SS}
U	NC	A3	A2	$\overline{\text{OE}}$	A1	A0	NC

Note: Bumps 1B, 7T, 3C, and 5C are actually NC's but should be wired 3C = V_{DD} and 1B, 7T and 5C = V_{SS} to assure compatibility with future versions.

Truth Table

$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	DQ ₁ to DQ ₈	V _{DD} Current
H	X	X	Not Selected	ISB1, ISB2
L	L	H	Read	
L	X	L	Write	I _{DD}
L	H	H	High Z	

Note: X: "H" or "L"

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	V _{DD}	-0.5 to +4.6	V
Input Voltage	V _{IN}	-0.5 to V _{DD} +0.5 (≤ 4.6 V max.)	V
Output Voltage	V _{OUT}	-0.5 to V _{DD} +0.5 (≤ 4.6 V max.)	V
Allowable power dissipation	PD	1.5	W
Storage temperature	T _{STG}	-55 to 150	°C

Note:

Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation shall be restricted to Recommended Operating Conditions. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage for -10/12/15	V _{DD}	3.0	3.3	3.6	V
Input High Voltage	V _{IH}	2.0	—	V _{DD} +0.3	V
Input Low Voltage	V _{IL}	-0.3	—	0.8	V
Ambient Temperature, Commercial Range	T _{Ac}	0	—	70	°C
Ambient Temperature, Industrial Range	T _{Ai}	-40	—	85	°C

Notes:

1. Input overshoot voltage should be less than V_{DD}+2 V and not exceed 20 ns.
2. Input undershoot voltage should be greater than -2 V and not exceed 20 ns.

Capacitance

Parameter	Symbol	Test Condition	Max	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0\text{ V}$	10	pF
Output Capacitance	C_{OUT}	$V_{OUT} = 0\text{ V}$	7	pF

Notes:

1. Tested at $T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$
2. These parameters are sampled and are not 100% tested.

DC I/O Pin Characteristics

Parameter	Symbol	Test Conditions	Min	Max
Input Leakage Current	I_{IL}	$V_{IN} = 0\text{ to }V_{DD}$	-2 μA	2 μA
Output Leakage Current	I_{OL}	Output High Z, $V_{OUT} = 0\text{ to }V_{DD}$	-1 μA	1 μA
Output High Voltage	V_{OH}	$I_{OH} = -4\text{ mA}$	2.4	
Output Low Voltage	V_{OL}	$I_{OL} = +4\text{ mA}$		0.4 V

Power Supply Currents

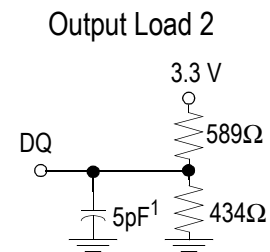
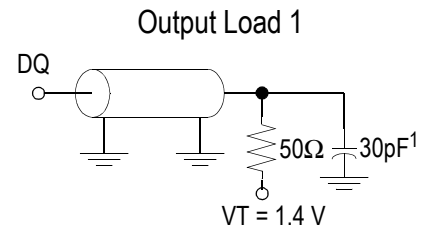
Parameter	Symbol	Test Conditions	0 to 70°C			-40 to 85°C		
			10 ns	12 ns	15 ns	10 ns	12 ns	15 ns
Operating Supply Current	I_{DD}	$\bar{E} \leq V_{IL}$ All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ Min. cycle time $I_{OUT} = 0\text{ mA}$	225 mA	220 mA	180 mA	270 mA	240 mA	200 mA
Standby Current	I_{SB1}	$\bar{E} \geq V_{IH}$ All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ Min. cycle time	130 mA	120 mA	110 mA	150 mA	140 mA	130 mA
Standby Current	I_{SB2}	$E \geq V_{DD} - 0.2\text{V}$ All other inputs $\geq V_{DD} - 0.2\text{ V}$ or $\leq 0.2\text{ V}$	60 mA			80 mA		

AC Test Conditions

Parameter	Conditions
Input high level	$V_{IH} = 2.4\text{ V}$
Input low level	$V_{IL} = 0.4\text{ V}$
Input rise time	$t_r = 1\text{ V/ns}$
Input fall time	$t_f = 1\text{ V/ns}$
Input reference level	1.4 V
Output reference level	1.4 V
Output load	Fig. 1 & 2

Notes:

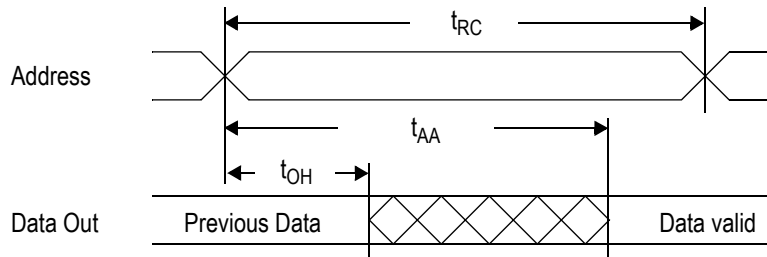
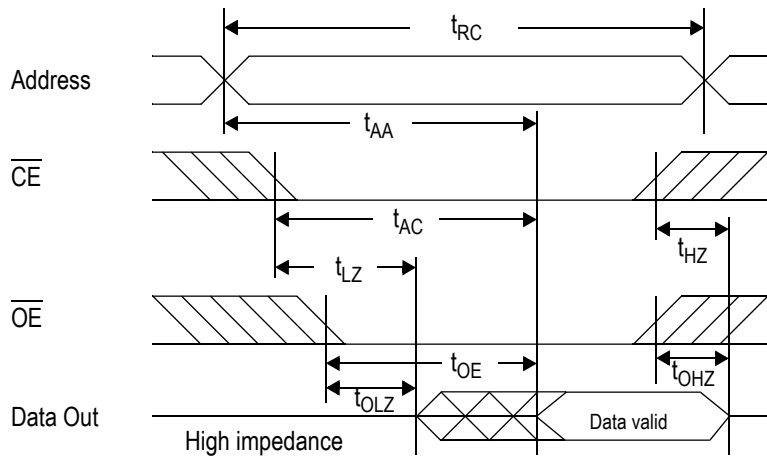
1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in **Fig. 1** unless otherwise noted
3. Output load 2 for t_{LZ} , t_{HZ} , t_{OLZ} and t_{OHZ} .



AC Characteristics

Read Cycle

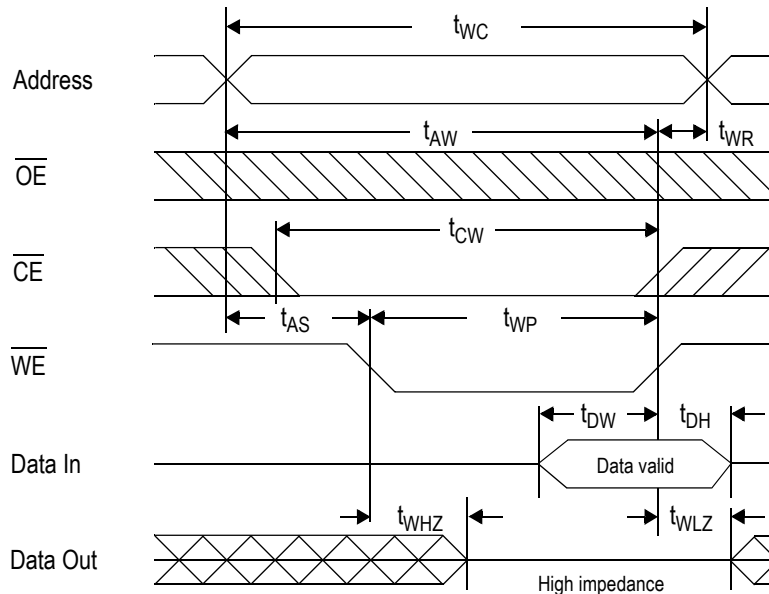
Parameter	Symbol	-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	
Read cycle time	t_{RC}	10	—	12	—	15	—	ns
Address access time	t_{AA}	—	10	—	12	—	15	ns
Chip enable access time (\overline{CE})	t_{AC}	—	10	—	12	—	15	ns
Output enable to output valid (\overline{OE})	t_{OE}	—	4	—	5	—	6	ns
Output hold from address change	t_{OH}	3	—	3	—	3	—	ns
Chip enable to output in low Z (\overline{CE})	t_{LZ}^*	3	—	3	—	3	—	ns
Output enable to output in low Z (\overline{OE})	t_{OLZ}^*	0	—	0	—	0	—	ns
Chip disable to output in High Z (\overline{CE})	t_{HZ}^*	—	5	—	6	—	7	ns
Output disable to output in High Z (\overline{OE})	t_{OHZ}^*	—	4	—	5	—	6	ns

Read Cycle 1: $\overline{CE} = \overline{OE} = V_{IL}$

Read Cycle 2: $\overline{WE} = V_{IH}$


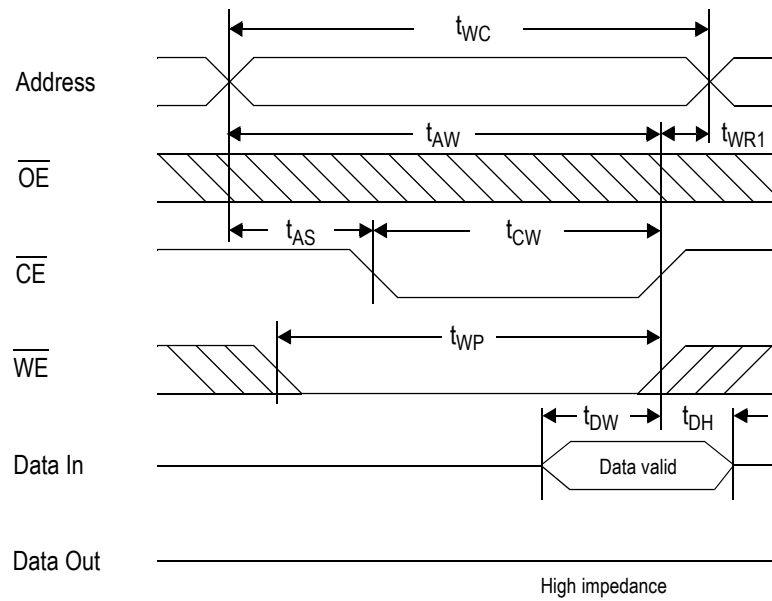
Write Cycle

Parameter	Symbol	-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	
Write cycle time	t _{WC}	10	—	12	—	15	—	ns
Address valid to end of write	t _{AW}	7	—	8	—	10	—	ns
Chip enable to end of write	t _{CW}	7	—	8	—	10	—	ns
Data set up time	t _{DW}	5	—	6	—	7	—	ns
Data hold time	t _{DH}	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	7	—	8	—	10	—	ns
Address set up time	t _{AS}	0	—	0	—	0	—	ns
Write recovery time (\overline{WE})	t _{WR}	0	—	0	—	0	—	ns
Write recovery time (\overline{CE})	t _{WR1}	0	—	0	—	0	—	ns
Output Low Z from end of write	t _{WLZ} *	3	—	3	—	3	—	ns
Write to output in High Z	t _{WHZ} *	—	4	—	5	—	6	ns

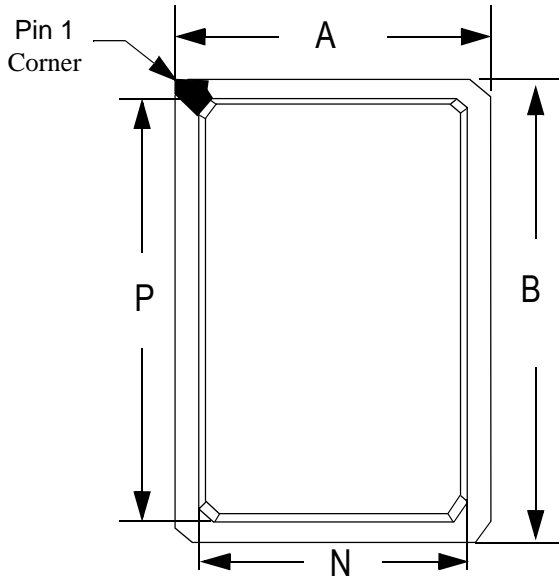
* These parameters are sampled and are not 100% tested.

Write Cycle 1: \overline{WE} Controlled


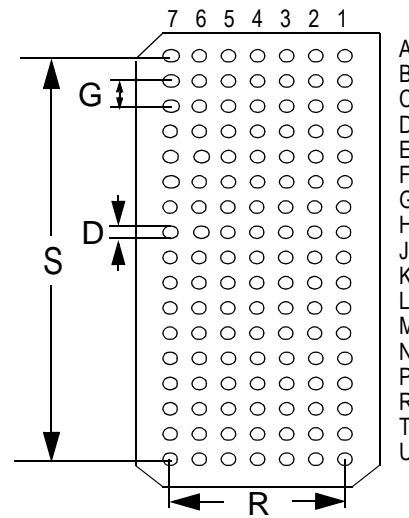
Write Cycle 2: \overline{CE} Controlled



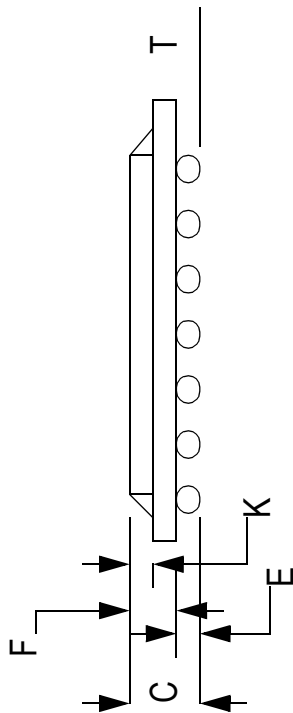
Package Dimensions - 119-Pin PBGA



Top View



Bottom View



Side View

Package Dimensions - 119 Pin PBGA

Symbol	Description	Min.	Nom.	Max
A	Width	13.8	14.0	14.2
B	Length	21.8	22.0	22.2
C	Package Height (including ball)	—	—	2.40
D	Ball Size	0.60	0.75	0.90
E	Ball Height	0.50	0.60	0.70
F	Package Height (excluding balls)	—	1.46	1.70
G	Width between Balls	—	1.27	—
K	Package Height above board	0.80	0.90	1.00
N	Cut-out Package Width	—	12.00	—
P	Foot Length	—	19.50	—
R	Width of package between balls	—	7.62	—
S	Length of package between balls	—	20.32	—
T	Variance of Ball Height	—	0.15	—

Unit: mm

Ordering Information

Part Number *	Package	Access Time	Temp. Range	Status
GS78116B-10	BGA	10 ns	Commercial	
GS78116B-12	BGA	12 ns	Commercial	
GS78116B-15	BGA	15 ns	Commercial	
GS78116B-10I	BGA	10 ns	Industrial	
GS78116B-12I	BGA	12 ns	Industrial	
GS78116B-15I	BGA	15 ns	Industrial	

* Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. For example: GS78116B-12T

Asynchronous SRAM Datasheet Revision History

Rev. Code: Old; New	Types of Changes Format or Content	Page #/Revisions/Reason
GS78116Rev0.01a 5/1999; 1.00 X/1999	Format/Typos	• p.2/Changed E to CE/consistency.
	Content	• p.2/Changed Pin T1 from BA to Bd/Correction
GS78116Rev 1.0010/1999A;Rev 1.01 2/2000FormatB		• Added GSI Logo
Rev 1.01 2/2000FormatB; 78116_r1_02	Format/Content	<ul style="list-style-type: none"> • Updated format to comply with Technical Publication standards • Finalized document and removed preliminary references