100-Pin TQFP
Commercial Temp
Industrial Temp

512K x 18, 256K x 32, 256K x 36 9Mb Sync Burst SRAMs

5.5 ns–8.5 ns
2.5 V or 3.3 V V_{DD}
2.5 V or 3.3 V I/O

Features

- Flow Through mode operation; Pin 14 = No Connect
- 2.5 V or 3.3 V +10%/–10% core power supply
- 2.5 V or 3.3 V I/O supply
- $\overline{LBO}$ pin for Linear or Interleaved Burst mode
- Internal input resistors on mode pins allow floating mode pins
- Byte Write ($\overline{BW}$) and/or Global Write ($\overline{GW}$) operation
- Internal self-timed write cycle
- Automatic power-down for portable applications
- JEDEC-standard 100-lead TQFP package

		-5.5	-6	-6.5	-7	-7.5	-8.5	Unit
Flow Through 2-1-1-1	t_{KQ}	5.5	6.0	6.5	7.0	7.5	8.5	ns
	tCycle	5.5	6.0	6.5	7.0	7.5	8.5	ns
3.3 V	Curr (x18)	175	165	160	150	145	135	mA
	Curr (x32/x36)	200	190	180	170	165	150	mA
2.5 V	Curr (x18)	175	165	160	150	145	135	mA
	Curr (x32/x36)	200	190	180	170	165	150	mA

Functional Description

Applications

The GS880F18/32/36AT is a 9,437,184-bit (8,388,608-bit for x32 version) high performance synchronous SRAM with a 2-bit burst address counter. Although of a type originally developed for Level 2 Cache applications supporting high performance CPUs, the device now finds application in synchronous SRAM applications, ranging from DSP main store to networking chip set support.

Controls

Addresses, data I/Os, chip enables ($\overline{E1}$, E2, $\overline{E3}$), address burst control inputs ($\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$), and write control inputs ($\overline{Bx}$, $\overline{BW}$, $\overline{GW}$) are synchronous and are controlled by a positive-edge-triggered clock input (CK). Output enable ($\overline{G}$) and power down control (ZZ) are asynchronous inputs. Burst cycles can be initiated with either $\overline{ADSP}$ or $\overline{ADSC}$ inputs. In Burst mode, subsequent burst addresses are generated internally and are controlled by $\overline{ADV}$. The burst address counter may be configured to count in either linear or interleave order with the Linear Burst Order ($\overline{LBO}$) input. The Burst function need not be used. New addresses can be loaded on every cycle with no degradation of chip performance.

Designing For Compatibility

The JEDEC standard for Burst RAMS calls for a $\overline{FT}$ mode pin option on Pin 14. Board sites for flow through Burst RAMS should be designed with V_{SS} connected to the $\overline{FT}$ pin location to ensure the broadest access to multiple vendor sources. Boards designed with $\overline{FT}$ pin pads tied low may be stuffed with GSI's pipeline/flow through-configurable Burst RAMs or any vendor's flow through or configurable Burst SRAM. Boards designed with the $\overline{FT}$ pin location tied high or floating must employ a non-configurable flow through Burst RAM, like this RAM, to achieve flow through functionality.

Byte Write and Global Write

Byte write operation is performed by using Byte Write enable ($\overline{BW}$) input combined with one or more individual byte write signals ($\overline{Bx}$). In addition, Global Write ($\overline{GW}$) is available for writing all bytes at one time, regardless of the Byte Write control inputs.

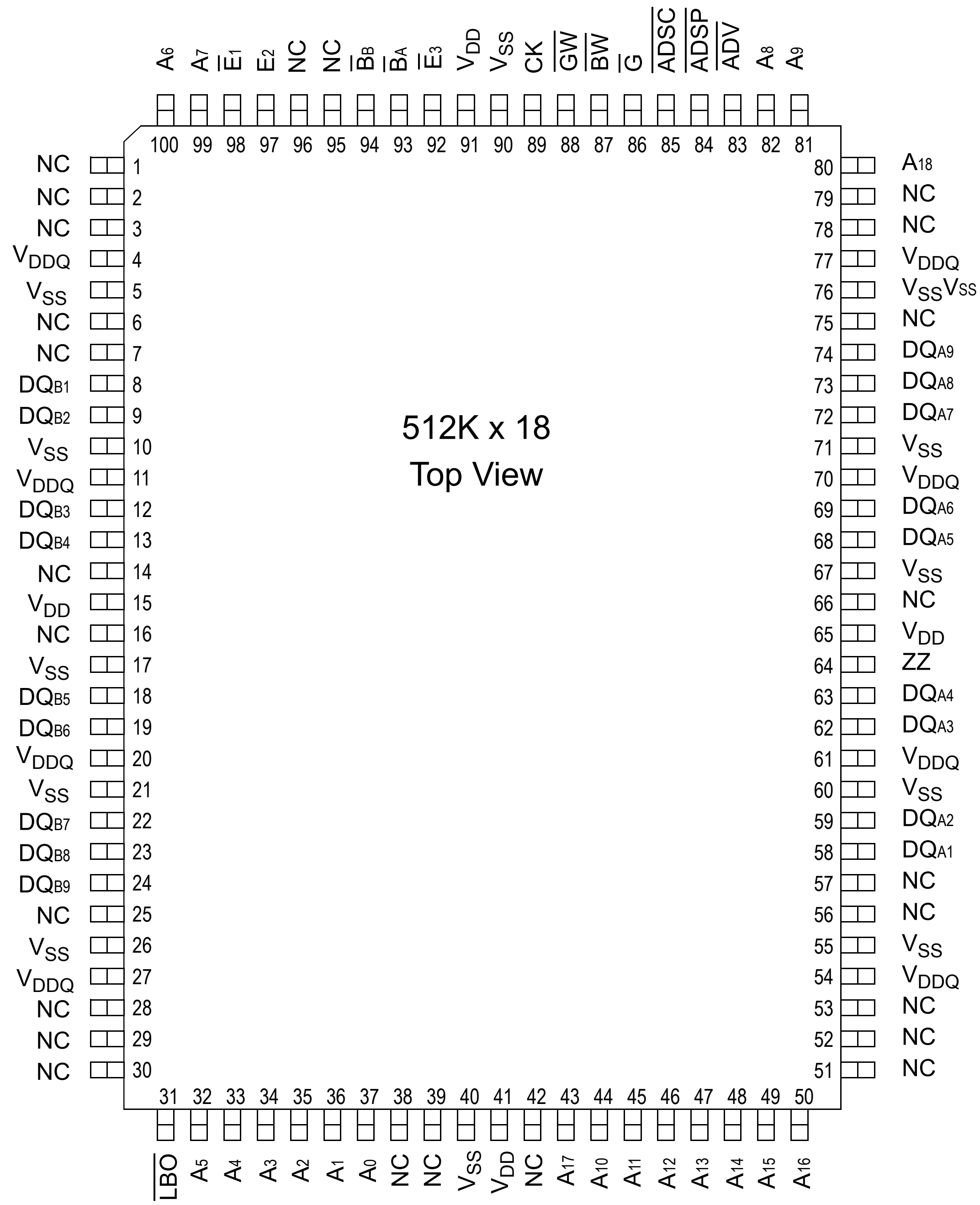
Sleep Mode

Low power (Sleep mode) is attained through the assertion (High) of the ZZ signal, or by stopping the clock (CK). Memory data is retained during Sleep mode.

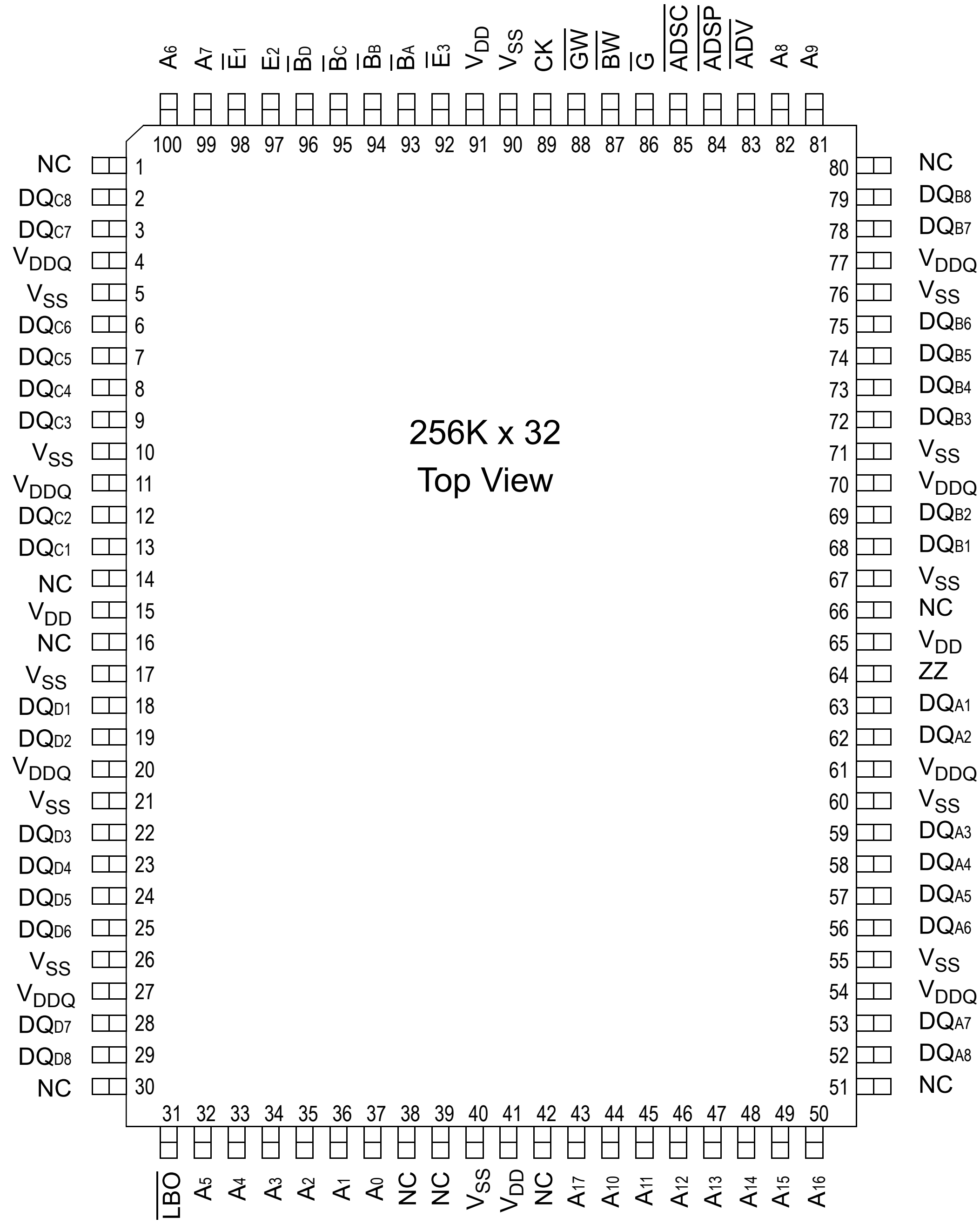
Core and Interface Voltages

The GS880F18/32/36AT operates on a 2.5 V or 3.3 V power supply. All input are 3.3 V and 2.5 V compatible. Separate output power (V_{DDQ}) pins are used to decouple output noise from the internal circuits and are 3.3 V and 2.5 V compatible.

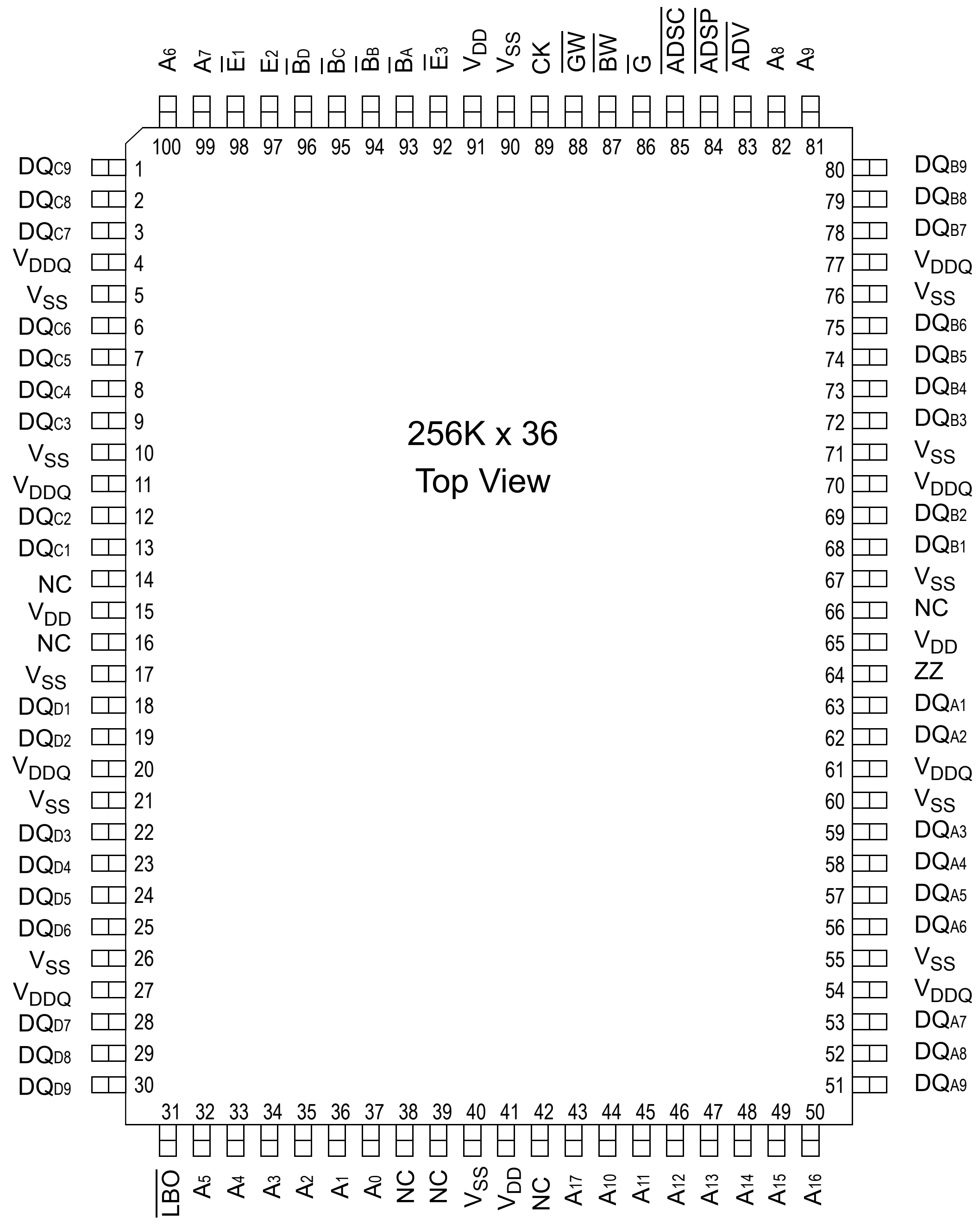
GS880F18A 100-Pin TQFP Pinout



GS880F32A 100-Pin TQFP Pinout



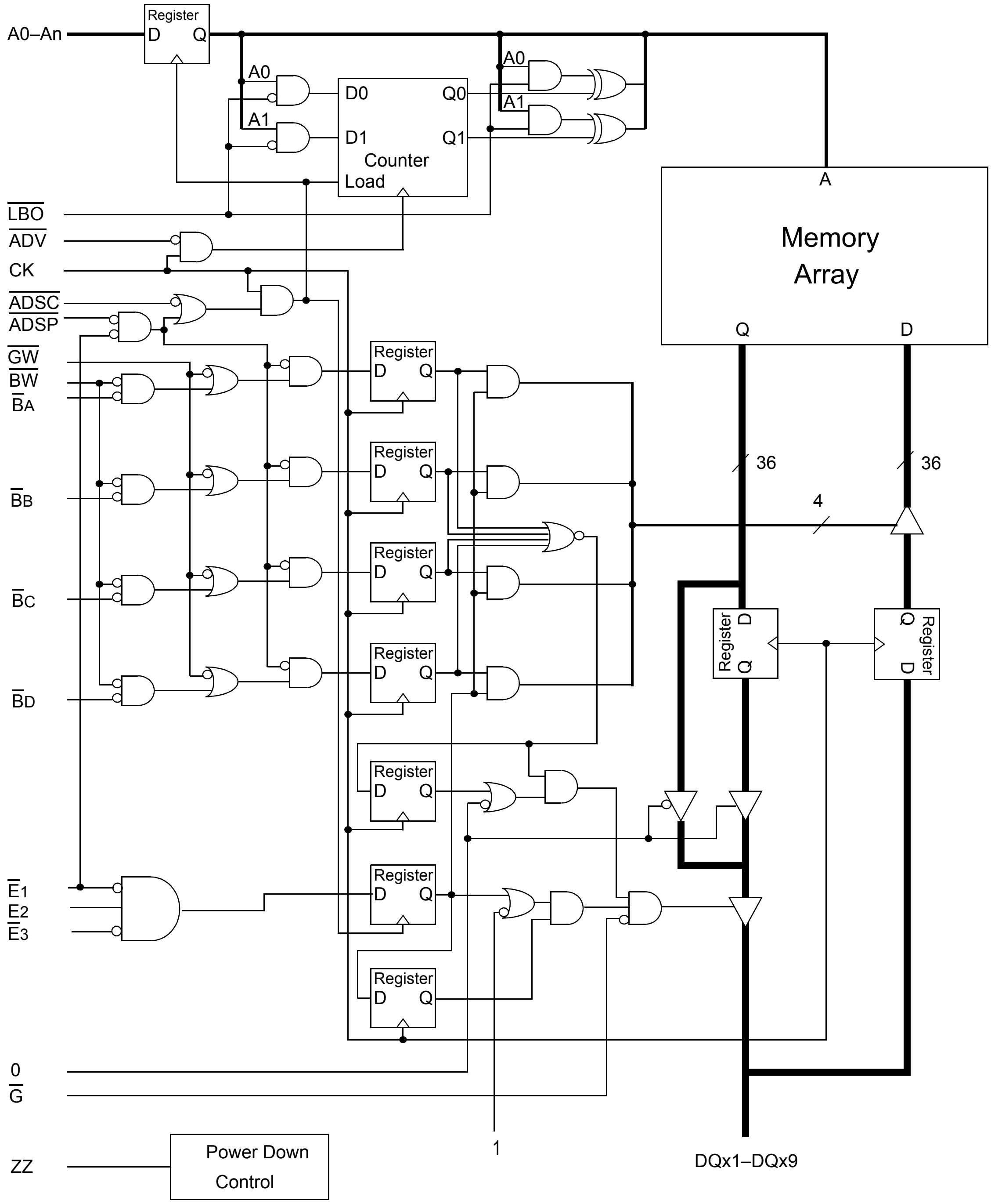
GS880F36A 100-Pin TQFP Pinout



TQFP Pin Description

Symbol	Type	Description
A_0, A_1	I	Address field LSBs and Address Counter preset Inputs
A_2–A_{17}	I	Address Inputs
A_{18}	I	Address Input
DQ_{A1}–DQ_{A9} DQ_{B1}–DQ_{B9} DQ_{C1}–DQ_{C9} DQ_{D1}–DQ_{D9}	I/O	Data Input and Output pins
NC	—	No Connect
$\overline{BW}$	I	Byte Write—Writes all enabled bytes; active low
$\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, $\overline{B}_D$	I	Byte Write Enable for DQ_A, DQ_B Data I/Os; active low
CK	I	Clock Input Signal; active high
$\overline{GW}$	I	Global Write Enable—Writes all bytes; active low
$\overline{E}_1$	I	Chip Enable; active low
$\overline{G}$	I	Output Enable; active low
$\overline{ADV}$	I	Burst address counter advance enable; active low
$\overline{ADSP}$, $\overline{ADSC}$	I	Address Strobe (Processor, Cache Controller); active low
ZZ	I	Sleep Mode control; active high
$\overline{LBO}$	I	Linear Burst Order mode; active low
V_{DD}	I	Core power supply
V_{SS}	I	I/O and Core Ground
V_{DDQ}	I	Output driver power supply

GS880F18/32/36A Block Diagram



Note: Only x36 version shown for simplicity.

Mode Pin Functions

Mode Name	Pin Name	State	Function
Burst Order Control	$\overline{\text{LBO}}$	L	Linear Burst
		H	Interleaved Burst
Power Down Control	ZZ	L or NC	Active
		H	Standby, $I_{DD} = I_{SB}$

Note:
There is a pull-down device on the ZZ pin, so this input pin can be unconnected and the chip will operate in the default states as specified in the above tables.

Burst Counter Sequences

Linear Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	10	11	00
3rd address	10	11	00	01
4th address	11	00	01	10

Note: The burst counter wraps to initial state on the 5th clock.

Interleaved Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	00	11	10
3rd address	10	11	00	01
4th address	11	10	01	00

Note: The burst counter wraps to initial state on the 5th clock.

BPR 1999.05.18

Byte Write Truth Table

Function	$\overline{\text{GW}}$	$\overline{\text{BW}}$	$\overline{\text{B}}_\text{A}$	$\overline{\text{B}}_\text{B}$	$\overline{\text{B}}_\text{C}$	$\overline{\text{B}}_\text{D}$	Notes
Read	H	H	X	X	X	X	1
Read	H	L	H	H	H	H	1
Write byte a	H	L	L	H	H	H	2, 3
Write byte b	H	L	H	L	H	H	2, 3
Write byte c	H	L	H	H	L	H	2, 3, 4
Write byte d	H	L	H	H	H	L	2, 3, 4
Write all bytes	H	L	L	L	L	L	2, 3, 4
Write all bytes	L	X	X	X	X	X	

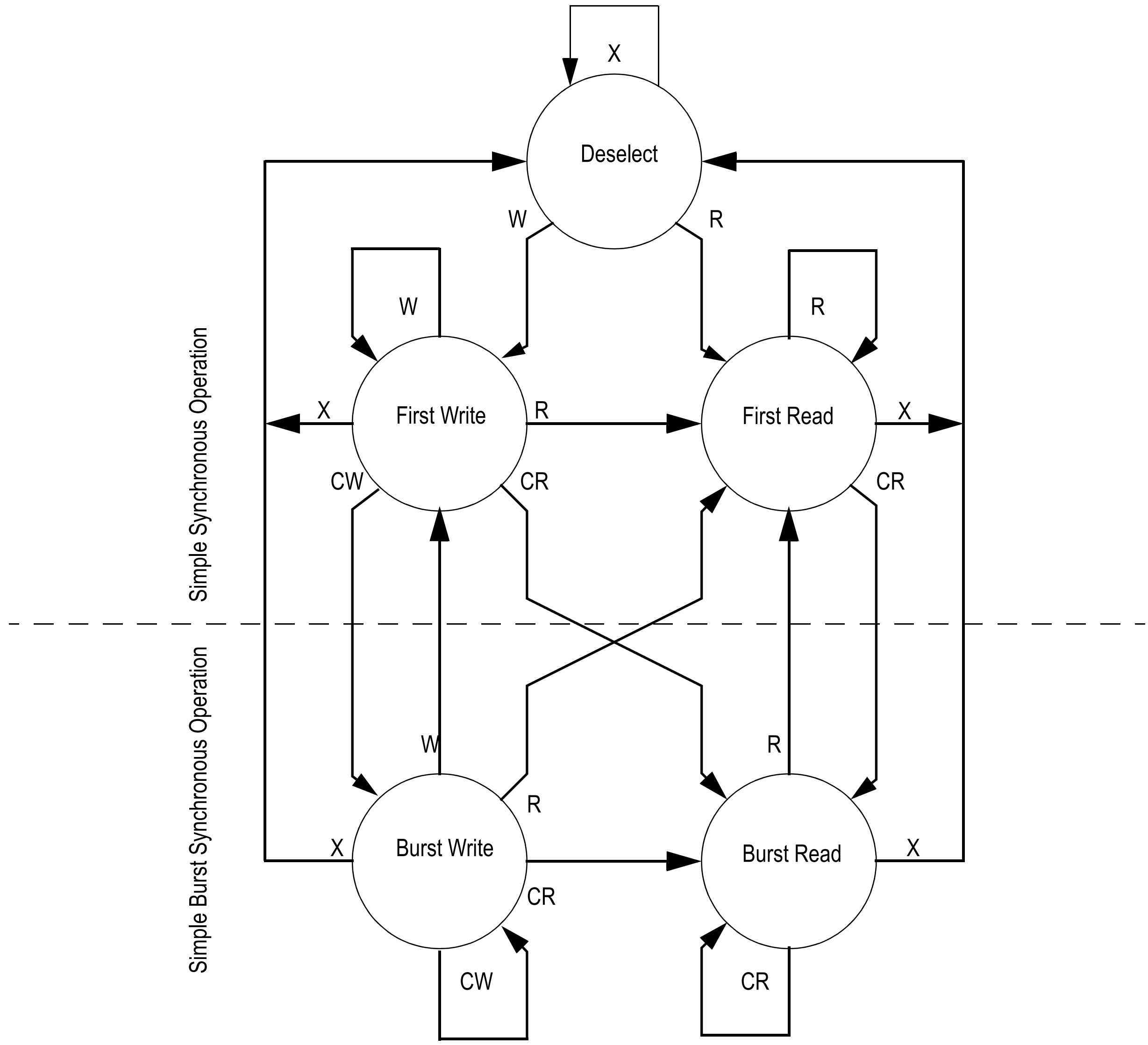
Notes:
1. All byte outputs are active in read cycles regardless of the state of Byte Write Enable inputs.
2. Byte Write Enable inputs $\overline{\text{B}}_\text{A}$, $\overline{\text{B}}_\text{B}$, $\overline{\text{B}}_\text{C}$, and/or $\overline{\text{B}}_\text{D}$ may be used in any combination with $\overline{\text{BW}}$ to write single or multiple bytes.
3. All byte I/Os remain High-Z during all write operations regardless of the state of Byte Write Enable inputs.
4. Bytes "C" and "D" are only available on the x32 and x36 versions.

Synchronous Truth Table

Operation	Address Used	State Diagram Key[5]	$\overline{E}_1$	E[2]	$\overline{\text{ADSP}}$	$\overline{\text{ADSC}}$	$\overline{\text{ADV}}$	$\overline{\text{W}}$[3]	DQ[4]
Deselect Cycle, Power Down	**None**	**X**	**H**	**X**	**X**	**L**	**X**	**X**	**High-Z**
Deselect Cycle, Power Down	None	X	L	F	L	X	X	X	High-Z
Deselect Cycle, Power Down	**None**	**X**	**L**	**F**	**H**	**L**	**X**	**X**	**High-Z**
Read Cycle, Begin Burst	External	R	L	T	L	X	X	X	Q
Read Cycle, Begin Burst	**External**	**R**	**L**	**T**	**H**	**L**	**X**	**F**	**Q**
Write Cycle, Begin Burst	**External**	**W**	**L**	**T**	**H**	**L**	**X**	**T**	**D**
Read Cycle, Continue Burst	*Next*	*CR*	*X*	*X*	*H*	*H*	*L*	*F*	*Q*
Read Cycle, Continue Burst	Next	CR	H	X	X	H	L	F	Q
Write Cycle, Continue Burst	*Next*	*CW*	*X*	*X*	*H*	*H*	*L*	*T*	*D*
Write Cycle, Continue Burst	Next	CW	H	X	X	H	L	T	D
Read Cycle, Suspend Burst	Current		X	X	H	H	H	F	Q
Read Cycle, Suspend Burst	Current		H	X	X	H	H	F	Q
Write Cycle, Suspend Burst	Current		X	X	H	H	H	T	D
Write Cycle, Suspend Burst	Current		H	X	X	H	H	T	D

Notes:
1. X = Don't Care, H = High, L = Low
2. E = T (True) if E_2 = 1; E = F (False) if E_2 = 0
3. $\overline{\text{W}}$ = T (True) and F (False) is defined in the Byte Write Truth Table preceding
4. $\overline{\text{G}}$ is an asynchronous input. $\overline{\text{G}}$ can be driven high at any time to disable active output drivers. $\overline{\text{G}}$ low can only enable active drivers (shown as "Q" in the Truth Table above).
5. All input combinations shown above are tested and supported. Input combinations shown in gray boxes need not be used to accomplish basic synchronous or synchronous burst operations and may be avoided for simplicity.
6. Tying $\overline{\text{ADSP}}$ high and $\overline{\text{ADSC}}$ low allows simple non-burst synchronous operations. See **BOLD** items above.
7. Tying $\overline{\text{ADSP}}$ high and $\overline{\text{ADV}}$ low while using $\overline{\text{ADSC}}$ to load new addresses allows simple burst operations. See *ITALIC* items above.

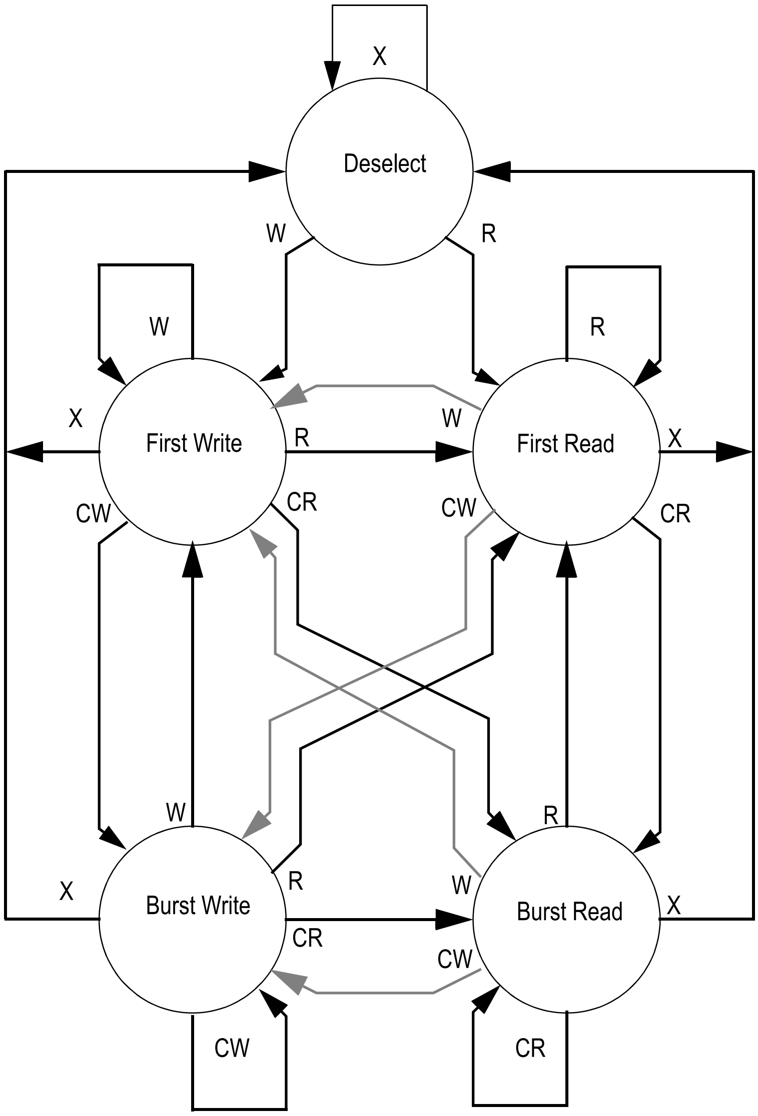
Simplified State Diagram



Notes:

1. The diagram shows only supported (tested) synchronous state transitions. The diagram presumes $\overline{G}$ is tied low.
2. The upper portion of the diagram assumes active use of only the Enable ($\overline{E1}$, E2, and $\overline{E3}$) and Write ($\overline{B_A}$, $\overline{B_B}$, $\overline{B_C}$, $\overline{B_D}$, $\overline{BW}$, and $\overline{GW}$) control inputs and that $\overline{ADSP}$ is tied high and $\overline{ADSC}$ is tied low.
3. The upper and lower portions of the diagram together assume active use of only the Enable, Write, and $\overline{ADSC}$ control inputs and assumes $\overline{ADSP}$ is tied high and $\overline{ADV}$ is tied low.

Simplified State Diagram with $\overline{G}$



Notes:
1. The diagram shows supported (tested) synchronous state transitions plus supported transitions that depend upon the use of $\overline{G}$.
2. Use of "Dummy Reads" (Read Cycles with $\overline{G}$ High) may be used to make the transition from read cycles to write cycles without passing through a Deselect cycle. Dummy Read cycles increment the address counter just like normal read cycles.
3. Transitions shown in grey tone assume $\overline{G}$ has been pulsed high long enough to turn the RAM's drivers off and for incoming data to meet Data Input Set Up Time.

Absolute Maximum Ratings

(All voltages reference to V_{SS})

Symbol	Description	Value	Unit
V_{DD}	Voltage on V_{DD} Pins	–0.5 to 4.6	V
V_{DDQ}	Voltage in V_{DDQ} Pins	–0.5 to 4.6	V
V_{CK}	Voltage on Clock Input Pin	–0.5 to 6	V
$V_{I/O}$	Voltage on I/O Pins	–0.5 to V_{DDQ} +0.5 (≤ 4.6 V max.)	V
V_{IN}	Voltage on Other Input Pins	–0.5 to V_{DD} +0.5 (≤ 4.6 V max.)	V
I_{IN}	Input Current on Any Pin	+/–20	mA
I_{OUT}	Output Current on Any I/O Pin	+/–20	mA
P_D	Package Power Dissipation	1.5	W
T_{STG}	Storage Temperature	–55 to 125	^oC
T_{BIAS}	Temperature Under Bias	–55 to 125	^oC

Note:
Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Exposure to conditions exceeding the Absolute Maximum Ratings, for an extended period of time, may affect reliability of this component.

Power Supply Voltage Ranges

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
3.3 V Supply Voltage	V_{DD3}	3.0	3.3	3.6	V	
2.5 V Supply Voltage	V_{DD2}	2.3	2.5	2.7	V	
3.3 V V_{DDQ} I/O Supply Voltage	V_{DDQ3}	3.0	3.3	3.6	V	
2.5 V V_{DDQ} I/O Supply Voltage	V_{DDQ2}	2.3	2.5	2.7	V	

Notes:
1. The part numbers of Industrial Temperature Range versions end the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.
2. Input Under/overshoot voltage must be –2 V > Vi < V_{DDn}+2 V not to exceed 4.6 V maximum, with a pulse width not to exceed 20% tKC.

V_{DDQ3} Range Logic Levels

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
V_{DD} Input High Voltage	V_{IH}	2.0	—	V_{DD} + 0.3	V	1
V_{DD} Input Low Voltage	V_{IL}	–0.3	—	0.8	V	1
V_{DDQ} I/O Input High Voltage	V_{IHQ}	2.0	—	V_{DDQ} + 0.3	V	1,3
V_{DDQ} I/O Input Low Voltage	V_{ILQ}	–0.3	—	0.8	V	1,3

Notes:
1. The part numbers of Industrial Temperature Range versions end the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.
2. Input Under/overshoot voltage must be –2 V > Vi < V_{DDn}+2 V not to exceed 4.6 V maximum, with a pulse width not to exceed 20% tKC.
3. V_{IHQ} (max) is voltage on V_{DDQ} pins plus 0.3 V.

V_{DDQ2} Range Logic Levels

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
V_{DD} Input High Voltage	V_{IH}	0.6*V_{DD}	—	V_{DD} + 0.3	V	1
V_{DD} Input Low Voltage	V_{IL}	–0.3	—	0.3*V_{DD}	V	1
V_{DDQ} I/O Input High Voltage	V_{IHQ}	0.6*V_{DD}	—	V_{DDQ} + 0.3	V	1,3
V_{DDQ} I/O Input Low Voltage	V_{ILQ}	–0.3	—	0.3*V_{DD}	V	1,3

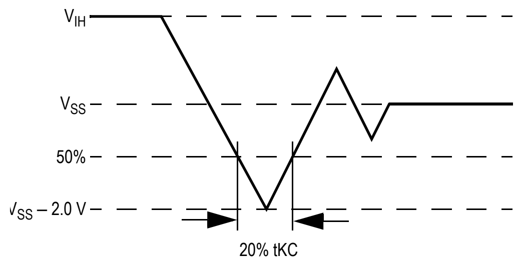
Notes:
1. The part numbers of Industrial Temperature Range versions end the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.
2. Input Under/overshoot voltage must be –2 V > Vi < V_{DDn}+2 V not to exceed 4.6 V maximum, with a pulse width not to exceed 20% tKC.
3. V_{IHQ} (max) is voltage on V_{DDQ} pins plus 0.3 V.

Recommended Operating Temperatures

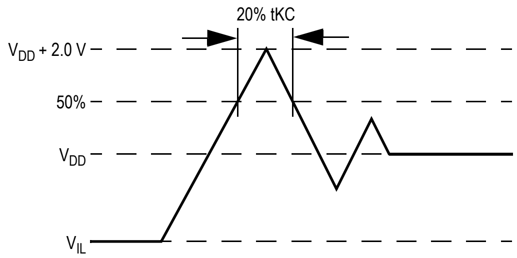
Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Ambient Temperature (Commercial Range Versions)	T_A	0	25	70	°C	2
Ambient Temperature (Industrial Range Versions)	T_A	–40	25	85	°C	2

Note:
1. The part numbers of Industrial Temperature Range versions end the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.
2. Input Under/overshoot voltage must be –2 V > Vi < V_{DDn}+2 V not to exceed 4.6 V maximum, with a pulse width not to exceed 20% tKC.

Undershoot Measurement and Timing



Overshoot Measurement and Timing



Capacitance

(T_A = 25°C, f = 1 MHz, V_{DD} = 2.5 V)

Parameter	Symbol	Test conditions	Typ.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0 V	4	5	pF
Input/Output Capacitance	$C_{I/O}$	V_{OUT} = 0 V	6	7	pF

Note: These parameters are sample tested.

Package Thermal Characteristics

Rating	Layer Board	Symbol	Max	Unit	Notes
Junction to Ambient (at 200 lfm)	single	$R_{\Theta JA}$	40	°C/W	1,2
Junction to Ambient (at 200 lfm)	four	$R_{\Theta JA}$	24	°C/W	1,2
Junction to Case (TOP)	—	$R_{\Theta JC}$	9	°C/W	3

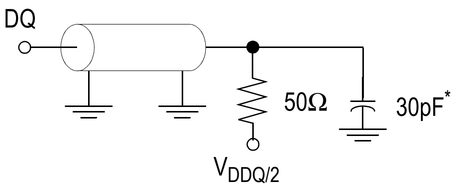
Notes:
1. Junction temperature is a function of SRAM power dissipation, package thermal resistance, mounting board temperature, ambient. Temperature air flow, board density, and PCB thermal resistance.
2. SCMI G-38-87
3. Average thermal resistance between die and top surface, MIL SPEC-883, Method 1012.1

AC Test Conditions

Parameter	Conditions
Input high level	V_{DD} – 0.2 V
Input low level	0.2 V
Input slew rate	1 V/ns
Input reference level	$V_{DD}/2$
Output reference level	$V_{DDQ}/2$
Output load	**Fig. 1**

Notes:
1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in **Fig. 1** unless otherwise noted.
3. Device is deselected as defined by the Truth Table.

Output Load 1



* Distributed Test Jig Capacitance

DC Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Max
Input Leakage Current (except mode pins)	I_{IL}	V_{IN} = 0 to V_{DD}	–1 uA	1 uA
ZZ Input Current	I_{IN1}	$V_{DD} \geq V_{IN} \geq V_{IH}$ $0\ V \leq V_{IN} \leq V_{IH}$	–1 uA –1 uA	1 uA 100 uA
$\overline{FT}$ Input Current	I_{IN2}	$V_{DD} \geq V_{IN} \geq V_{IL}$ $0\ V \leq V_{IN} \leq V_{IL}$	–100 uA –1 uA	1 uA 1 uA
Output Leakage Current	I_{OL}	Output Disable, V_{OUT} = 0 to V_{DD}	–1 uA	1 uA
Output High Voltage	V_{OH2}	I_{OH} = –8 mA, V_{DDQ} = 2.375 V	1.7 V	—
Output High Voltage	V_{OH3}	I_{OH} = –8 mA, V_{DDQ} = 3.135 V	2.4 V	—
Output Low Voltage	V_{OL}	I_{OL} = 8 mA	—	0.4 V

Operating Currents

Parameter	Test Conditions	Mode		Symbol	-5.5		-6		-6.5		-7		-7.5		-8.5		Unit
					0 to 70°C	–40 to 85°C	0 to 70°C	–40 to 85°C	0 to 70°C	–40 to 85°C	0 to 70°C	–40 to 85°C	0 to 70°C	–40 to 85°C	0 to 70°C	–40 to 85°C	
Operating Current **3.3 V**	Device Selected; All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ Output open	**(x36/ x32)**	Flow Through	I_{DD} I_{DDQ}	180 20	190 20	170 20	180 20	165 15	175 15	155 15	165 15	150 15	160 15	140 10	150 10	mA
		(x18)	Flow Through	I_{DD} I_{DDQ}	165 10	175 10	155 10	165 10	150 10	160 10	140 10	150 10	135 10	145 10	125 10	135 10	mA
Operating Current **2.5 V**	Device Selected; All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ Output open	**(x36/ x32)**	Flow Through	I_{DD} I_{DDQ}	180 20	190 20	170 20	180 20	165 15	175 15	155 15	165 15	150 15	160 15	140 10	150 10	mA
		(x18)	Flow Through	I_{DD} I_{DDQ}	165 10	175 10	155 10	165 10	150 10	160 10	140 10	150 10	135 10	145 10	125 10	135 10	mA
Standby Current	$ZZ \geq V_{DD} - 0.2$ V		Flow Through	I_{SB}	20	30	20	30	20	30	20	30	20	30	20	30	mA
Deselect Current	Device Deselected; All other inputs $\geq V_{IH}$ or $\leq V_{IL}$		Flow Through	I_{DD}	60	65	50	55	50	55	50	55	50	55	45	50	mA

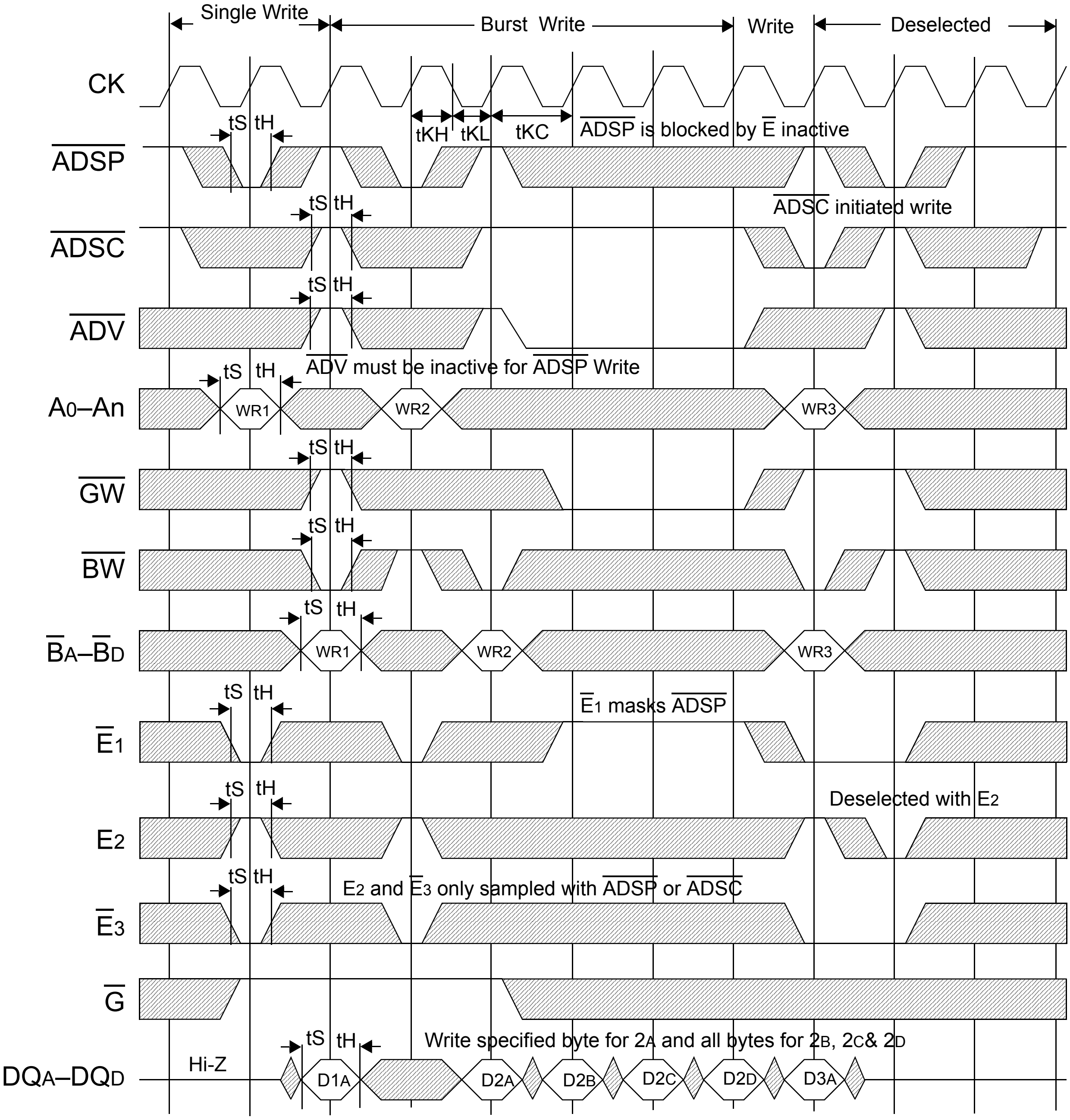
Notes:
1. I_{DD} and I_{DDQ} apply to any combination of V_{DD3}, V_{DD2}, V_{DDQ3}, and V_{DDQ2} operation.
2. All parameters listed are worst case scenario.

AC Electrical Characteristics

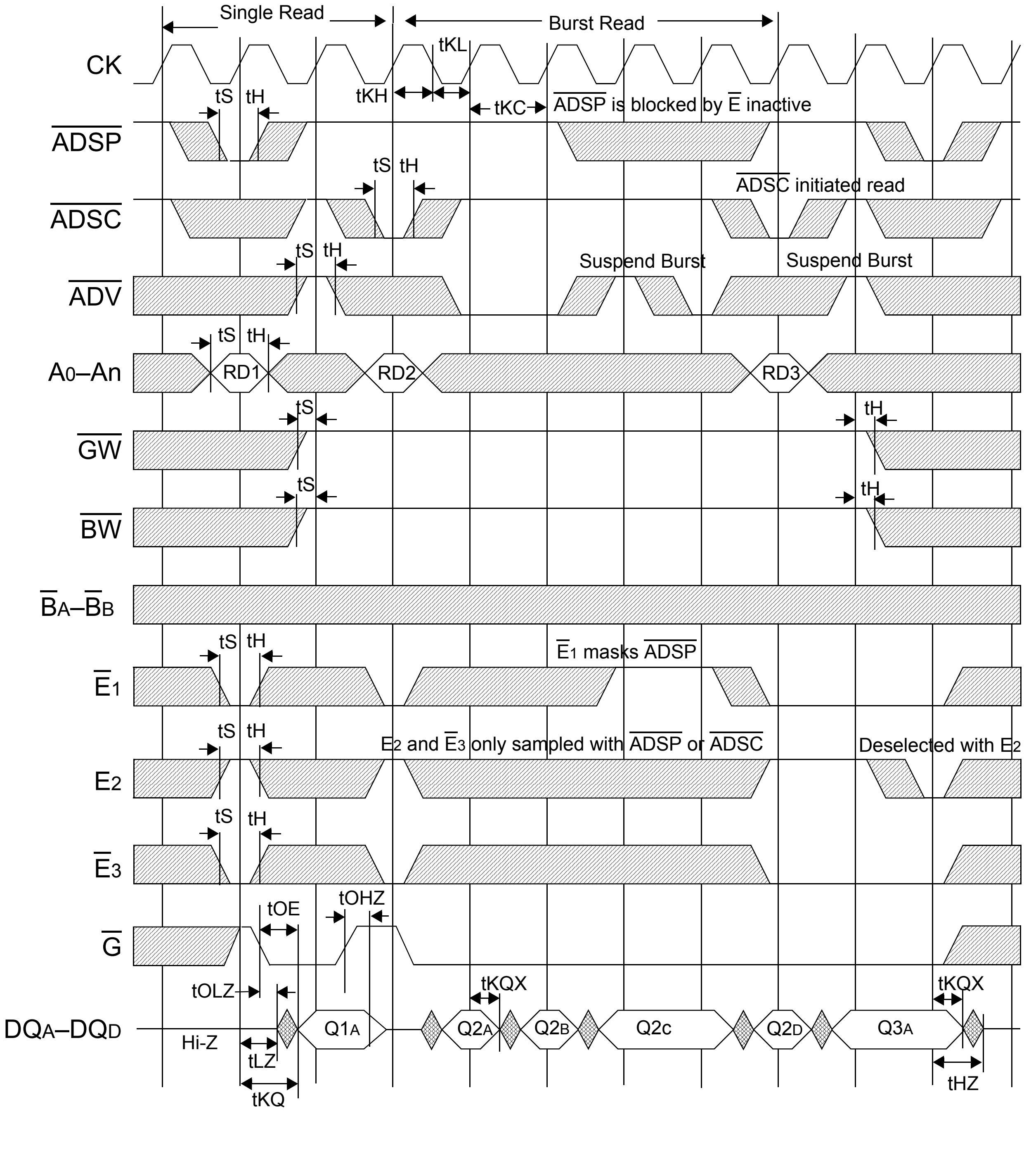
	Parameter	Symbol	-5.5		-6		-6.5		-7		-7.5		-8.5		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Flow Through	Clock Cycle Time	tKC	5.5	—	6.0	—	6.5	—	7.0	—	7.5	—	8.5	—	ns
	Clock to Output Valid	tKQ	—	5.5	—	6.0	—	6.5	—	7.0	—	7.5	—	8.5	ns
	Clock to Output Invalid	tKQX	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns
	Clock to Output in Low-Z	tLZ[1]	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns
	Setup time	tS	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
	Hold time	tH	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns
	Clock HIGH Time	tKH	1.3	—	1.3	—	1.3	—	1.3	—	1.5	—	1.7	—	ns
	Clock LOW Time	tKL	1.5	—	1.5	—	1.5	—	1.5	—	1.7	—	2	—	ns
	Clock to Output in High-Z	tHZ[1]	1.5	2.3	1.5	2.5	1.5	3.0	1.5	3.0	1.5	3.0	1.5	3.0	ns
	$\overline{G}$ to Output Valid	tOE	—	2.3	—	2.5	—	3.2	—	3.5	—	3.8	—	4.0	ns
	$\overline{G}$ to output in Low-Z	tOLZ[1]	0	—	0	—	0	—	0	—	0	—	0	—	ns
	$\overline{G}$ to output in High-Z	tOHZ[1]	—	2.3	—	2.5	—	3.0	—	3.0	—	3.0	—	3.0	ns
	ZZ setup time	tZZS[2]	5	—	5	—	5	—	5	—	5	—	5	—	ns
	ZZ hold time	tZZH[2]	1	—	1	—	1	—	1	—	1	—	1	—	ns
	ZZ recovery	tZZR	20	—	20	—	20	—	20	—	20	—	20	—	ns

Notes:
1. These parameters are sampled and are not 100% tested.
2. ZZ is an asynchronous signal. However, In order to be recognized on any given clock cycle, ZZ must meet the specified setup and hold times as specified above.

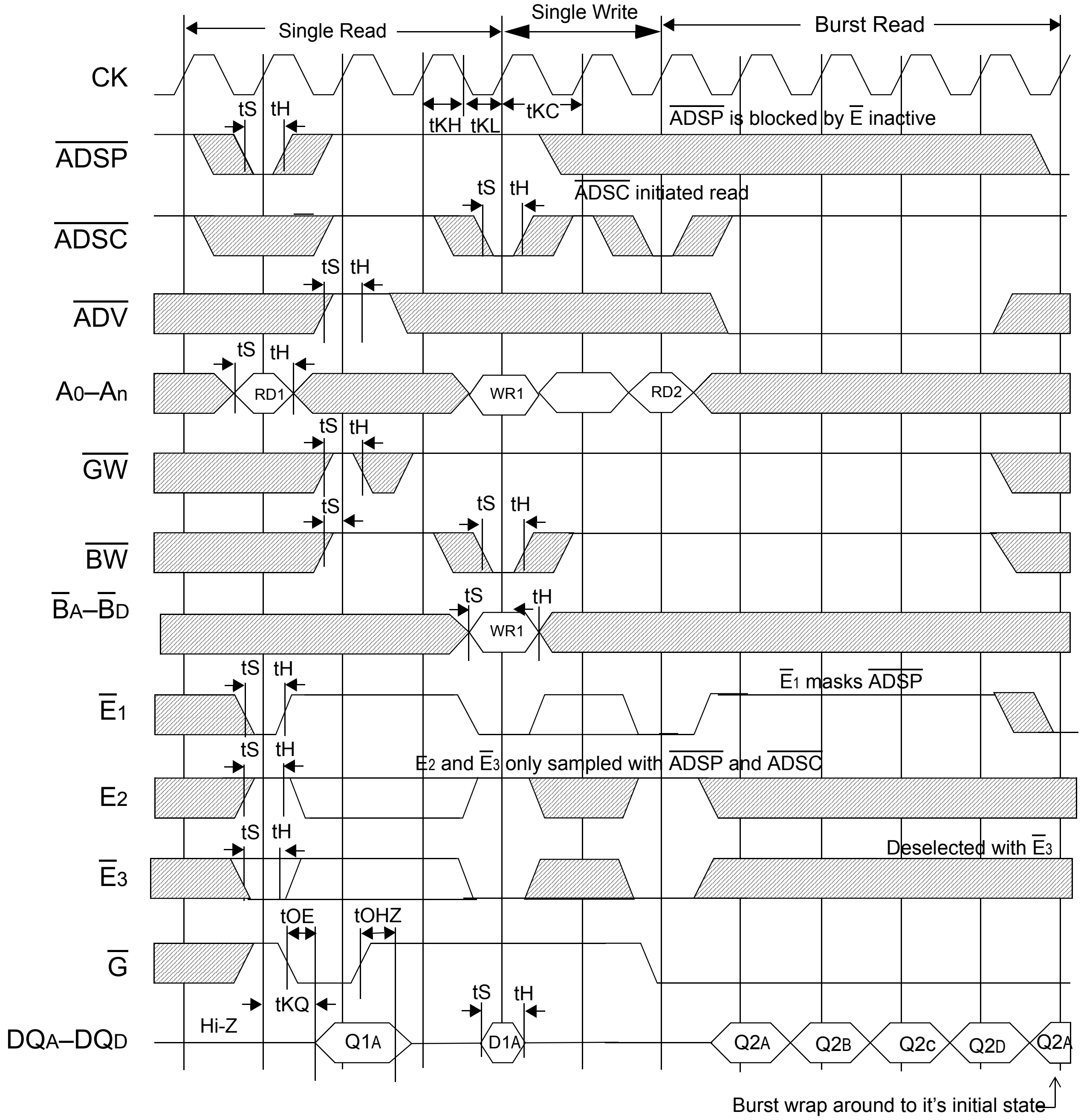
Write Cycle Timing



Flow Through Read Cycle Timing



Flow Through Read-Write Cycle Timing

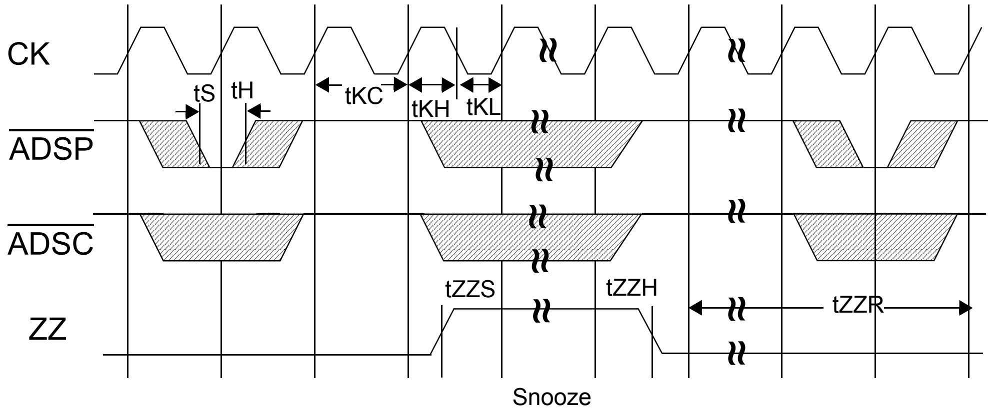


Sleep Mode

During normal operation, ZZ must be pulled low, either by the user or by its internal pull down resistor. When ZZ is pulled high, the SRAM will enter a Power Sleep mode after 2 cycles. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM operates normally after ZZ recovery time.

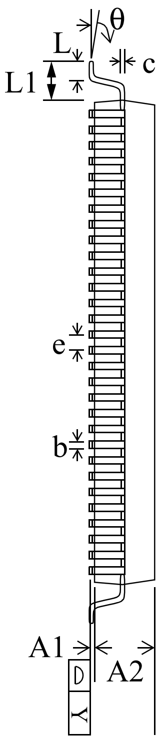
Sleep mode is a low current, power-down mode in which the device is deselected and current is reduced to $I_{SB}2$. The duration of Sleep mode is dictated by the length of time the ZZ is in a High state. After entering Sleep mode, all inputs except ZZ become disabled and all outputs go to High-Z The ZZ pin is an asynchronous, active high input that causes the device to enter Sleep mode. When the ZZ pin is driven high, $I_{SB}2$ is guaranteed after the time tZZI is met. Because ZZ is an asynchronous input, pending operations or operations in progress may not be properly completed if ZZ is asserted. Therefore, Sleep mode must not be initiated until valid pending operations are completed. Similarly, when exiting Sleep mode during tZZR, only a Deselect or Read commands may be applied while the SRAM is recovering from Sleep mode.

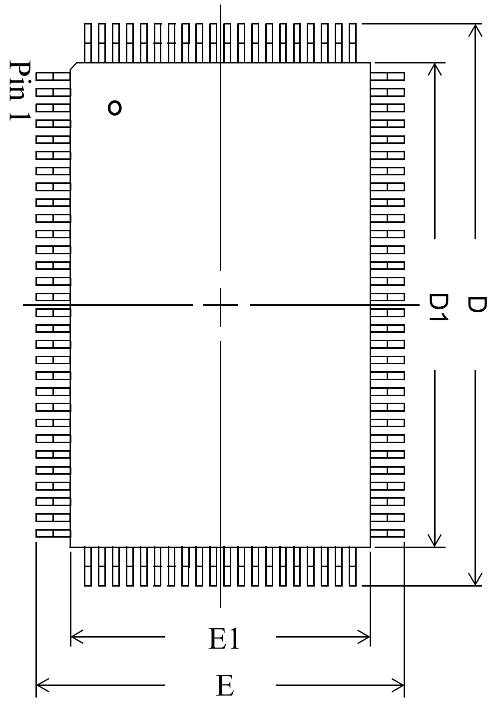
Sleep Mode Timing Diagram



TQFP Package Drawing

Symbol	Description	Min.	Nom.	Max
A1	Standoff	0.05	0.10	0.15
A2	Body Thickness	1.35	1.40	1.45
b	Lead Width	0.20	0.30	0.40
c	Lead Thickness	0.09	—	0.20
D	Terminal Dimension	21.9	22.0	22.1
D1	Package Body	19.9	20.0	20.1
E	Terminal Dimension	15.9	16.0	16.1
E1	Package Body	13.9	14.0	14.1
e	Lead Pitch	—	0.65	—
L	Foot Length	0.45	0.60	0.75
L1	Lead Length	—	1.00	—
Y	Coplanarity	—	—	0.10
θ	Lead Angle	0°	—	7°





Notes:
1. All dimensions are in millimeters (mm).
2. Package width and length do not include mold protrusion.

Ordering Information for GSI Synchronous Burst RAMs

Org	Part Number[1]	Type	Package	Speed[2] (MHz/ns)	T_A[3]	Status
512K x 18	GS880F18AT-5.5	Flow Through	TQFP	5.5	C	
512K x 18	GS880F18AT-6	Flow Through	TQFP	6.0	C	
512K x 18	GS880F18AT-6.5	Flow Through	TQFP	6.5	C	
512K x 18	GS880F18AT-7	Flow Through	TQFP	7.0	C	
512K x 18	GS880F18AT-7.5	Flow Through	TQFP	7.5	C	
512K x 18	GS880F18AT-8.5	Flow Through	TQFP	8.5	C	
256K x 32	GS880F32AT-5.5	Flow Through	TQFP	5.5	C	
256K x 32	GS880F32AT-6	Flow Through	TQFP	6.0	C	
256K x 32	GS880F32AT-6.5	Flow Through	TQFP	6.5	C	
256K x 32	GS880F32AT-7	Flow Through	TQFP	7.0	C	
256K x 32	GS880F32AT-7.5	Flow Through	TQFP	7.5	C	
256K x 32	GS880F32AT-8.5	Flow Through	TQFP	8.5	C	
256K x 36	GS880F36AT-5.5	Flow Through	TQFP	5.5	C	
256K x 36	GS880F36AT-6	Flow Through	TQFP	6.0	C	
256K x 36	GS880F36AT-6.5	Flow Through	TQFP	6.5	C	
256K x 36	GS880F36AT-7	Flow Through	TQFP	7.0	C	
256K x 36	GS880F36AT-7.5	Flow Through	TQFP	7.5	C	
256K x 36	GS880F36AT-8.5	Flow Through	TQFP	8.5	C	
512K x 18	GS880F18AT-5.5I	Flow Through	TQFP	5.5	I	
512K x 18	GS880F18AT-6I	Flow Through	TQFP	6.0	I	
512K x 18	GS880F18AT-6.5I	Flow Through	TQFP	6.5	I	
512K x 18	GS880F18AT-7I	Flow Through	TQFP	7.0	I	
512K x 18	GS880F18AT-7.5I	Flow Through	TQFP	7.5	I	
512K x 18	GS880F18AT-8I	Flow Through	TQFP	8.5	I	
256K x 32	GS880F32AT-5.5I	Flow Through	TQFP	5.5	I	
256K x 32	GS880F32AT-6I	Flow Through	TQFP	6.0	I	
256K x 32	GS880F32AT-6.5I	Flow Through	TQFP	6.5	I	
256K x 32	GS880F32AT-7I	Flow Through	TQFP	7.0	I	
256K x 32	GS880F32AT-7.5I	Flow Through	TQFP	7.5	I	
256K x 32	GS880F32AT-8.5I	Flow Through	TQFP	8.5	I	

Notes:
1. Customers requiring delivery in Tape and Reel should add the character “T” to the end of the part number. Example: GS880F18-6T.
2. The speed column indicates the cycle frequency (MHz) of the device in Pipeline mode and the latency (ns) in Flow Through mode. Each device is Pipeline/Flow through mode-selectable by the user.
3. T_A = C = Commercial Temperature Range. T_A = I = Industrial Temperature Range.
4. GSI offers other versions this type of device in many different configurations and with a variety of different features, only some of which are covered in this data sheet. See the GSI Technology web site (www.gsitechnology.com) for a complete listing of current offerings.

Org	Part Number[1]	Type	Package	Speed[2] (MHz/ns)	T_A[3]	Status
256K x 36	GS880F36AT-5.5I	Flow Through	TQFP	5.5	I	
256K x 36	GS880F36AT-6I	Flow Through	TQFP	6.0	I	
256K x 36	GS880F36AT-6.5I	Flow Through	TQFP	6.5	I	
256K x 36	GS880F36AT-7I	Flow Through	TQFP	7.0	I	
256K x 36	GS880F36AT-7.5I	Flow Through	TQFP	7.5	I	
256K x 36	GS880F36AT-8.5I	Flow Through	TQFP	8.5	I	

Notes:
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9Mb Sync SRAM Datasheet Revision History

DS/DateRev. Code: Old; New	Types of Changes Format or Content	Page;Revisions;Reason
880F18A_r1		• Creation of new datasheet
880F18A_r1; 880F18A_r1_01	Content	• Updated FT power numbers • Updated AC Characteristics table • Changed 8Mb references to 9Mb • Updated ZZ recovery time diagram • Updated AC Test Conditions table and removed Output Load 2 diagram
880F18A_r1_01; 880F18A_r1_02	Content	• Removed Preliminary banner • Removed pin locations in pin description table