HARRIS SEMICONDUCTOR

CA555, LM555

Timers for Timing Delays and Oscillator Applications in Commercial, Industrial and Military Equipment

March 1993

Features

- Accurate Timing from Microseconds through Hours
- Astable and Monostable Operation
- Adjustable Duty Cycle
- Output Capable of Sourcing or Sinking up to 200mA
- Output Capable of Driving TTL Devices
- Normally ON and OFF Outputs
- High Temperature Stability . . . . . 0.005%/°C
- Directly Interchangeable with SE555, NE555, MC1555, and MC1455

Applications

- Precision Timing
- Sequential Timing
- Time Delay Generation
- Pulse Generation
- Pulse Detector
- Pulse Width and Position Modulation

Ordering Information

PART NO.	TEMP. RANGE	PACKAGE
CA0555E	-55°C to +125°C	8 Lead Plastic DIP
CA0555M	-55°C to +125°C	8 Lead SOIC
CA0555M96	-55°C to +125°C	8 Lead SOIC*
CA0555T	-55°C to +125°C	8 Pin TO-5 Metal Can
CA0555CE	0°C to +70°C	8 Lead Plastic DIP
CA0555CM	0°C to +70°C	8 Lead SOIC
CA0555CM96	0°C to +70°C	8 Lead SOIC*
CA0555CT	0°C to +70°C	8 Pin TO-5 Metal Can
LM555N	0°C to +70°C	8 Lead Plastic DIP
LM555CN	0°C to +70°C	8 Lead Plastic DIP

* Denotes Tape and Reel

Description

The CA555 and CA555C are highly stable timers for use in precision timing and oscillator applications. As timers, these monolithic integrated circuits are capable of producing accurate time delays for periods ranging from microseconds through hours. These devices are also useful for astable oscillator operation and can maintain an accurately controlled free running frequency and duty cycle with only two external resistors and one capacitor.

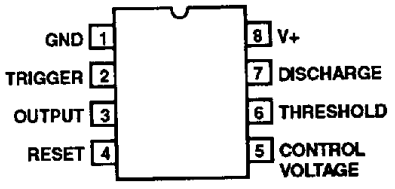
The circuits of the CA555 and CA555C may be triggered by the falling edge of the waveform signal, and the output of these circuits can source or sink up to a 200mA current or drive TTL circuits.

These types are direct replacements for industry types in packages with similar terminal arrangements e.g. SE555 and NE555, MC1555 and MC1455, respectively. The CA555 type circuits are intended for applications requiring premium electrical performance. The CA555C type circuits are intended for applications requiring less stringent electrical characteristics.

Technical data on LM branded types is identical to the corresponding CA branded types.

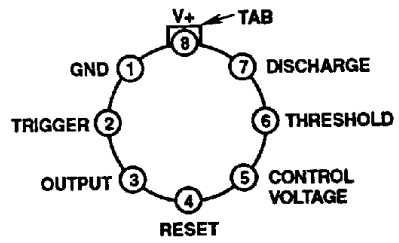
Pinouts

CA555, CA555C, LM555C (PDIP, SOIC)
TOP VIEW

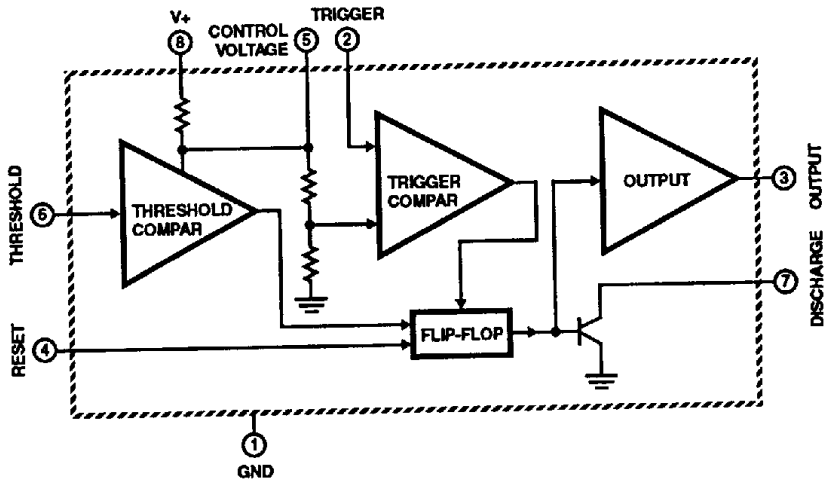


TO-5 Style Package with Formed Leads

CA555, CA555C, LM555C (METAL CAN)
TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 834.2

Specifications CA555, CA555C, LM555

Absolute Maximum Ratings

DC Supply Voltage 18V
Power Dissipation
Up to T_A = +55°C 600mW
Above T_A = +55°C ..... Derate Linearly 5mW/°C
Junction Temperature ..... +175°C
Junction Temperature (Plastic Packages) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range
CA555 ..... -55°C to +125°C
CA555C ..... 0°C to +70°C
Storage Temperature Range ..... -65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

T_A = +25°C, V+ = 5V to 15V Unless Otherwise Specified

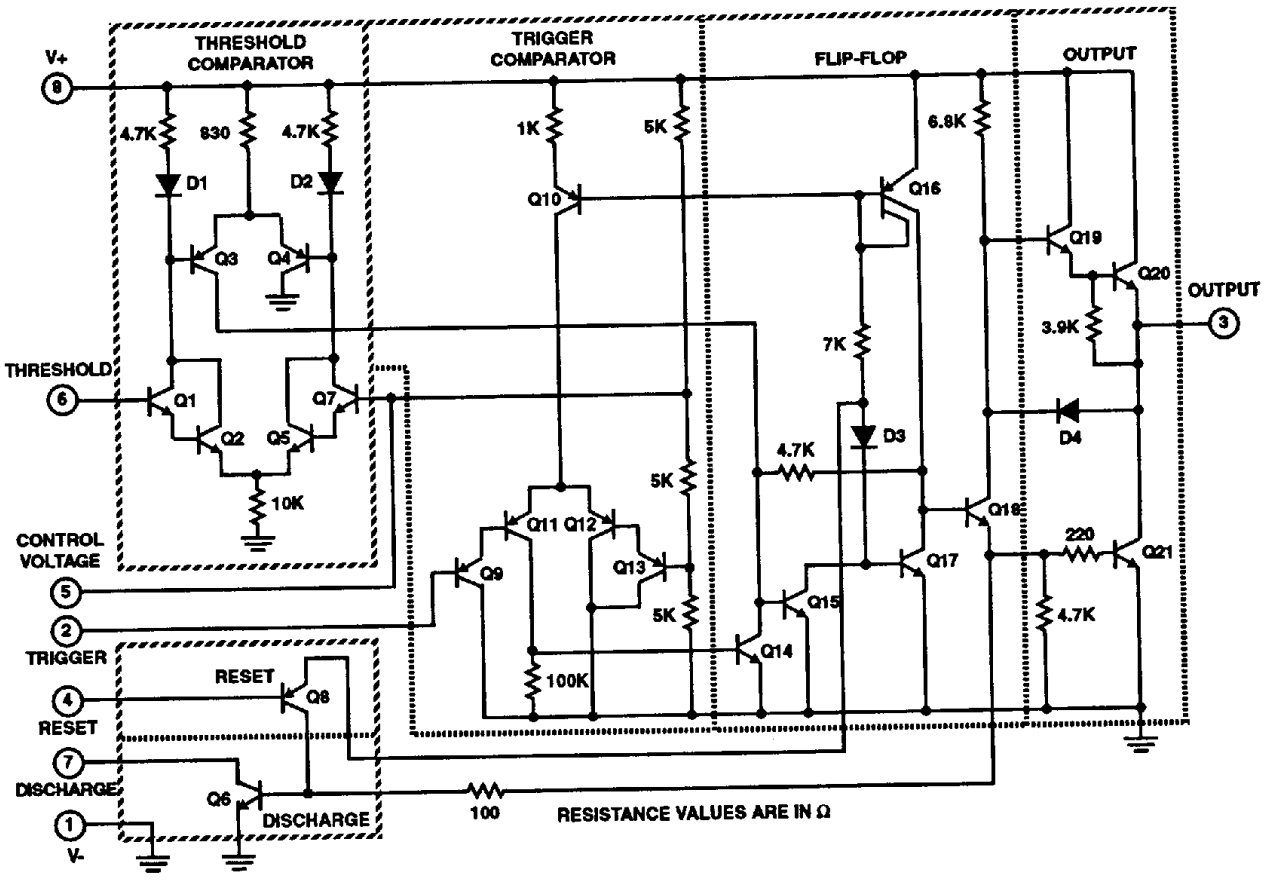
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS						UNITS
			CA555			CA555C			
			MIN	TYP	MAX	MIN	TYP	MAX	
DC Supply Voltage	V+		4.5	-	18	4.5	-	16	V
DC Supply Current (Low State), Note 1	I+	V+ = 5V, R_L = ∞	-	3	5	-	3	6	mA
		V+ = 15V, R_L = ∞	-	10	12	-	10	15	mA
Threshold Voltage	V_{TH}		-	$(^2/_3)$V+	-	-	$(^2/_3)$V+	-	V
Trigger Voltage		V+ = 5V	1.45	1.67	1.9	-	1.67	-	V
		V+ = 15V	4.8	5	5.2	-	5	-	V
Trigger Current			-	0.5	-	-	0.5	-	µA
Threshold Current, Note 2	I_{TH}		-	0.1	0.25	-	0.1	0.25	µA
Reset Voltage			0.4	0.7	1.0	0.4	0.7	1.0	V
Reset Current			-	0.1	-	-	0.1	-	mA
Control Voltage Level		V+ = 5V	2.9	3.33	3.8	2.6	3.33	4	V
		V+ = 15V	9.6	10	10.4	9	10	11	V
Output Voltage Low State	V_{OL}	V+ = 5V, I_{SINK} = 5mA	-	-	-	-	0.25	0.35	V
		I_{SINK} = 8mA	-	0.1	0.25	-	-	-	V
		V+ = 15V, I_{SINK} = 10mA	-	0.1	0.15	-	0.1	0.25	V
		I_{SINK} = 50mA	-	0.4	0.5	-	0.4	0.75	V
		I_{SINK} = 100mA	-	2.0	2.2	-	2.0	0.5	V
		I_{SINK} = 200mA	-	2.5	-	-	2.5	-	V
Output Voltage High State	V_{OH}	V+ = 5V, I_{SOURCE} = 100mA	3.0	3.3	-	2.75	3.3	-	V
		V+ = 15V, I_{SOURCE} = 100mA	13.0	13.3	-	12.75	13.3	-	V
		I_{SOURCE} = 200mA	-	12.5	-	-	12.5	-	V
Timing Error (Monostable)		R_1, R_2 = 1kΩ to 100kΩ, C = 0.1µF Tested at V+ = 5V, V+ = 15V	-	0.5	2	-	1	-	%
Frequency Drift with Temperature			-	30	100	-	50	-	ppm/°C
Drift with Supply Voltage			-	0.05	0.2	-	0.1	-	%/V
Output Rise Time	t_R		-	100	-	-	100	-	ns
Output Fall Time	t_F		-	100	-	-	100	-	ns

NOTES:

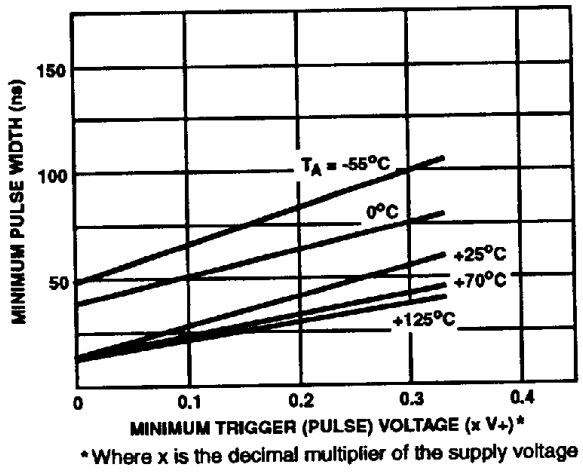
1. When the output is in a high state, the DC supply current is typically 1mA less than the low state value.
2. The threshold current will determine the sum of the values of R_1 and R_2 to be used in Figure 14 (astable operation); the maximum total $R_1 + R_2$ = 20MΩ.

Schematic Diagram

CA555 AND CA555C



Typical Performance Curves



*Where x is the decimal multiplier of the supply voltage

FIGURE 1. MINIMUM PULSE WIDTH vs MINIMUM TRIGGER VOLTAGE

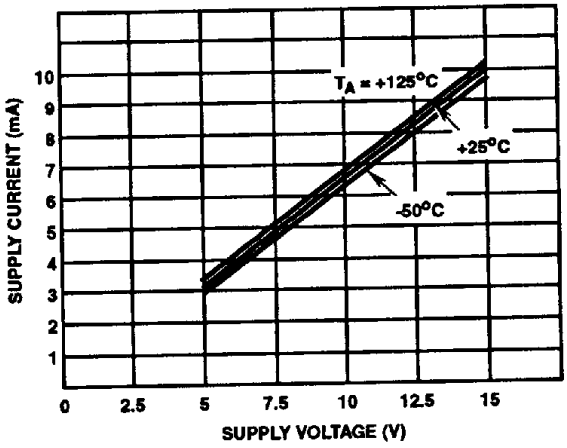


FIGURE 2. SUPPLY CURRENT vs SUPPLY VOLTAGE

Typical Performance Curves

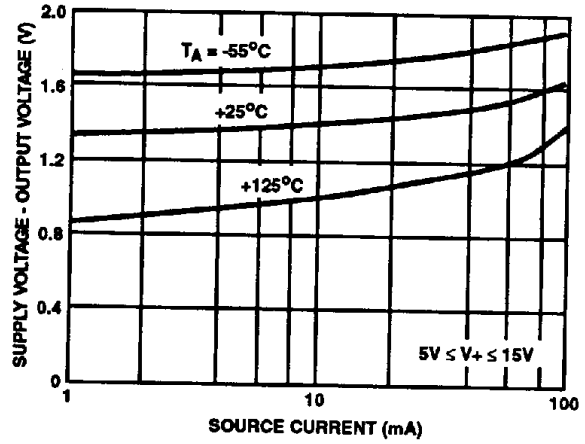


FIGURE 3. OUTPUT VOLTAGE DROP (HIGH STATE) vs SOURCE CURRENT

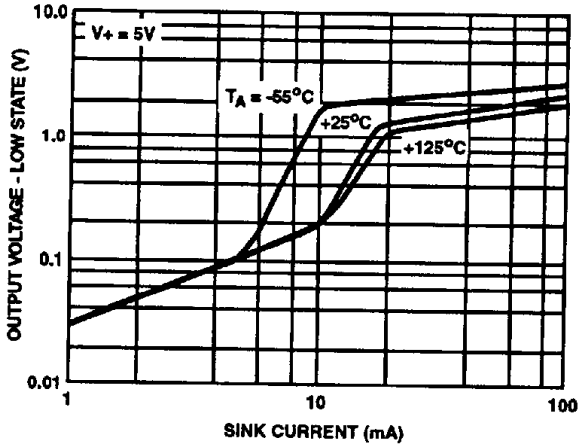


FIGURE 4. OUTPUT VOLTAGE LOW STATE vs SINK CURRENT AT V+ = 5V

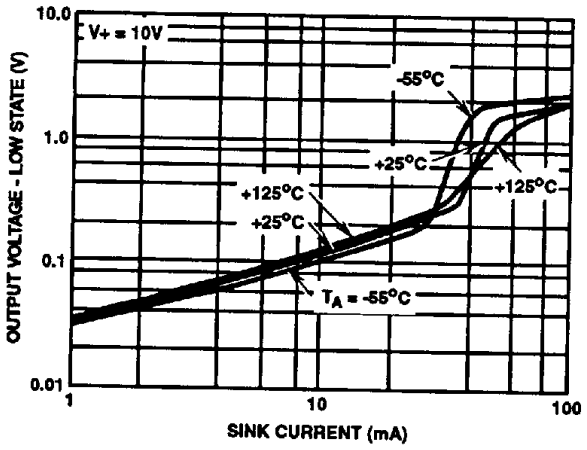


FIGURE 5. OUTPUT VOLTAGE LOW STATE vs SINK CURRENT AT V+ = 10V

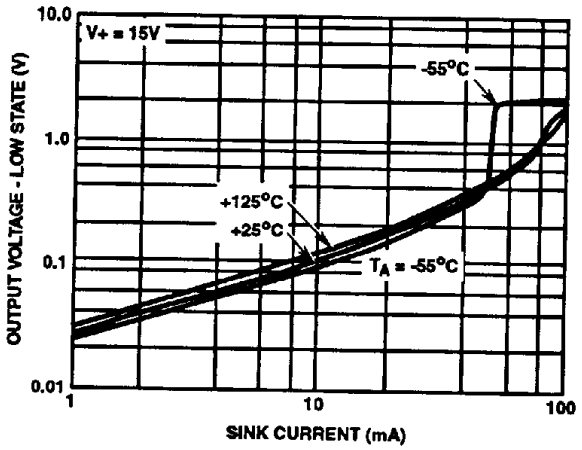


FIGURE 6. OUTPUT VOLTAGE LOW STATE vs SINK CURRENT AT V+ = 15V

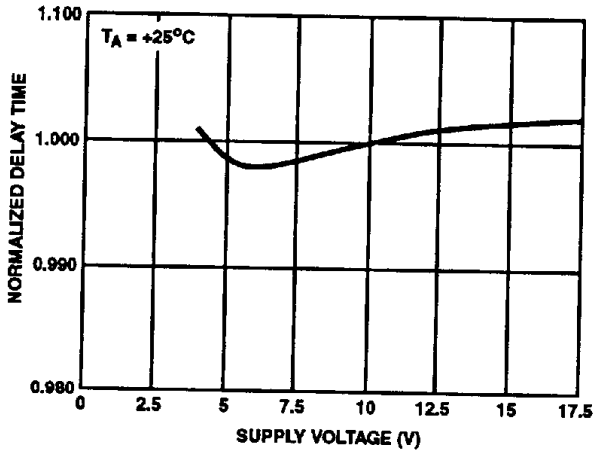


FIGURE 7. DELAY TIME vs SUPPLY VOLTAGE

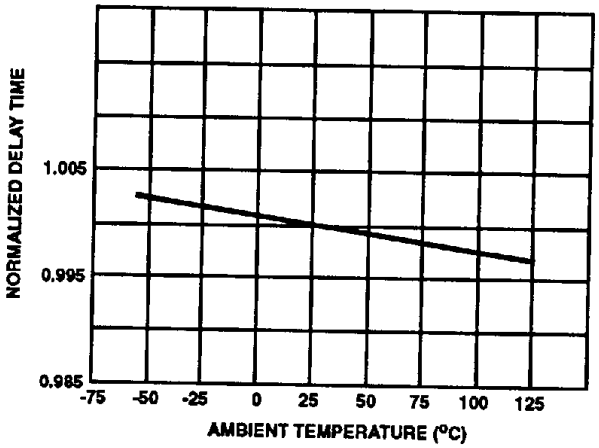


FIGURE 8. DELAY TIME vs TEMPERATURE

Typical Performance Curves

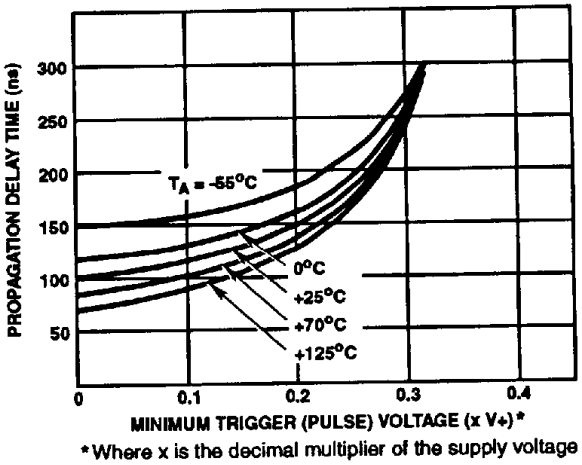


FIGURE 9. PROPAGATION DELAY TIME vs TRIGGER VOLTAGE

Typical Applications

Reset Timer (Monostable Operation)

Figure 10 shows the CA555 connected as a reset timer. In this mode of operation capacitor C_T is initially held discharged by a transistor on the integrated circuit. Upon closing the "start" switch, or applying a negative trigger pulse to terminal 2, the integral timer flip-flop is "set" and releases the short circuit across C_T which drives the output voltage "high" (relay energized). The action allows the voltage across the capacitor to increase exponentially with the constant $t = R_1C_T$. When the voltage across the capacitor equals 2/3 V+, the comparator resets the flip-flop which in turn discharges the capacitor rapidly and drives the output to its low state.

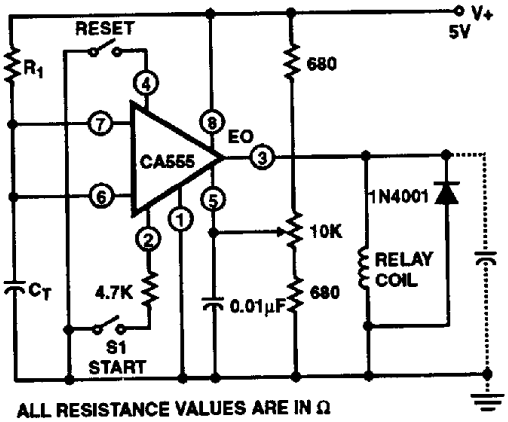


FIGURE 10. RESET TIMER (MONOSTABLE OPERATION)

Since the charge rate and threshold level of the comparator are both directly proportional to V+, the timing interval is relatively independent of supply voltage variations. Typically, the timing varies only 0.05% for a 1V change in V+.

Applying a negative pulse simultaneously to the reset terminal (4) and the trigger terminal (2) during the timing cycle discharges C_T and causes the timing cycle to restart. Momentarily closing only the reset switch during the timing interval discharges C_T, but the timing cycle does not restart.

Figure 11 shows the typical waveforms generated during this mode of operation, and Figure 12 gives the family of time delay curves with variations in R_1 and C_T.

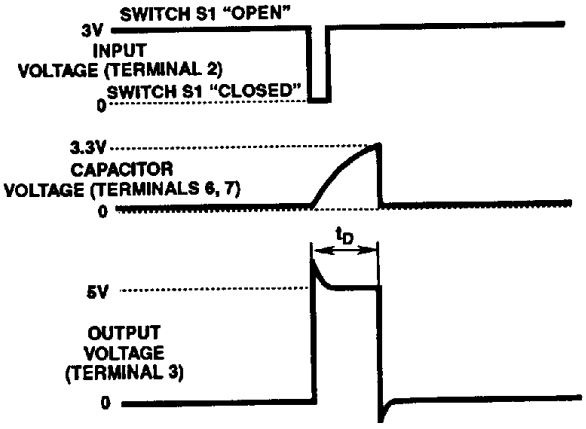


FIGURE 11. TYPICAL WAVEFORMS FOR RESET TIMER

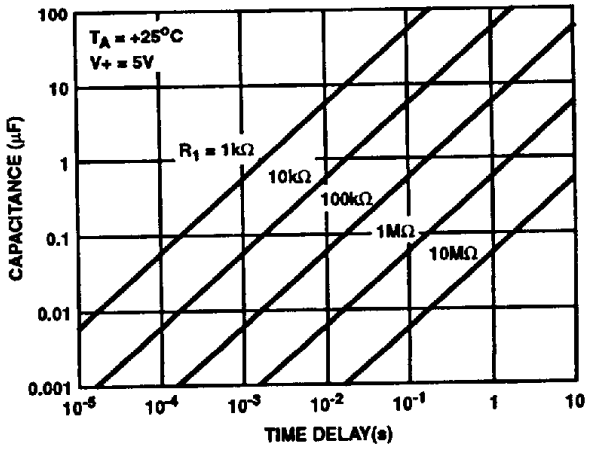


FIGURE 12. TIME DELAY vs RESISTANCE AND CAPACITANCE

Repeat Cycle Timer (Astable Operation)

Figure 13 shows the CA555 connected as a repeat cycle timer. In this mode of operation, the total period is a function of both R_1 and R_2.

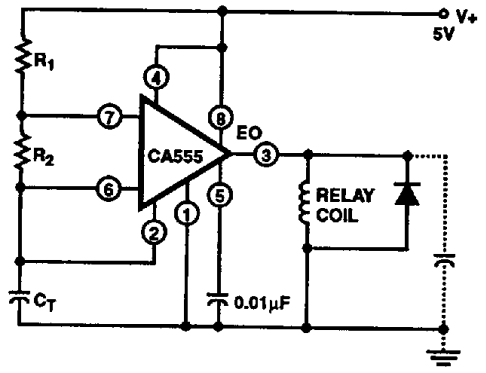


FIGURE 13. REPEAT CYCLE TIMER (ASTABLE OPERATION)

$$T = 0.693\ (R_1 + 2R_2)\ C_T = t_1 + t_2$$

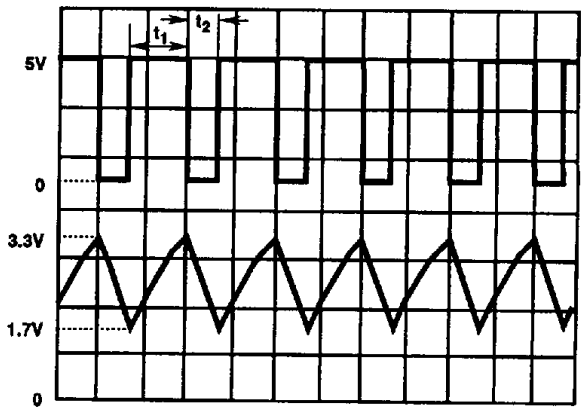
where $t_1 = 0.693\ (R_1 + R_2)\ C_T$

and $t_2 = 0.693\ (R_2)\ C_T$

the duty cycle is:

$$\frac{t_1}{t_1 + t_2} = \frac{R_1 + R_2}{R_1 + 2R_2}$$

Typical waveforms generated during this mode of operation are shown in Figure 14. Figure 15 gives the family of curves of free running frequency with variations in the value of (R_1 + $2R_2$) and C_T.



Top Trace: Output voltage (2V/div. and 0.5ms/div.)
Bottom Trace: Capacitor voltage (1V/div. and 0.5ms/div.)

FIGURE 14. TYPICAL WAVEFORMS FOR REPEAT CYCLE TIMER

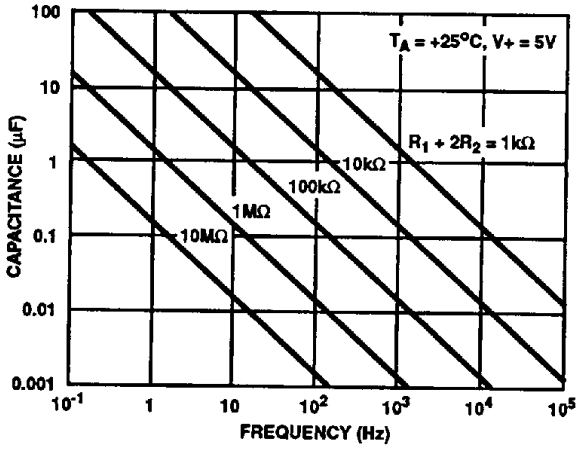


FIGURE 15. FREE RUNNING FREQUENCY OF REPEAT CYCLE TIMER WITH VARIATION IN CAPACITANCE AND RESISTANCE