Semiconductor Inc.
System IC SBU

HB7141D
CMOS IMAGE SENSOR
With 8-bit ADC

DESCRIPTION

HB7141D is a highly integrated single chip CMOS image sensor using Hynix 0.5um CMOS process developed for image application to realize high efficiency photo sensor. The sensor has 812X612 pixels total, and 800X600 pixels effective. Each pixel is high photo sensitive, small size active pixel element that converts photons to analog voltage signal. The sensor has three on-chip 8 bit Digital to Analog Convert (DAC) and 812 comparators to digitize the pixel output. The three on-chip 8 bit DAC can be used for independent gain control. Hynix proprietary on-chip CDS circuit can reduce Fixed Pattern Noise (FPN) dramatically. The whole 8 bit digital color raw data is directly available on the package pins and just few control signals are needed for whole chip control, so it is very ease to configure a system using the sensor.

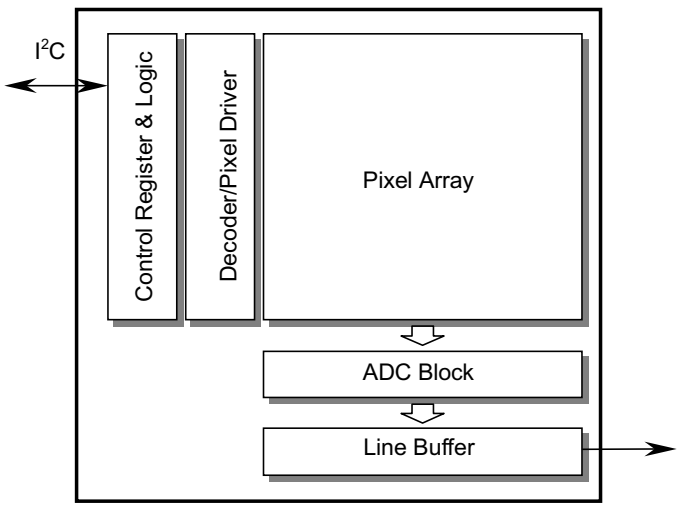
FEATURES

- 800 x 600 pixels resolution
- 8um x 8um square pixels
- High efficiency photo sensors
- Integrated 8-bit ADC for direct digital output
- Low power 3.3V operation (5V tolerant I/O)
- Integrated pan control and window sizing
- Clock speed up to 20MHz
- Programmable frame rate and synchronous format
- Full function control through standard I^2C bus
- Built-in AGC
- 48Pin CLCC
- Anti-blooming circuit
- Flexible exposure time control
- Integrated on-chip timing and drive control
- 1/2" optical format

TECHNICAL SPECIFICATION

Total Pixel Array	812x612
Effective Pixel Array	802x602
Pixel size	8x8um^2
Fill factor	30%
Format	SVGA
Sensitivity	8.0V/lux·sec
Supply voltage for analog	3.3V
Supply voltage for digital	3.3V
Supply voltage for 5V tolerant input	5.0V
Power Consumption	100mW@10MHz
Operating temperature	0~40 Centigrade
Technology	0.5um 2metal CMOS

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

- Supply voltage(Analog, Digital) : 3.0 V ~ 3.6 V
- Voltage on any input pins : 0 V ~ 5.0 V
- Operating Temperature(Centigrade) : 0 ~ 40
- Storage Temperature(Centigrade) : -30 ~ 80

Note : Input pins are 5V tolerant. Stresses exceeding the absolute maximum ratings may induce failure.

DC Operating Conditions

Symbol	Parameter	Units	Min.	Max.	Load[pF]	Notes
V_{dd}	Internal operation supply voltage	Volt	3.0	3.6		
V_{ih}	Input voltage logic "1"	Volt	2.0	5	6.5	
V_{il}	Input voltage logic "0"	Volt	0	0.8	6.5	
V_{oh}	Output voltage logic "1"	Volt	2.15	3.6	60	
V_{ol}	Output voltage logic "0"	Volt	0.4	0.4	60	
T_a	Ambient operating temperature	Celsius	0	40		

AC Operating Conditions

Symbol	Parameter	Max Operation Frequency	Units	Notes
MCLK	Main clock frequency	20	MHz	1
SCK	I^2C clock frequency	400	kHz	2

1. MCLK can be divided according to Clock Divide Register for internal clock.
2. SCK is driven by host processor. For the detail serial bus timing, refer to I^2C Spec.

ELECTRO-OPTICAL CHARACTERISTICS

Color temperature of light source: 3200K / IR cut-off filter (CM-500S, 1mm thickness) is used.

Parameter	Units	Min.	Typical	Max.	Note
Sensitivity	mV / lux·sec	6500	8000	9500	1)
Dark Signal	mV/sec		5	100	2)
Output Saturation Signal	mV	1200	1250		3)
Dynamic Range	dB			48	4)
Output Signal Shading	%		8	13	5)
Dark Signal Shading	mV/sec		3	300	6)
Frame Rate	fps			30	7)

Note:

1) Measured at 8lux illumination for exposure time 10 ms.
2) Measured at zero illumination for exposure time 50 ms. (T_{temp} = 40 Centigrade)
3) Measured at V_{dd} =3.3V and 100lux illumination for exposure time 50msec.
4) 48dB is limited by 8-bit ADC.
5) Variance of average value of 4x4 pixels response of each block over all equal blacks at 50% saturation level illumination for exposure time 10msec.
6) Range between V_{max} and V_{min} at zero illumination for exposure time 50msec, where V_{max} and V_{min} are the maximum and minimum values of each block's response, respectively.
7) Measured at MCLK 15MHz.
   Integration time must be set in order for effective window height not to exceed window height.
   It's because effective window height is directly proportional to integration time.

Soldering

Infrared(IR) / Convection solder reflow condition

Parameter	Units	Min.	Typical	Max.	Note
Peak Temperature Range	Celsius	-	230	240	1)

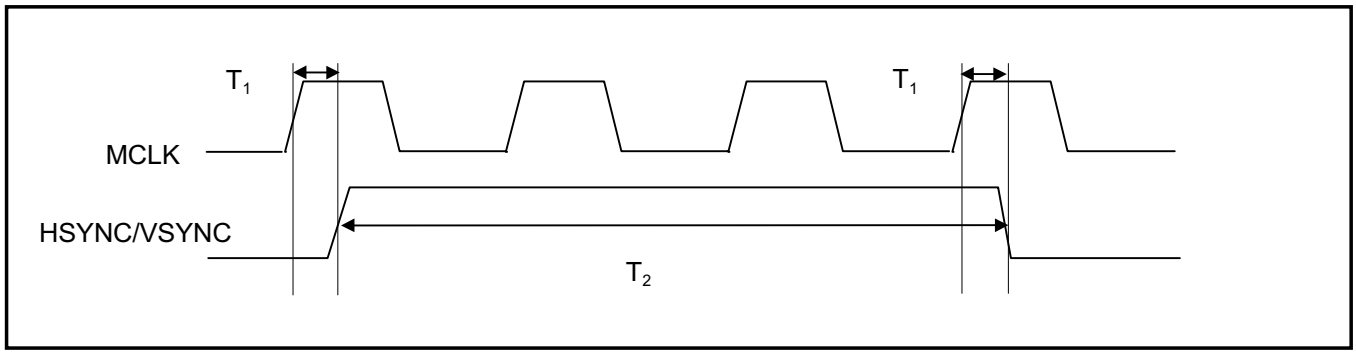
Note:

1) Time within 5 Celsius of actual peak temperature, 10sec

INPUT / OUTPUT AC CHARACTERISTICS

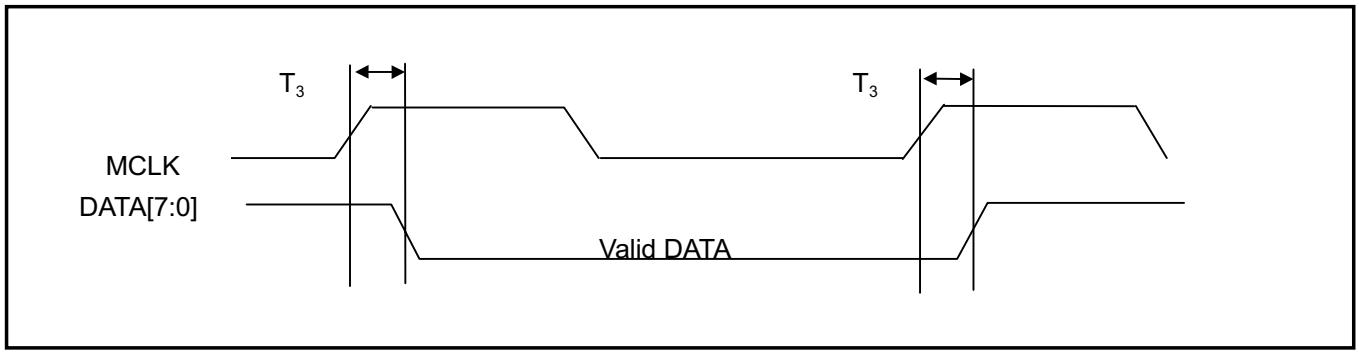
- All output timing delays are measured with output load 60[pF].
- Output delay include the internal clock path delay[6ns] and output driving delay that changes in respect to the output load, the operating environment, and a board design.
- Due to the variable valid time delay of the output, output signals may be latched in the negative edge of MCLK for the stable data transfer between the image sensor and a host for less than 15MHz operation.

MCLK to HSYNC/VSYNC Timing



T_1 : MCLK rising to HSYNC/VSYNC valid maximum time : 18ns [output load: 60pF]
T_2 : HSYNC/VSYNC valid time : minimum 1 Clock(subject to T_1, T_2 timing rule)

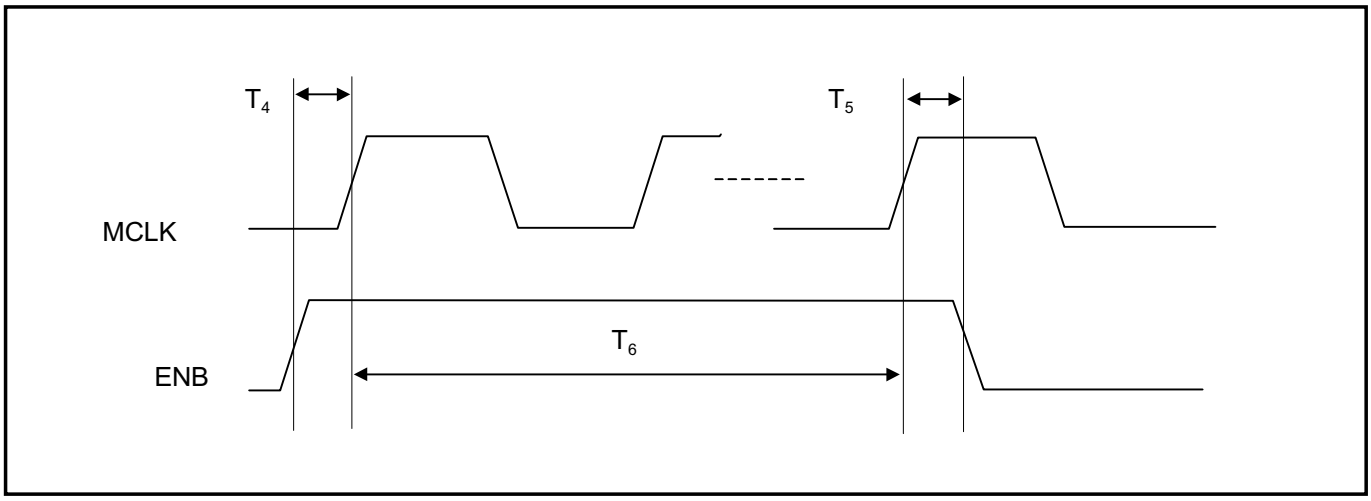
MCLK to DATA Timing



T_3 : MCLK rising to DATA Valid maximum Time : 18ns [output load: 60pF]
Note) HSYNC signal is high when valid data is on the DATA bus.

INPUT / OUTPUT AC CHARACTERISTICS (Continue)

ENB Timing



T_4 : ENB Setup Time : 5ns

T_5 : ENB Hold Time : 5ns

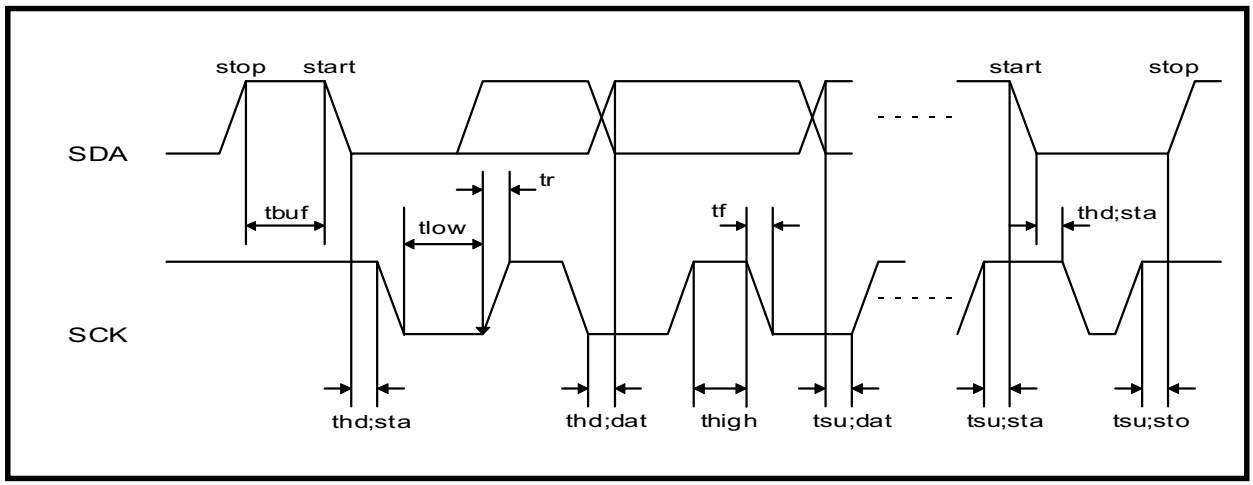
T_6 : ENB Valid Time : minimum 2 Clock

RESET Timing

Must in Valid (active LOW) state at least 8MCLK periods

INPUT / OUTPUT AC CHARACTERISTICS (Continue)

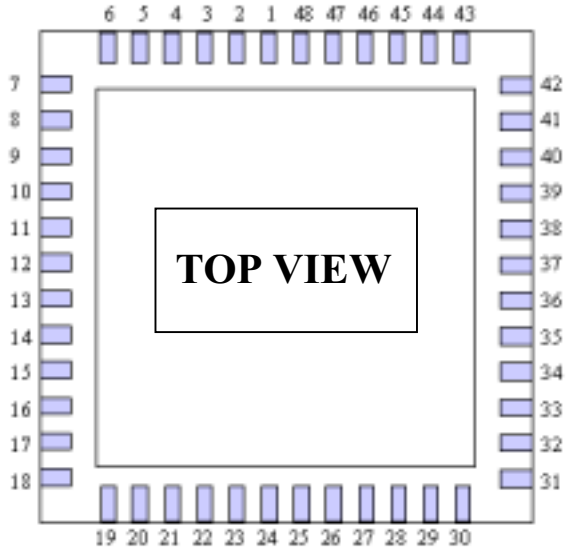
I²C Bus (Programming Serial Bus) Timing



I²C Bus Interface Timing

Parameter	Symbol	Min.	Max.	Unit
SCK clock frequency	f_{sck}	0	400	KHz
Time that IIC bus must be free before a new transmission can start	t_{buf}	1.2		us
Hold time for a START	$t_{hd};s_{ta}$	1.0		us
LOW period of SCK	t_{low}	1.2		us
HIGH period of SCK	t_{high}	1.0		us
Setup time for START	$t_{su};s_{ta}$	1.2		us
Data hold time	$t_{hd};d_{at}$	1.3		us
Data setup time	$t_{su};d_{at}$	250		ns
Rise time of both SDA and SCK	t_r		250	ns
Fall time of both SDA and SCK	t_f		300	ns
Setup time for STOP	$t_{su};s_{to}$	1.2		us
Capacitive load of each bus lines(SDA,SCK)	C_b			pf

PIN CONFIGURATION



PIN NO.	NAME
1	SCK
2	DGND
3	ENB
4	DGND
5	MCLK
6	VDD5
7	AVDD
8	AGND
17	AGND
18	AVDD
21	DGND
22	DATA7
23	DATA6
24	DATA5
25	DATA4

PIN NO.	NAME
26	DGND
27	DATA3
28	DATA2
29	DATA1
30	DATA0
31	DVDD
32	DGND
42	DVDD
43	RESET
44	VSYNC
45	HSYNC
46	DGND
47	SDA
48	DGND

Pin9~16, Pin19~20, Pin33~41 : No Connection

PIN DESCRIPTION

PIN	NAME	I/O	DESCRIPTION
1	SCK	I	I^2C Clock ; I^2C clock control from I^2C master
2	DGND	I	Digital Ground
3	ENB	I	Sensor Enable Signal ; 'H' enable normal operation 'L' disable sensor
4	DGND	I	Digital Ground
5	MCLK	I	Master Clock (up to 20MHz) ; Global master clock for image sensor internal timing control
6	VDD5	I	I/O bias voltage for 5V tolerant *1)
7	AVDD	I	Analog Supply Voltage 3.3V
8	AGND	I	Analog Ground
9 ~ 16	N.C		No Connection
17	AGND	I	Analog Ground
18	AVDD	I	Analog Supply Voltage 3.3V
19, 20	Reserved		Reserved
21	DGND	I	Digital Ground
22	DATA7	O	Image Data bit 7
23	DATA6	O	Image Data bit 6
24	DATA5	O	Image Data bit 5
25	DATA4	O	Image Data bit 4
26	DGND	I	Digital Ground
27	DATA3	O	Image Data bit 3
28	DATA2	O	Image Data bit 2
29	DATA1	O	Image Data bit 1
30	DATA0	O	Image Data bit 0
31	DVDD	I	Digital Supply Voltage 3.3V
32	DGND	I	Digital Ground
33 ~ 41	N.C		No Connection
42	DVDD	I	Digital Supply Voltage 3.3V
43	RESET	I	Hardware Reset Signal, Active Low
44	VSYNC	O	Vertical synchronization signal / Frame start output ; Signal pulse at start of image data frame with programmable blanking duration
45	HSYNC /DVALID	O	Horizontal synchronization signal / Data valid output ; Data valid when 'H' with programmable blanking duration
46	DGND	I	Digital Ground
47	SDA	I/O	I^2C Data ; I^2C standard data I/O port
48	DGND	I	Digital Ground

*1) Tie to DVDD for 3.3V operation / Tie to 5V for 5V tolerant operation

REGISTER DESCRIPTION

MODE_B

This is operating mode select register. Each bit's description is as below.

Bit	Function	Description
0	Integration time unit	Integration time is controlled by register 25H, 26H Integration time register value's unit will be changed by this bit setting, as line or pixel unit. Line mode is general, but under high light intensity Condition, or need of precise integration time control, pixel mode is used. Default is line mode.
1	Shot mode	Continuous frame mode : The sensor outputs the sensing data Consecutively. That is, sensor updates frame buffer data continuously after Reading out. Single shot frame mode : Sensor stops updating frame buffer after only one frame data storing to catch just one picture frame. Default is continuous mode.
3	HSYNC pin configuration	HSYNC only mode: HSYNC pin outputs the HSYNC signal only. HSYNC & internal clock mode : HSYNC pin outputs 'Anding' signal of HSYNC signal and internal pixel clock. Use this mode to get pixel data and pixel clock both from the sensor Default is HSYNC only mode
5,4	Output data type	Three output data types : data - reference, data only and reference only For CDS(correlated double sampling), the sensor measured the reference and data respectively. To get rid of circuit noise, the sensor execute CDS. Default is data - reference (CDS).

MODE_C

This is operating mode select register. Each bit's description is as below

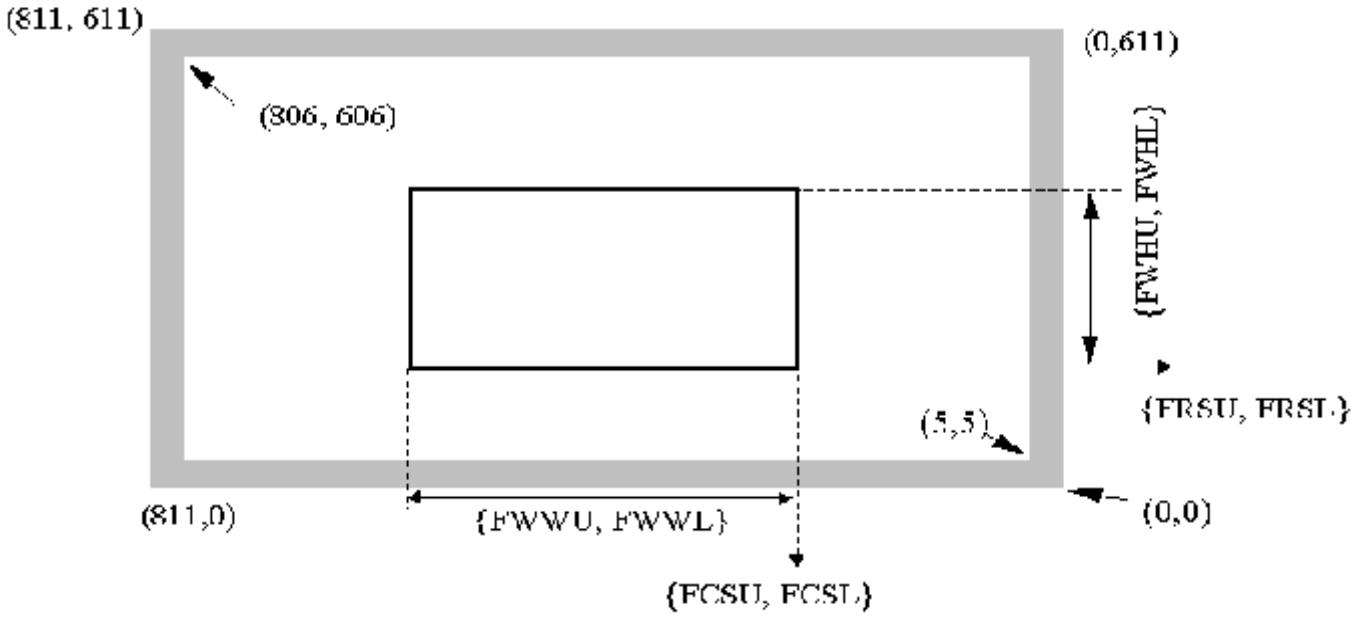
Bit	Function	Description
1	Display Mode	Color Mode : Color Output Black & White Mode : Black & White Output ; In this mode pixel output is controlled by 'G' gain only.
2	Power Down Mode	Enable Analog Block Power Down Disable Analog Block Power Down

REGISTER DESCRIPTION (continue)

FRAME REGISTER

The HB7141D can read any user specific window area within total effective window.

This is called panning function. For this function, 'row start', 'column start', 'width', 'height' can be programmed with four 4 registers, FRS(Frame Row Start), FCS(Frame Column Start), FWH(Frame Window Height), FWW(Frame Window Width). Panning window can be programmed as below.



Note1) Accessible pixel array size is 812X612

The edge of accessible pixel array may be commonly dedicated for just color interpolation.

In the case of a color image sensor the interpolation is needed to get all R,G,B color value for each pixel of a color image.

So, one more extra pixel line is needed at the edge of pixel array than what want to display.

That is, to make 800X600 effective window, 802X602 pixel array is necessary. You have to consider this interpolation line when you program the 'Frame register'. For example, If you want to get 300X250 image size, you have to program 302X252 to frame register.

Note2) You have to change the frame register value as below to get the full 800X600 window size.

FRSU, FRSL	5	FWHU, FWHL	602
FCSU, FCSL	5	FWWU, FWWL	802

CONTROL REGISTER DESCRIPTION (continue)

CONTROL REGISTER Control registers is divided into timing related register and adjust register.

TIMING RELATED REGISTER

- **HSYNC blank register**

The HSYNC blank register defines the active period of HSYNC output and the programming unit is pixel clock.

This low active signal defines boundary of each line. The pixel data output is valid while HSYNC is high. The value programmed to HSYNC blank register defines HSYNC low period under the 'full window size mode operation.(refer to timing diagram).

If the display window width is decreased by frame register's programming, the actual HSYNC blank register is increased as much as decreasing of window width automatically. (refer to timing diagram)

- **VSYNC blank register**

The VSYNC blank register defines the active period of VSYNC output and the programming unit is line. This high active signal defines boundary of each frame. Same as HSYNC, VSYNC register value also has a meaning under the full window size mode. That is, VSYNC blank register value means VSYNC high period under the full window size mode. According to variation of display window height by programming of frame register, VSYNC high active duration is also increased.

- **Integration time value register**

Integration time value register defines integration time.

This is same as exposure time in a camera. So, at dark condition, long integration time is necessary.

The unit is changed by value of MODE_B register's bit 0 as pixel or line.

- **Master clock divider register**

This four bits register is used to divide external pixel clock frequency for internal use. The actual pixel operating frequency used in the sensor is same as external pixel frequency divided by divisor as below.

Register value	Divisor	Register value	Divisor	Register value	Divisor
0	1	4	16	8	256
1	2	5	32	9	512
2	4	6	64	10	1024
3	8	7	128	11	2048

REGISTER DESCRIPTION (continue)

ADJUST REGISTER

Each chip has a little different photo-diode characteristics. So, some calibration of sensing circuit is needed to get the optimal performance. The adjust register is designed for this calibration purpose. There are three kinds of registers as below.

- **Reset level register**

The register controls the voltage level that is initially compared to pixel analog voltage, and the initial voltage level is called as “reference voltage level”. Internal DAC analog voltage decrements from reference voltage level until the pixel analog voltage output is lager than DAC analog voltage. Appropriate reference voltage level varies from various factors, such as process variation, luminance, etc. If the register value is set to too large or too small value, vertical fixed pattern noise may be produced. Therefore this register value must be programmed to appropriate value in order to avoid FPN. For the automatic reset level control, please refer to Reset Level Statistics Register Section. High register value means high reference voltage and large digital output. Program value range is 0~63, User should refer to the "RESET LEVEL CONTROL" application notes for proper using this register.

- **Gain register**

There are three gain registers - R, G and B gain register, respectively. The G gain register of them is only used to amplify digital pixel output in the B/W mode. If the gain register value is decreased, digital pixel output is increased. That is, under dark light condition the pixel output is not enough to get right image so that we must amplify the output value by decreasing gain value to get good image. Program value range is 0~63. However, we recommend that the range should be 30~60 for capturing image quality.

- **Pixel bias voltage register**

This register controls pixel reference level by controlling bias current of pixel output sensing load Transistor.

It controls pixel output level itself, compare with that reset level register adjust ADC circuit to calibrate reference level for data reading. Available program range is 0~7. The larger register value causes the higher bias current to decrease pixel output reference level.

REGISTER DESCRIPTION (continue)

RESET LEVEL STATISTICS REGISTER

- **Low Reset Level Count[<5]**

  This two-byte register has a value representing a eighth (1/8) of pixels that have reset value less than 5 during one frame time and is updated when VSYNC gets active.

  With high reset level counter register it can be used as a parameter for external automatic reset level control logic that update the appropriate value in the reset level register to automatically compensate die to die overall reset level variation.

- **High Reset Level Count[＞147]**

  This two byte register has a value representing a eighth (1/8) of pixels that have reset value larger than 147 during one frame time and is updated when VSYNC gets active.

  With low reset level counter register it can be used as a parameter for external automatic reset level control logic that update the appropriate value in the reset level (30H) register to automatically compensate die to die overall reset level variation.

REGISTER ADDRESS AND DEFAULT VALUE

<table>
<tr><th>Group</th><th>Symbol</th><th>Address</th><th>Description</th></tr>
<tr><td rowspan="2">Mode-Registers</td><td>MODE_A</td><td>00H</td><td>Reserved</td></tr>
<tr><td>MODE_B</td><td>01H</td><td>Operating Mode Selection (Default : 04H)

<table>
<tr><td>b0</td><td>0</td><td>Line Unit Integration</td></tr>
<tr><td></td><td>1</td><td>Pixel Unit Integration</td></tr>
</table>
<table>
<tr><td>b1</td><td>0</td><td>Continuous Frame</td></tr>
<tr><td></td><td>1</td><td>Single Shot Frame</td></tr>
</table>
<table>
<tr><td>b2</td><td>0</td><td>Reserved</td></tr>
<tr><td></td><td>1</td><td>Windowed Image</td></tr>
</table>
<table>
<tr><td>b3</td><td>0</td><td>HSYNC only</td></tr>
<tr><td></td><td>1</td><td>HSYNC & Internal Clock</td></tr>
</table>
<table>
<tr><td>b5</td><td>b4</td><td>Output Data Type</td></tr>
<tr><td>0</td><td>0</td><td>Data_Level - Reference_Level</td></tr>
<tr><td>0</td><td>1</td><td>Reference_Level</td></tr>
<tr><td>1</td><td>0</td><td>Data_Level</td></tr>
<tr><td>1</td><td>1</td><td>reserved</td></tr>
</table>
<table>
<tr><td>b7</td><td>b6</td><td>Operating Mode</td></tr>
<tr><td>0</td><td>0</td><td>Normal Mode</td></tr>
<tr><td>0</td><td>1</td><td>Reserved</td></tr>
<tr><td>1</td><td>0</td><td>Reserved</td></tr>
<tr><td>1</td><td>1</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>MODE_C</td><td>02H</td><td>
<table>
<tr><td>b0</td><td>0</td><td>8 bit mode</td></tr>
<tr><td></td><td>1</td><td>Reserved</td></tr>
</table>Default :00H

<table>
<tr><td>b1</td><td>0</td><td>Color Output</td></tr>
<tr><td></td><td>1</td><td>Black & White Output</td></tr>
</table>
<table>
<tr><td>b2</td><td>0</td><td>Disable Analog Power Down</td></tr>
<tr><td></td><td>1</td><td>Enable Analog Power Down</td></tr>
</table></td></tr>
</table>

REGISTER ADDRESS AND DEFAULT VALUE (continue)

Group	Symbol	Address	Description	Default	
Frame-Registers	FRSU	10H	Row Start Address (Upper byte)	00H	[5]
	FRSL	11H	Row Start Address (Lower byte)	05H	
	FCSU	12H	Column start Address (Upper byte)	00H	[5]
	FCSL	13H	Column start Address (Lower byte)	05H	
	FWHU	14H	Window Height (Upper byte)	02H	[602]
	FWHL	15H	Window Height (Lower byte)	5aH	
	FWWU	16H	Window Width (Upper byte)	03H	[802]
	FWWL	17H	Window Width (Lower byte)	22H	
Timing-Register	THBU	20H	HSYNC Blanking Duration value (Upper byte)	Default :00H	
	THBL	21H	HSYNC Blanking Duration value (Lower byte)	03H	
	TVBU	22H	VSYNC Blanking Duration value (Upper byte)	00H	
	TVBL	23H	VSYNC Blanking Duration value (Lower byte)	03H	
	TITU	25H	Integration Time value (Upper byte)	00H	
	TITM	26H	Integration Time value (Middle byte)	01H	
	TITL	27H	Integration Time value (Lower byte)	F4H	
	TMCD	28H	Master Clock Divider	00H	
Adjust-Register	ARLV	30H	Reset Level Value	28H	
	ARCG	31H	Red Color Gain	28H	
	AGCG	32H	Green Color Gain	28H	
	ABCG	33H	Blue Color Gain	28H	
	APBV	34H	Pixel Bias Voltage Control	02H	
Offset Register	OFSR	50H	R Offset Register (Test purpose Only)	00H	
	OFSG	51H	G offset Register (Test purpose Only)	00H	
	OFSB	52H	B offset Register (Test purpose Only)	00H	
Reset Level Statistics Register	LoREfNOH	57H	Low Reset Level Counter [<3] (Upper byte)	(Read Only)	
	LoREfNOL	58H	Low Reset Level Counter [<3] (Lower byte)	(Read Only)	
	HiRefNOH	59H	High Reset Level Counter [>147] (Upper byte)	(Read Only)	
	HiRefNOL	5AH	High Reset Level Counter [>147] (Lower byte)	(Read Only)	

PROGRAMMING SEQUENCE FOR CMOS IMAGE SENSOR

- **Single Register Byte Programming**

S	22H	A	01H	A	mode inform	A	P
*1	*2	*3	*4	*5	*6	*7	*8

⇨ Set "Operating Mode" register into Window mode

*1. Drive: I^2C start condition
*2. Drive: 22H(001_0001 + 0) [device address + R/W bit]
*3. Read: acknowledge from sensor
*4. Drive: 01H [sub-address]
*5. Read: acknowledge from sensor
*6. Drive: 04H [mode information]
*7. Read: acknowledge from sensor
*8. Drive: I^2C stop condition

- **Multiple Register Byte Programming using Auto increment Mode**

S	22H	A	01H	A	02H	A	65H	A	P
*1	*2	*3	*4	*5	*6	*7	*8	*9	*10

⇨ You can program multiple configuration registers with single I^2C bus cycle.

⇨ Set "Row Start Address" register as 265H

*1. Drive: I^2C start condition
*2. Drive: 22H(001_0001 + 0) [device address + R/W bit]
*3. Read: acknowledge from sensor
*4. Drive: 01H [sub-address]
*5. Read: acknowledge from sensor
*6. Drive: 02H [row start address upper byte]
*7. Read: acknowledge from sensor
*8. Drive: 65H [row start address lower byte]
*9. Read: acknowledge from sensor
*10. Drive : I^2C stop condition

PROGRAMMING SEQUENCE FOR CMOS IMAGE SENSOR (continue)

- **Reading Register Value**

S	22H	A	01H	A	S	23H	A	Read Data	A	P
*1	*2	*3	*4	*5	*6	*7	*8	*9	*10	

⇨ Single Read or Auto-Increment Read

⇨ Set "Reset Level Value" register

*1. Drive: I^2C start condition

*2. Drive: 22H(001_0001 + 0) [device address + R/W bit(be careful. R/W=0)]

*3. Read: acknowledge from sensor

*4. Drive: 01H [sub-address]

*5. Read: acknowledge from sensor

*6. Drive: I^2C start condition

*7. Drive: 23H(001_0001 + 1) [device address + R/W bit(be careful. R/W=1)]

*8. Read: acknowledge from sensor

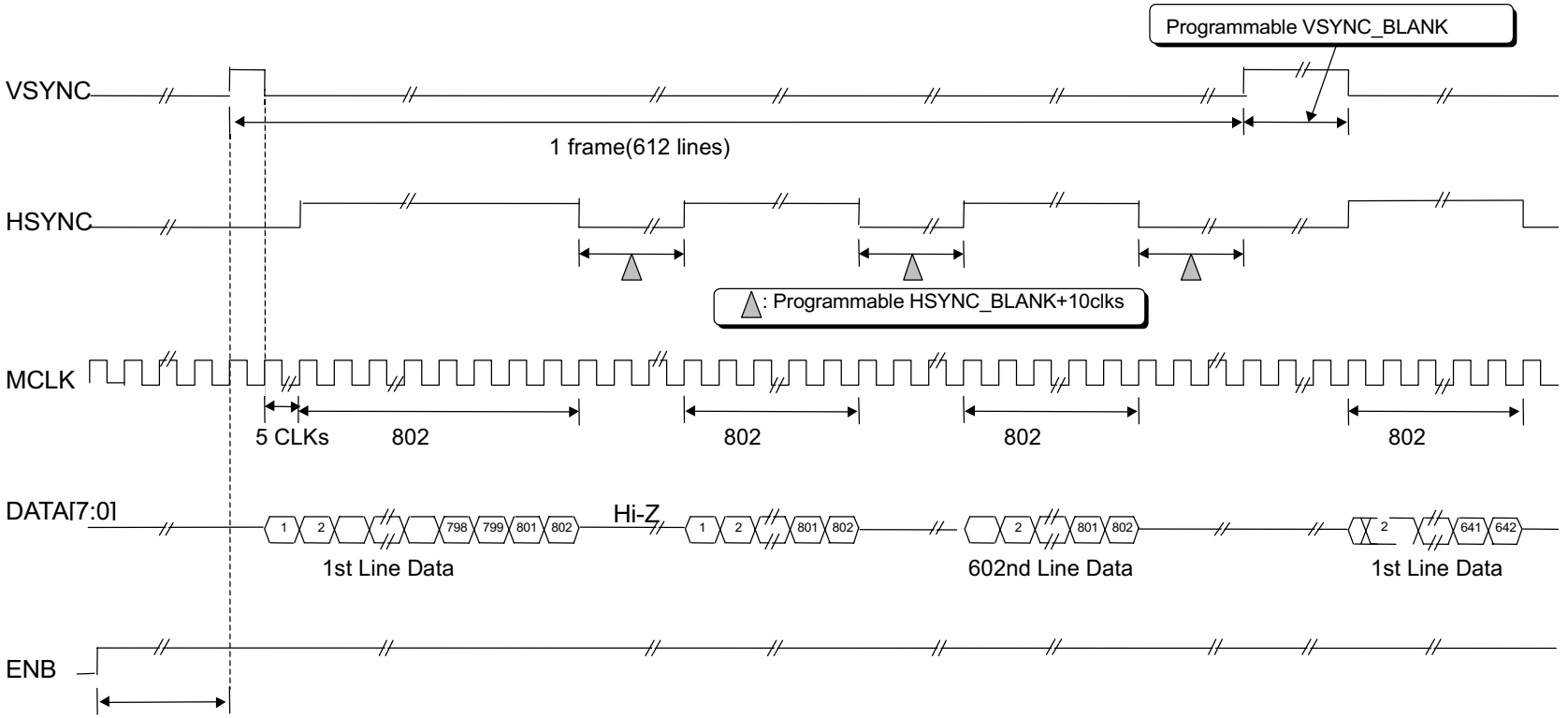
*9. Read: Read Data from sensor

*10. Drive: acknowledge to sensor(if there is no more read data Ack=1, else Ack=0)

*11. Drive : I^2C stop condition

TIMING DIAGRAM

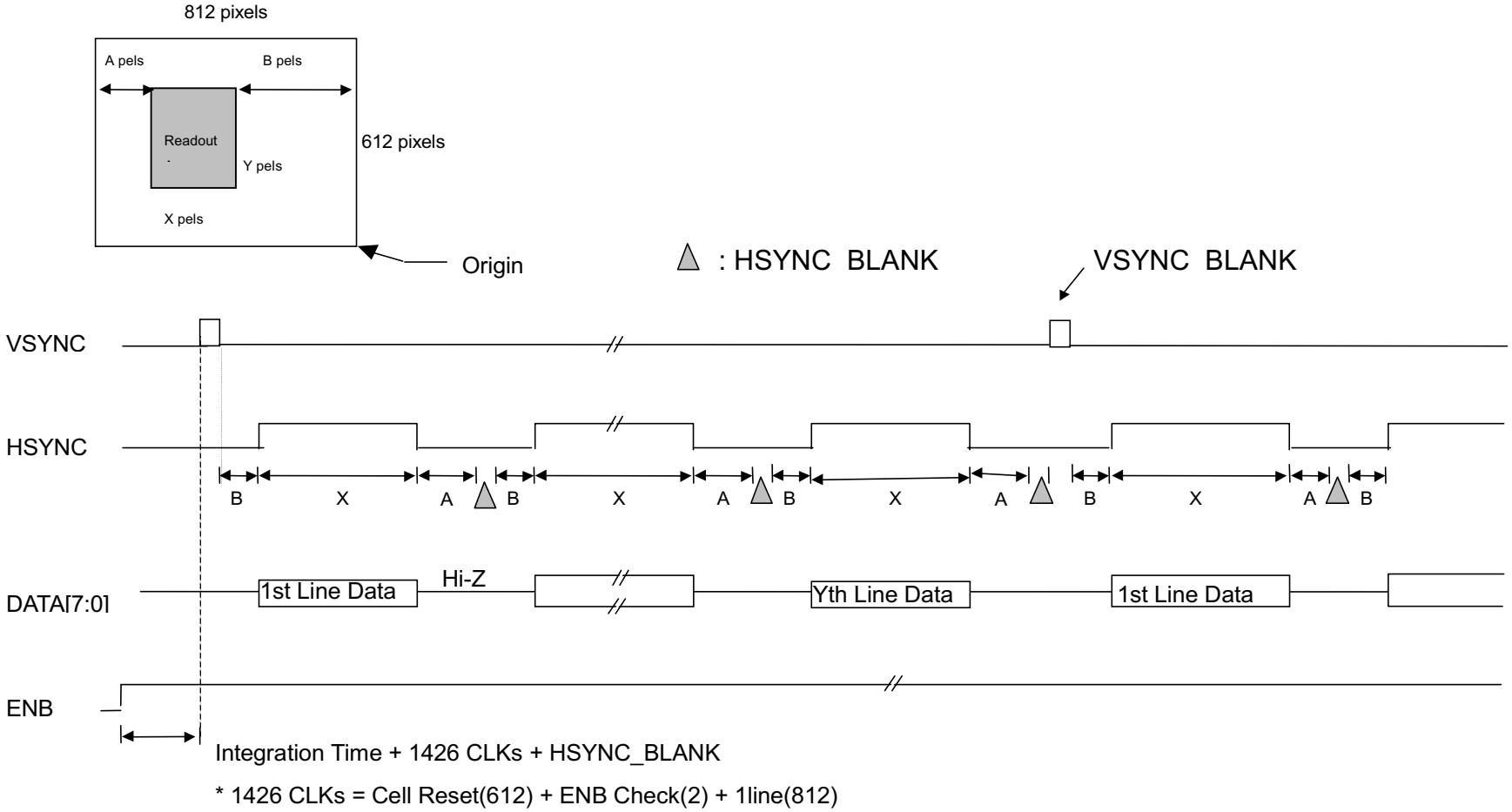
1. Synchronous Readout Mode @ Full sized image (802x602)



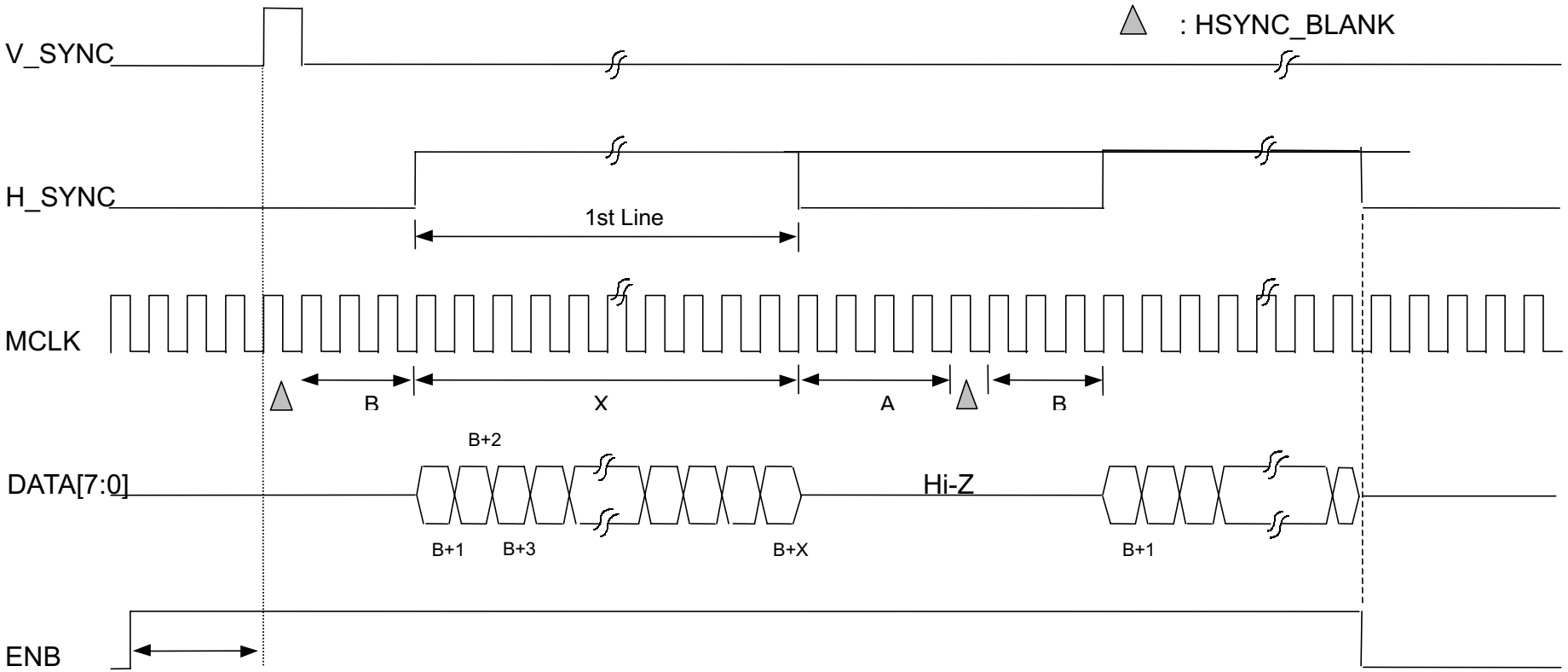
Integration Time + 1426 CLKs + HSYNC_BLANK

* 1426 CLKs = Cell Reset(612) + ENB Check(2) + 1line(812)

2. Synchronous Readout Mode @ Windowed image (X * Y pixels)



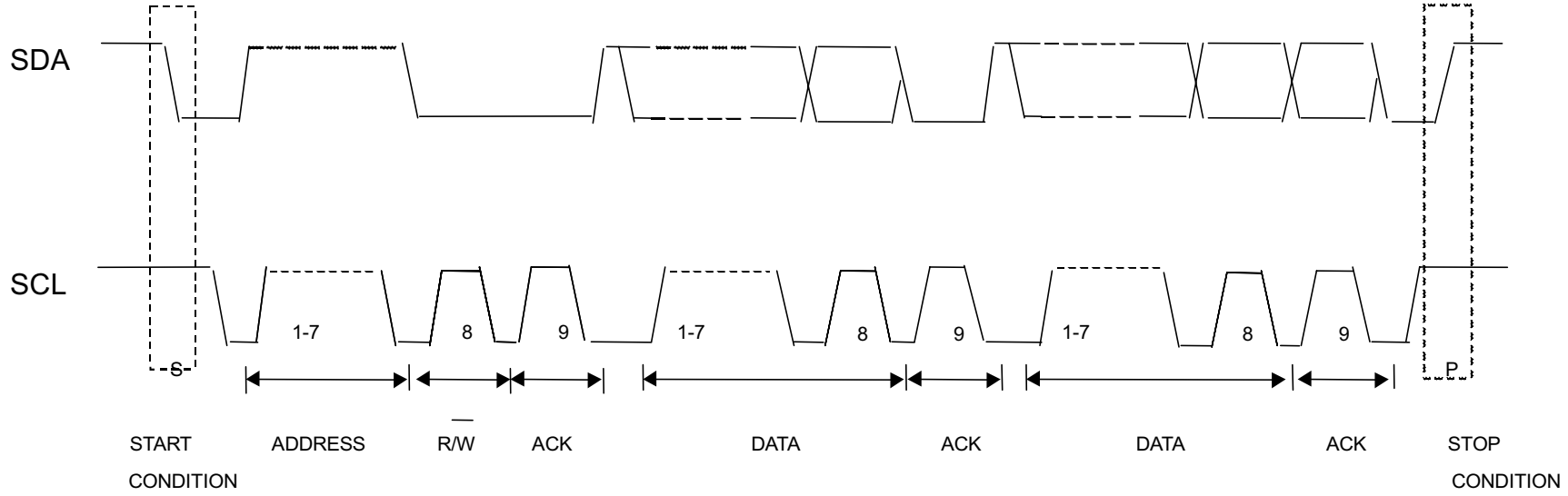
2. Synchronous Readout Mode @ Windowed image (X * Y pixels) – Continued



Integration Time + 1426 CLKs + HSYNC_BLANK

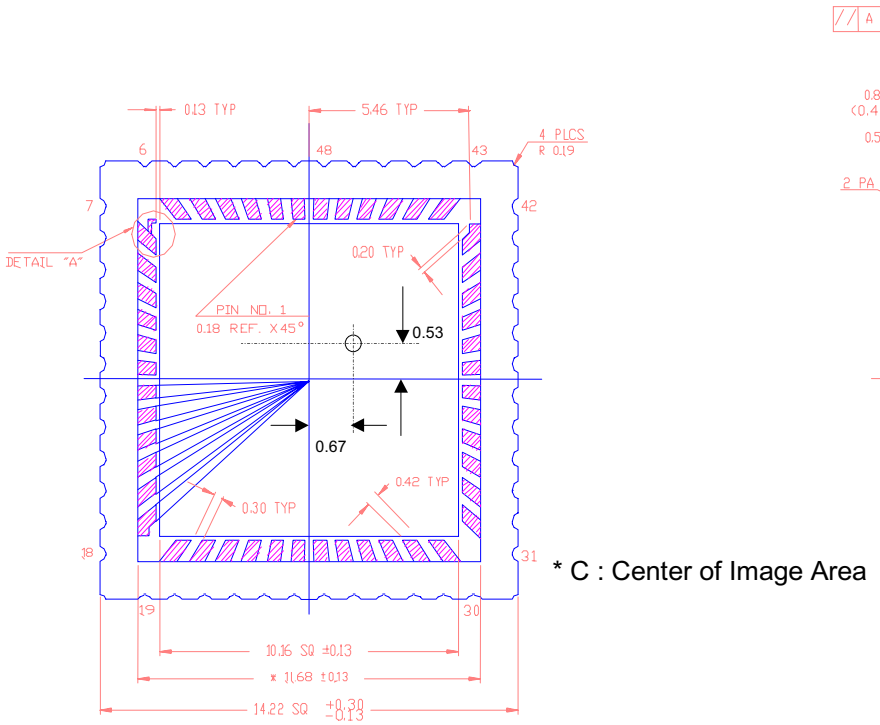
* 1426 CLKs =Cell Reset(612) + ENB Check(2) + 1line(812)

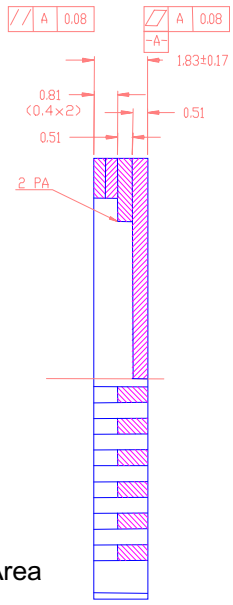
3. I²C Control Mode

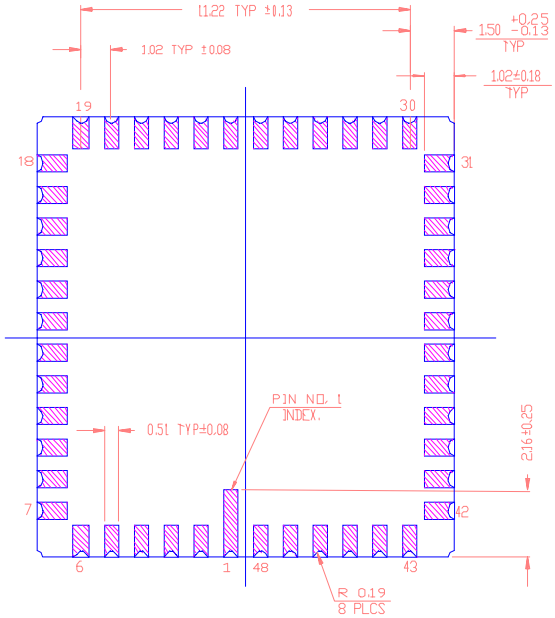


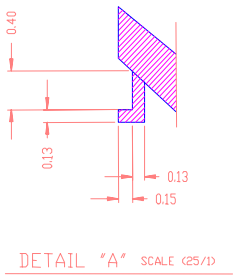
PACKAGE DISMENSION (48 PIN PLCC/CLCC)

UNIT: mm









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