GDC21D301A
(Transport Decoder)

Version 1.5

HDS-GDC21D301A-9908 / 10

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1. General Description

The GDC21D301A Transport Decoder resides in the center of an MPEG-2 decoding system. It accepts MPEG-2 transport streams, parses the transport and packetized elementary stream (PES) layers into the separate data streams, and provides rate buffering for the parsed data streams. Then it passes those data streams to video and audio decoders. The GDC21D301A also extracts Program Clock Reference (PCR) in the data stream and provides the Pulse Width Modulation (PWM) signals in order to recover the clock and to synchronize the playback of video and audio. The GDC21D301A manages an external DRAM that is used for data storage and buffering the various parsed data streams. This DRAM is shared with the host processor so that the system's memory requirements can be consolidated into a single, low-cost DRAM. The GDC21D301A stores data packets destined for the host directly in shared DRAM for easy access by the host.

2. Features

The GDC21D301A is fully compliant with MPEG-2 ISO/IEC 13818-1 specification.

Decoding Features

- Performs MPEG-2 transportation and PES layer handling
- Supports maximum 80 Mbps transport streams
- Provides a high-speed data output port
- Identifies and extracts up to 32 transport stream (TS) packet PIDs

PCR & Time Stamp Control Features

- Provides two PWM signals to recover the system clock
- Provides the instant value of internal STC counter when a frame begins
- Extracts PTS and DTS of video and audio for Lip-synchronization

Interface

- Supports byte-parallel/bit-serial TS input
- Supports video/audio PES layer or elementary stream layer output
- Provides error code insertion capability in video elementary stream
- Supports an external error input signal for declaring an erroneous packet
- Supports 8/16-bit host bus interface

3. Pin Description

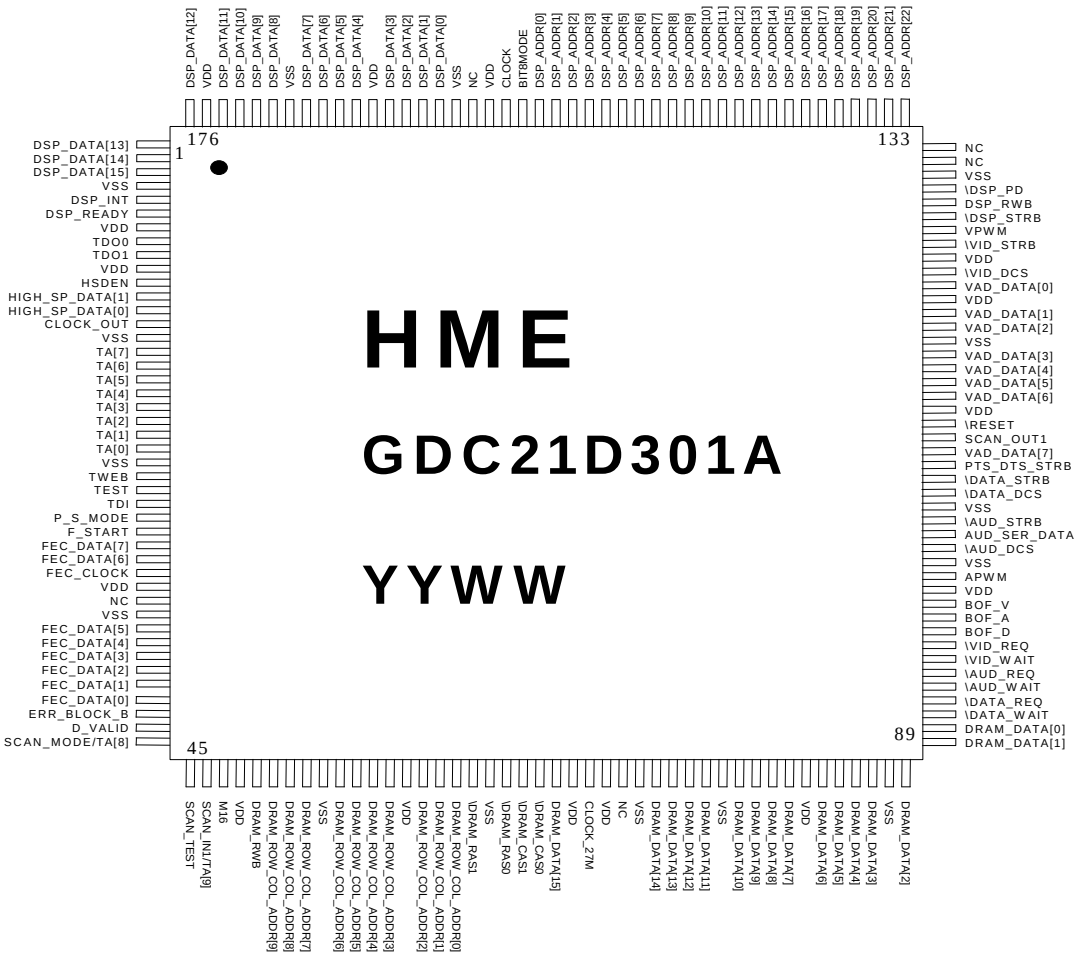


Figure 1. Pin Description

(Package : 176TQFP)

NAME	PIN	TYPE	DESCRIPTION
CLOCKS & RESET			
CLOCK	157	I	**Operation clock.** The frequency of operating clock is 27MHz and it should be locked in encoder system clock. The clock may be supplied by external VCXO controlled by VPWM.
CLOCK_27M	69	I	**27MHz clock.** It is used to count STC value. This clock may be supplied by external VCXO controlled by VPWM.
CLOCK_OUT	14	O	**Operation Clock Output.** For high-speed output data
\RESET	112	I	**Global Reset (active low)** The signal asynchronously resets the GDC21D301A.
TEST INTERFACE (for IC self-test purpose only)			
TEST	26	I	**Test Mode**
TA[9:0]	46,44,16,17, 18,19,20,21,2 2,23	I	**Test address.** TA[9] and TA[8] are respectively multiplexed with SCAN_IN1 and SCAN_MODE pins.
TDI	27	I	**Test Input Data**
TWEB	25	I	**Test Write Enable (active low)**
TDO0	8	O	**Test Output Data0**
TDO1	9	O	**Test Output Data1**
TRANSPORT STREAM INTERFACE			
P_S_MODE	28	I	**FEC Data Input Mode Selection.** 0: byte-parallel input mode 1: bit-serial input mode
FEC_DATA[7:0]	30,31,36,37, 38,39,40,41	I	**TS Data.** It is used for byte-parallel or bit-serial transfers of a coded TS data to the device. In bit-serial mode, FEC_DATA[0] is a serial data input for TS data.
F_START	29	I	**FEC Sync Byte Indicator.** F_START is valid in bit-serial input mode only. FEC_DATA is aligned by the byte parallel with this signal. This signal should be activated at the first bit of the TS sync byte or every first bit of the data byte.
FEC_CLOCK	32	I	**FEC Data Clock.** FEC_CLOCK is used to latch a data byte or a single bit of coded TS into the device on the rising edge. FEC_CLOCK may be asynchronous with the device. The value of FEC_DATA is locked into the GDC21D301A internal buffer on the rising edge of FEC_CLOCK, if D_VALID is asserted HIGH.

Pin Description *(continued)*

NAME	PIN	TYPE	DESCRIPTION
HIGH SPEED DATA INTERFACE			
\ERR_BLOCK	42	I	**FEC Packet Error (active low).** This optional signal may be used to declare that the error has occurred in a packet. It is used in place of transport_error_indicator bit in the TS header by the equipment interfacing with the GDC21D301A.
D_VALID	43	I	**FEC Data Valid.** This signal indicates that the data value of FEC_DATA bus is valid transport stream byte or serial bit. It will be latched in the internal buffer on the rising edge of FEC_CLOCK.
HSDEN	11	O	**High Speed Port Data Enable**
HIGH_SP_DATA [1:0]	12, 13	O	**High Speed Port Data**
CLOCK RECOVERY INTERFACE			
VPWM	126	O	**Pulse Width Modulated Pulse1.** Low pass filtered VPWM signal is fed to external VCXO for adjusting its output frequency.
APWM	101	O	**Pulse Width Modulated Pulse2.** This is used to lock the Audio clock in the Video clock for lip synchronization. Low pass filtered APWM signal is fed to the VCXO.
DRAM INTERFACE			
M16	47	I	**DRAM 16-Mbit Configuration**
DRAM_RWB	49	O	**DRAM Read/Write.** When you access DRAM, read mode or write mode can be set as following. 0 : Write mode 1 : Read mode
DRAM_ROW_COL_ ADDR[9:0]	50,51,52,54, 55,56,57,59, 60,61	O	**DRAM Parallel Address Bus [9:0].** Row-column address is multiplexed when you access external DRAM. For the fast page mode access, row address is applied first, and column address is applied next.
DRAM_DATA[15:0]	67,73,74,75, 76,78,79,80, 81,83,84,85, 86,88,89,90	I/O/Z	**DRAM Parallel Data Bus [15:0].**
\DRAM_RAS0	64	O	**DRAM Row Address Strobe0.** Select DRAM0 device. When this signal goes to low, DRAM_ ROW_COL_-ADDR[9:0] has a valid row address.
\DRAM_RAS1	62	O	**DRAM Row Address Strobe1.** Select the DRAM1 device. When this signal goes to low, DRAM_ROW_COL_-ADDR[9:0] has a valid row address.
\DRAM_CAS0	66	O	**DRAM Column Address Strobe0.** Select the low byte DRAM data. When this signal goes to low, DRAM_-ROW_COL_ADDR[9:0] has a valid column address.
\DRAM_CAS1	65	O	**DRAM Column Address Strobe1.** Select the high byte DRAM data. When this signal goes to low, DRAM_-ROW_COL_ADDR[9:0] has a valid column address.

Pin Description *(continued)*

NAME	PIN	TYPE	DESCRIPTION
HOST PROCESSOR INTERFACE			
\DSP_STRB	127	I	**Host Strobe (active low) : Asynchronous.** Used by the host processor to access the GDC21D301A. When DSP_STRB signal is active, DSP_ADDR[22:0], DSP_DATA[15:0], and DSP_PD should be valid.
DSP_RWB	128	I	**Read/Write (active low) : Asynchronous.** The state of this signal defines data transfer type. 0 : Write to the device 1: Read from the device
\DSP_PD	129	I	**Transport Decoder Chip Selection (active low).** This signal is used to activate and access the internal registers of the GDC21D301A, the video decoder, the audio decoder, the data decoder, and DRAM.
DSP_ADDR[22:0]	133,134,135, 136,137,138, 139,140,141, 142,143,144, 145,146,147, 148,149,150, 151,152,153, 154,155	I	**Host Address Bus.** These signals are connected to the address bus of the host processor interfaced with the GDC21D301A, the video decoder, the audio decoder, the data decoder, and DRAM. 0x4FFFFF ~ 0x4C0000 : Transport Decoder address space 0x5BFFFF ~ 0x480000 : Video decoder space 0x47FFFF ~ 0x440000 : Audio decoder space 0x43FFFF ~ 0x400000 : Auxiliary data decoder space 0x3FFFFF ~ 0x000000 : DRAM space
BIT8MODE	156	I	**Host Interface Mode Selection.** 0 : 16-bit data bus interface 1 : 8-bit data bus interface
DSP_DATA[15:0]	3, 2, 1, 176, 174,173,172, 171,169,168, 167,166,164, 163,162,161	I/O/Z	**Host Data Bus.** These signals are connected to the address bus of external host processor.
DSP_READY	6	O/Z	**Data Acknowledge (active high)**
DSP_INT	5	O	**Interrupt Request (active high)**

Pin Description *(continued)*

NAME	PIN	TYPE	DESCRIPTION
VIDEO DECODER INTERFACE			
\VID_WAIT	95	I	**Video Wait (active low).** This signal indicates that the access of registers in the video decoder is ready.
\VID_REQ	96	I	**Video Compressed Data Request (active low).** A video decoder requests video data from the GDC21D301A by using this signal.
\VID_STRB	125	O	**Video Compressed Data Strobe (active low).** The signal indicates that the video data in VAD_DATA[7:0] exists. The video decoder should latch the video data on the rising edge of VID_STRB.
\VID_DCS	123	O	**Video Chip Select (active low).** This signal activates data transfers between the video decoder and the host processor. Host processor can access the registers of the video decoder.
VAD_DATA[7:0]	110,114,115, 116,117,119, 120,122	I/O/Z	**Video/Audio Decoder Data.** Parallel bit stream output of compressed audio, video, and auxiliary data.
PTS_DTS_STRB	109	O	**Video PTS/DTS Strobe (active high).** When this signal is asserted High, the GDC21D301A puts PTS (Presentation_Time_Stamp) or DTS (Decoding_Time_Stamp) into VAD_DATA[7:0] bus.
BOF_V	99	I	**Begin of Frame0.** On the rising edge of this signal, STC, the counted PCR value, is copied to STC3_reg.
AUDIO DECODER INTERFACE			
\AUD_WAIT	95	I	**Audio Wait (active low).** This signal indicates that the access of registers in the audio decoder is ready.
\AUD_REQ	94	I	**Audio Data Request (active low).** An audio decoder requests audio data from the GDC21D301A by using this signal.
AUD_SER_DATA	104	O	**Audio Serial Data.**
\AUD_STRB	105	O	**Audio Data Strobe (active low).** This signal indicates that audio data on VAD_DATA[7:0] exists. \AUD_STRB signal can be used as the data clock for serial and parallel data transmission. Thus, if output mode is parallel, \AUD_STRB is 1-byte strobe. And if output mode is serial, \AUD_STRB is 1-bit strobe.
\AUD_DCS	103	O	**Audio Select (active low).** This signal activates data transfers between the audio decoder and the host processor. Host processor should communicate data with the audio decoder through the GDC21D301A.
BOF_A	98	I	**Begin of Frame1.** On the rising edge of this signal, STC, the counted PCR_value, is copied to STC3_reg.

Pin Description *(continued)*

NAME	PIN	TYPE	DESCRIPTION
AUXILIARY DATA DECODER INTERFACE			
\DATA_WAIT	91	I	**Auxiliary Data Wait (active low).** This signal indicates that the access of registers in the auxiliary decoder is ready.
\DATA_REQ	92	I	**Auxiliary Data Request (active low).** This signal is asserted when an auxiliary device requests data from the GDC21D301A.
\DATA_STRB	108	O	**Auxiliary Data Strobe (active low).** This signal qualifies data contained in VAD_DATA[7:0]. This auxiliary decoder should latch the auxiliary data on the rising edge of DATA_STRB.
\DATA_DCS	107	O	**Auxiliary Select (active low).** This signal activates data transfers between the auxiliary decoder and the host processor. Host processor can access the registers of the auxiliary decoder.
BOF_D	97	I	**Begin of Frame2.** On the rising edge of this signal, STC, the counted PCR value, is copied to STC3_reg.
SCAN TEST			
SCAN_MODE	44	I	**Scan Test Mode Enable Input.** It has to be connected to VSS level.
SCAN_TEST	45	I	**Scan Test Mode Enable Input.** It has to be connected to VSS level.
SCAN_IN1	46	I	**Scan-path Input on Scan Test Mode.** It has to be connected to VSS level.
SCAN_OUT1	111	O	**Scan-path Output on Scan Test Mode**
POWER AND GROUND			
VDD	7, 10, 33, 48, 58,68,70,82, 100,113,121, 124	PWR	**3.3 V Power Supply**
VSS	4,15,24,35, 53,63,72,77, 87,102,106, 118,130	GND	**Ground**

4. Block Diagram

The figure 2 shows the internal block diagram of the GDC21D301A. This chip receives the byte-parallel/bit-serial transport data from FEC(Forward-Error-Correction) device, and stores the whole data into DRAM. After decoding the transport data in DRAM, it de-multiplexes audio, video, and auxiliary data packets, and transfers them into the corresponding decoder devices through the decoder interface blocks. The host processor can control the GDC21D301A and access the decoder devices and DRAM through the host interface. The GDC21D301A generates PWM pulses to control the frequency of system clock and audio clock. The pulse width of PWM can be programmed by the host processor.

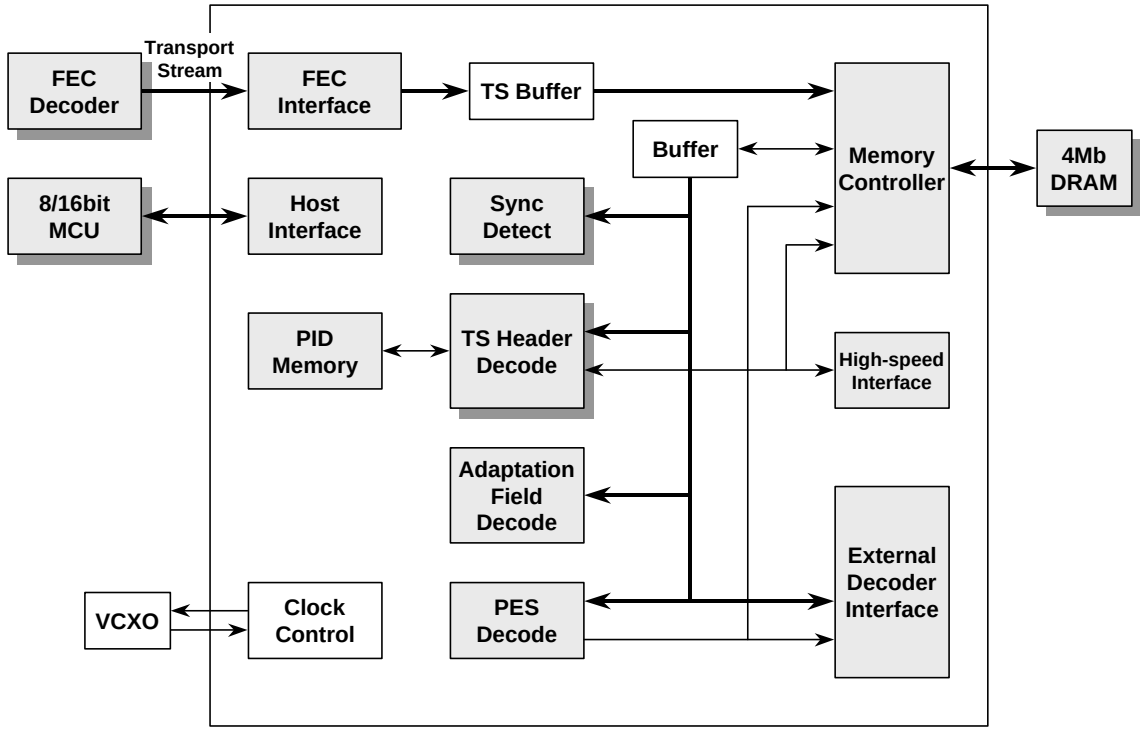


Figure 2. The Block Diagram of the Transport Decoder

5. Functional Description

5.1 Forward-Error-Correction (FEC) Interface

The GDC21D301A can receive Transport Stream packets in byte-parallel or bit-serial mode. FEC Interface block gets these TS data, and temporarily saves them in the internal buffer(TS Buffer).
In bit-serial mode, F_START should be activated(high) when the most significant bit or the first bit of each packet is fed. \ERR_BLOCK pin is used to indicate valid packet, and D_VALID pin to indicate valid TS data (it should be deactivated at parity bits). TS data is fed on the rising edge of FEC_CLOCK.

5.2 Sync Detector

This block searches the sync byte of TS packet(0x47) at *Sync Hysterisis* register during specified time. If it detects correct sync data, then TS Header Decoder block takes control of decoding process.

5.3 TS Header Decoder

This block decodes Transport Stream header and determines if packet should be decoded further by comparing PID with the values in internal PID memory. PSI data is stored in external DRAM, and can be read by the host processor. If *high speed out enable(Hig)* bit in PID registers is activated, the whole corresponding TS data are output to high-speed ports (refer to **Register Description** section).

5.4 Adaptation Field Decoder

Refer to the **Register Description** section

5.5 PES Decoder

This block decodes PES header and de-multiplexes payload data to appropriate parts (refer to **Register Description** section).
Audio and auxiliary data are stored in DRAM, re-read by the GDC21D301A, and sent to external decoder. But video data is directly output to the external decoder.

5.6 Memory Controller

This controls DRAM interface. It refreshes DRAM, writes and reads data to and from DRAM. The corresponding addresses where the data is written and read are stored in pointer memory by the Host processor. The GDC21D301A requires one or two DRAMs (256Kx16b or 1Mx16b).

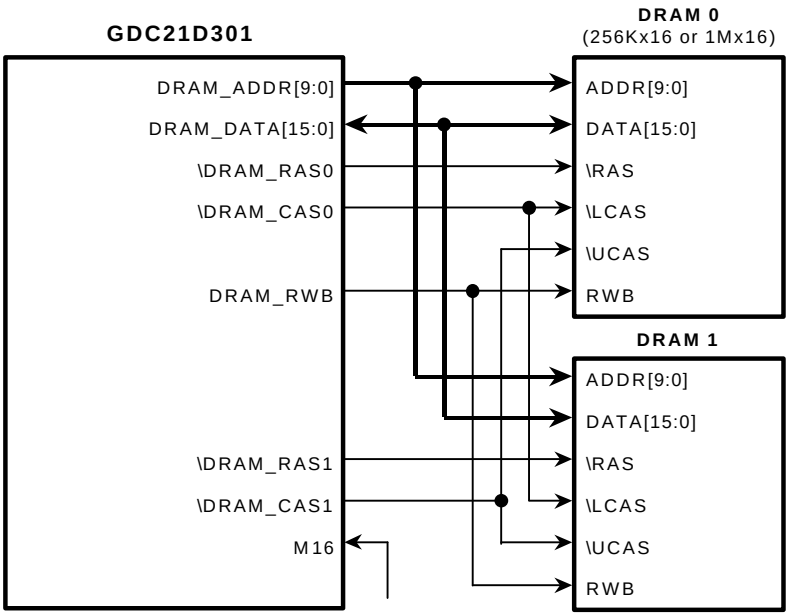


Figure 3. External DRAM Interface

5.7 High-Speed Interface

This is an interface block of external high-speed ports which send whole TS packets.

5.8 External Decoder Interface

This reads data from buffer and sends it to the corresponding external decoder. It also controls the input/output of data to and from external decoder.

5.9 Host Interface

Host Processor can access external decoders through the GDC21D301A transport decoder. **DSP_DATA[15:0]** ports are used for data bus.

To access one of the external decoders through the GDC21D301A, host address bus (**DSP_ADDR[22:0]**) should be as follows.

For video decoder access,
DSP_ADDR[22:18] = “100 11”.

For audio decoder access,
DSP_ADDR[22:18] = “100 01”.

For auxiliary decoder access,
DSP_ADDR[21:18] = “100 00”.

5.10 Clock Controller

It outputs two PWM signals(VPWM and APWM) which can be controlled by the Host Processor. The PWM signals can be used to control external VCXOs.

6. Register Description

This chapter describes the registers in the GDC21D301A. Table 1 summarizes these registers. Note the following general information:

- All registers are 16-bit wide and can read/write unless especially noted.
- All accesses to internal registers are allowed by word or byte using **DSP_ADDR[0]** pin which determines access mode unit.
- The reserved bits should be written to zero to preserve compatibility with future features.
- Register addresses that are not defined in Table 1 are reserved. Read from these locations causes unpredictable results. It is recommended not to access these registers.
- In order to access these register, you should set **DSP_ADDR[22:18]** to "100 11".

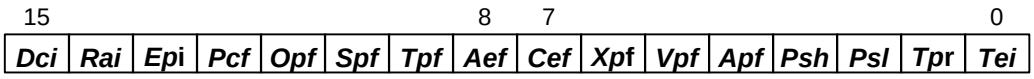
Table 1. Register Summary

ADDR[A10:A0]	R/W	REGISTERS	DEFINITION
000	R/W	Interrupt Flag 1	Indicates active interrupts
002	R/W	Interrupt Flag 2	Indicates active interrupts
004	R/W	Interrupt Mask 1	Interrupt Enable
006	R/W	Interrupt Mask 2	Interrupt Enable
008	R/W	Instruction	Controls the decoding
00a	R/W	Round Buffer	Controls Buffer Management
00c	R	PID Flag 1	Current Packet transferred
00e	R	PID Flag 2	Current Packet transferred
010	R/W	PWM control 1	Controls PWM output
012	R/W	PWM control 2	Controls PWM output
014	R/W	Sync Hysterisis	Sets lock/unlock parameters for sync detect
02a ~ 02e	R	PTS	PTS of Current Packet transferred
030 ~ 034	R	DTS	DTS of Current Packet transferred
036 ~ 03c	R	PCR	PCR of Current Packet transferred
040	R	splicing_count_ down	Current Splicing Countdown transferred
042,044	R	ES_rate	Current ES rate transferred
046	R	DSM_trick_mode	Current DSM trick mode transferred
048	R	additional_copy_info	Additional copy information
060,062	R	STC 1	STC register contains the instant value of internal STC counter when new PCR is transferred.
064,066	R	STC 2	STC register contains the instant value of internal STC counter when the beginning of frame signal(BOF1) is detected.
068,06a	R	STC 3	STC register contains the instant value of internal STC counter when the beginning of frame signal(BOF2) is detected.
06c,06e	R	STC 4	STC register contains the instant value of internal STC counter when the beginning of frame signal(BOF3) is detected.
070,072	R	STC 5	STC register contains the instant value of internal STC counter when STC fetch instruction is activated.
400,402	R/W	Vid PID (0)	Assigns Video PID
404,406	R/W	Aud PID (1)	Assigns Audio PID
408,40a	R/W	Aux PID (2)	Assigns Auxiliary PID
40c,40e	R/W	PSI_3 PID	Assigns PSI_3 PID
410 ~ 47a	R/W	PSI_4 ~ PSI_30 PID	Assigns PSI_4 ~ PSI_30 PID
47c,47e	R/W	PSI_31 PID	Assigns PSI_31 PID

Table 1. Register Summary (*continued*)

ADDR[A10:A0]	R/W	REGISTERS	DEFINITION
618 ~ 61e	R/W	PSI_3's data buffer pointer	Start, End, Read, and Write Address
620 ~ 6f6	R/W	PSI_4 ~ PID_30's data buffer pointer	Start, End, Read, and Write Address
6f8 ~ 6fe	R/W	PSI_31's data buffer pointer	Start, End, Read, and Write Address
700 ~ 706	R/W	channel buffer pointer	Start, End, Read, and Write Address
708 ~ 70e	R/W	audio compressed data buffer pointer	Start, End, Read, and Write Address
710 ~ 716	R/W	audio PES extension data buffer pointer	Start, End, Read, and Write Address
718 ~ 71e	R/W	video PES extension data buffer pointer	Start, End, Read, and Write Address
720 ~ 726	R/W	auxiliary compressed data buffer pointer	Start, End, Read, and Write Address
728 ~ 72e	R/W	auxiliary PES extension data buffer pointer	Start, End, Read, and Write Address
730 ~ 736	R/W	transport_private_data buffer pointer	Start, End, Read, and Write Address
738 ~ 73e	R/W	adf_extension_data buffer pointer	Start, End, Read, and Write Address

Interrupt Flag 1 (0x000)

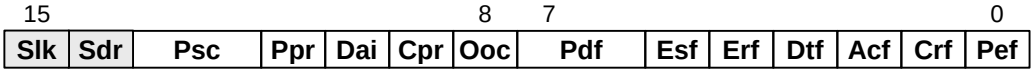


FIELD	BITS	DESCRIPTION	VALUES	DEFAULT
Dci	15	discontinuity_indicator		
Rai	14	random_access_indicator		
Epi	13	elementary_stream_priority_indicator		
Pcf	12	PCR_flag		
Opf	11	OPCR_flag		
Spf	10	splicing_point_flag		
Tpf	9	transport_private_flag		
Aef	8	adaptation_field_extension_flag		
Cef	7	continuity counter error		
Xpf	6	auxiliary packet comes		
Vpf	5	video packet comes		
Apf	4	audio packet comes		
Psh	3	one of PSI16 ~ PSI_31 packets comes		
Psl	2	one of PSI3 ~ PSI_15 packets comes		
Tpr	1	transport_priority		
Tei	0	transport_error_indicator		

Interrupt Flag 2 (0x002)

When an interrupt condition occurs, the corresponding bit in **Interrupt Flag** registers are asserted 1. Whenever a bit in the Interrupt Flag is 1, the corresponding bit in Interrupt Mask registers is set to 1, the *Ien* bit in the Instruction register to 1, and the GDC21D301A asserts **DSP_INT,** the external interrupt signal. Note that the occurrence of an interrupt condition always causes the corresponding bit in **Interrupt Flag** registers to be set, even if the condition is disabled(i.e., the corresponding bit in **Interrupt Mask** registers is set to 0).
Interrupt Flag 1, 2 registers are cleared by the Host whenever they are read, and **DSP_INT** is deasserted.

In the GDC21D301A, ***Slk*** and ***Sdr*** is added to indicate the state of Sync. The GDC21D301A first searches Sync byte from transport stream. If the device succeeds in finding 0x47, it writes ***Slk***(Sync_lock) bit in Interrupt flag 2 register. Until sync is detected, Sdr flag maintains active high state, so the host processor can monitor whether Sync(0x47) is detected or not.
All bits except ***Slk*** and ***Sdr*** are set when packet is matched to PID register.



FIELD	BITS	DESCRIPTION	VALUES	DEFAULT
Slk	15	Sync_lock		
Sdr	14	Sync_drop		
Psc	13:12	PES_scrambling_control		
Ppr	11	PES_priority		
Dai	10	data_alignment_indicator		
Cpr	9	copyright		
Ooc	8	original_or_copy		
Pdf	7:6	PTS_DTS_flag		
Esf	5	ESCR_flag		
Erf	4	ES_rate_flag		
Dtf	3	DSM_trick_mode_flag		
Acf	2	additional_copy_info_flag		
Crf	1	PES_CRC_flag		
Pef	0	PES_extension_flag		

Interrupt Mask 1 (0x004)

All bits respectively correspond with each ones in **Interrupt Flag 1** register.

1 = Interrupt enabled

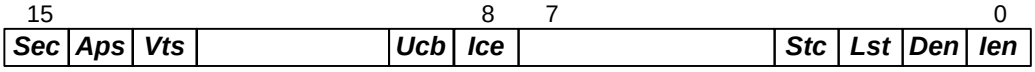
Interrupt Mask 2 (0x006)

All bits respectively correspond with each ones in **Interrupt Flag 2** register.

1 = Interrupt enabled

Instruction (0x008)

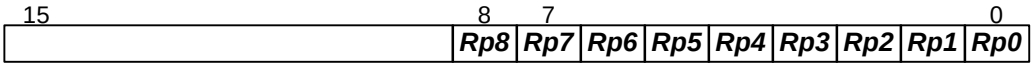
When error(discontinuity) happens in video packet, i.e., in case *Sec*='1', the GDC21D301A inputs video sequence error code in data output.
In case *Aps*='0', the GDC21D301A outputs audio compressed data in parallel mode, and in case *Aps*='1', the GDC21D301A outputs the data in serial mode through **AUD_SER_DATA** pin.
When *Vts* is 1, the GDC21D301A inputs PTS and DTS data before sending them to video packet according to *Pdf* flag bit of **Interrupt Flag 2** register. When *Ucb* is 1, the GDC21D301A receives data from channel input.
When *Ice* is 1, the GDC21D301A ignores channel empty condition(i.e., the GDC21D301A continues decoding data in channel buffer whether they were decoded before or not.).
When *Stc* is 1, the GDC21D301A loads internal PCR counter to **STC5** register, and then this bit is cleared automatically. In case *Lst* is 1, the GDC21D301A loads internal PCR counter with new value when next PCR value is loaded in the packet, and then this bit is cleared automatically.



FIELD	BITS	DESCRIPTION	VALUES	DEFAULT
Sec	15	Sequence_error_code	1=sequence_error_code inserted	
Aps	14	Audio parallel/serial output	0=parallel 1= serial	
Vts	13	Video PTS,DTS output	1=PTS/DTS inserted	
Ucb	9	Update channel buffer		
Ice	8	Ignore channel empty		
Stc	3	load STC5		
Lst	2	load PCR		
Den	1	Global decoding enable	1=decoding enable	
Ien	0	Global Interrupt enable	1=interrupt enable	

Round Buffer (0x00a)

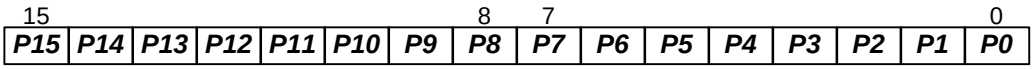
When *Rp*n is 1, write pointer is reached to end pointer, and the write pointer is changed to start pointer(i.e., the GDC21D301A overwrites the following data).



FIELD	BITS	DESCRIPTION	VALUES	DEFAULT
*Rp*n	8:0	Round the buffer of the **PSI**_n		

PID Flag 1 (0x00c)

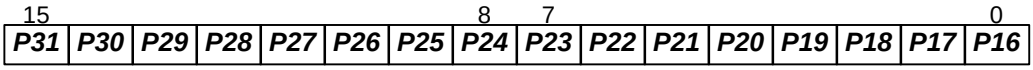
When the GDC21D301A decodes the packet whose PID is activated for decoding, it sets the corresponding bit in **PID Flag 1**, or **2** register.



FIELD	BITS	DESCRIPTION	VALUES	DEFAULT
P15 ~ P3	15:3	PID flag for **PSI_15 ~ PSI_3**		
P2	2	**Auxiliary PID** flag		
P1	1	**Audio PID** flag		
P0	0	**Video PID** flag		

PID Flag 2(0x00e)

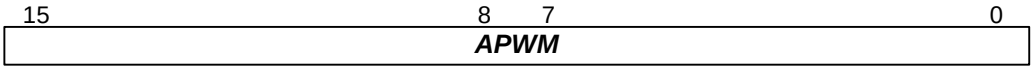
These bits indicate the type of the packet which the GDC21D301A is now decoding.



FIELD	BITS	DESCRIPTION	VALUES	DEFAULT
P31 ~ P16	15:0	PID flag for **PSI_31 ~ PSI_16**		

APWM control (0x010)

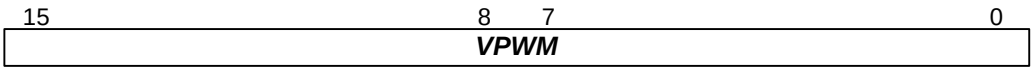
APWM output signal is generated by this value. External VCXO for audio can be controlled by this value and the lip synchronization between video and audio clock. The control of this register is the same as that of VPWM.



FIELD	BITS	DESCRIPTION	VALUES	DEFAULT
APWM	15:0	Audio PWM control	0x0000 to 0xFFFF	0x7FFF

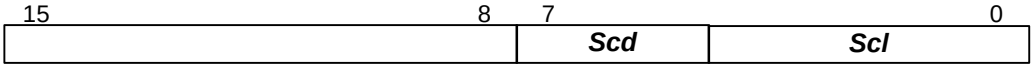
VPWM control (0x012)

The chip uses Sigma-delta modulation for VPWM signal. Modulation clock is 1/34 system clock(27MHz/34 = 794KHz). VPWM output signal is generated by this value. When the register value is 0x7FFF, the period of '1' and the period of '0' have the same value of 0.630usec, and the cycle time is 1.259usec, i.e., the duration of VPWM output signal is 50%. The larger is the value greater than 0x7FFF, the longer is the high period generated. For example, if register value is 0x0000, there is no data of '1' in 65536 data. Only the data of '0' is almost uniformly distributed in 65536 data. Adjusting PWM pulse, system VCXO can be controlled to achieve lip synchronization or system clocks locking.



FIELD	BITS	DESCRIPTION	VALUES	DEFAULT
VPWM	15:0	Video PWM control	0x0000 to 0xFFFF	0x7FFF

Sync Hysteresis (0x014)

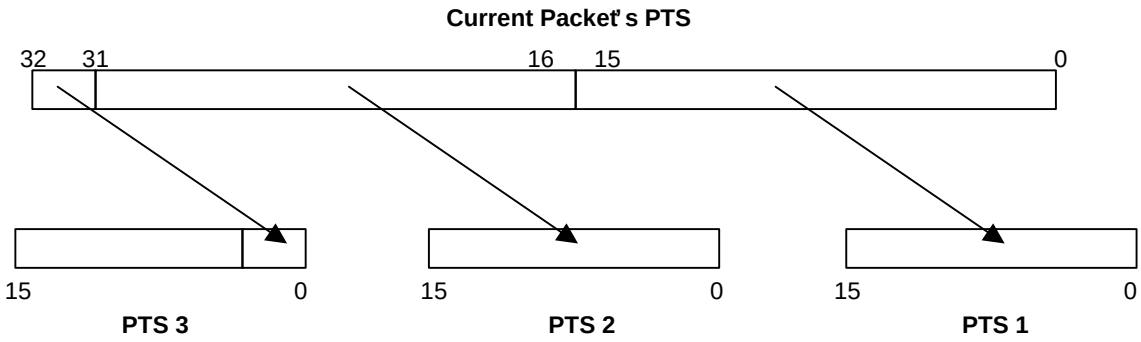


FIELD	BITS	DESCRIPTION	VALUES	DEFAULT
Scd	7:5	Sync Drop	0 = should not be used 1 – 7 = The number of consecutive sync bytes must be discarded to constitute a sync drop.	0x1
Scl	4:0	Sync Lock	0 = should not be used 1 – 31 = The number of consecutive sync bytes must be detected before sync is acquired.	0x03

PTS (0x02a ~ 0x02e)

PTS Register 1 (0x02a)
PTS Register 2 (0x02c)
PTS Register 3 (0x02e)

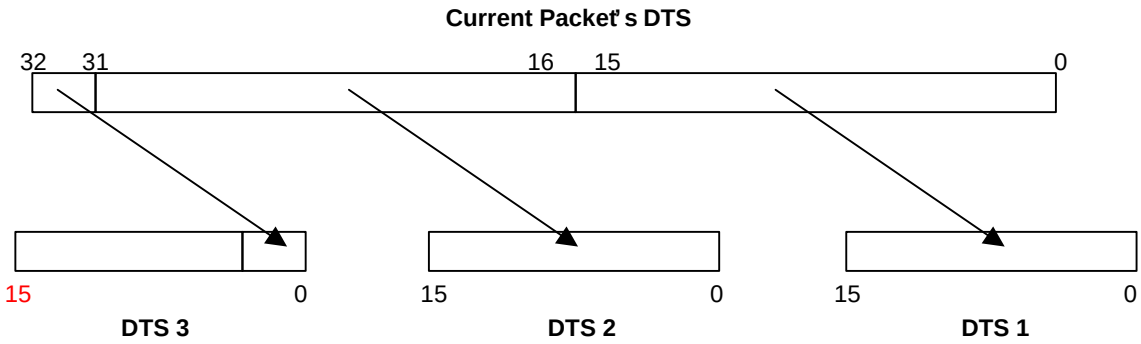
These read-only registers hold the PTS value that GDC21D301A retrieves from the transport packet whose PID value is activated for decoding.



DTS (0x030 ~ 0x034)

DTS Register 1 (0x030)
DTS Register 2 (0x032)
DTS Register 3 (0x034)

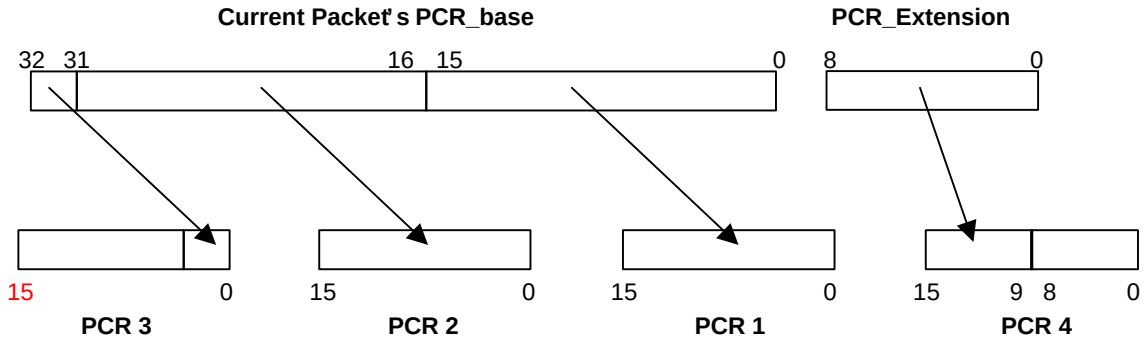
These read-only registers hold the DTS value that GDC21D301A retrieves from the transport packet whose PID value is activated for decoding.



PCR (0x036 ~ 0x03c)

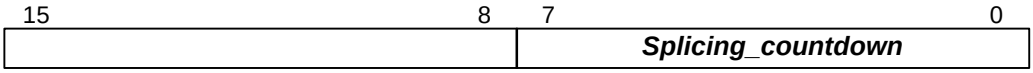
PCR Register 1 (0x036)
PCR Register 2 (0x038)
PCR Register 3 (0x03a)
PCR Register 4 (0x03c)

These read-only registers hold the PCR value that the GDC21D301A retrieves from the transport packet whose PID value is activated for decoding.



Splicing_countdown (0x040)

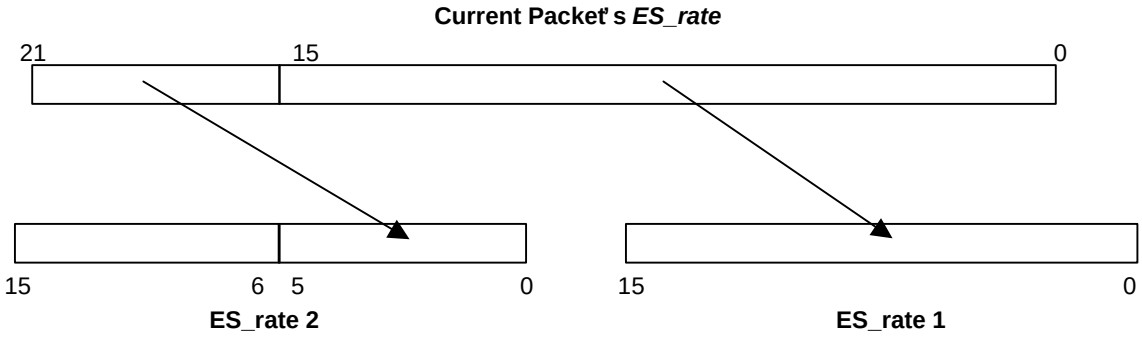
This read-only register holds the *splicing_countdown* value that the GDC21D301A retrieves from the transport packet whose PID value is activated for decoding.



ES_rate (0x042 ~ 0x044)

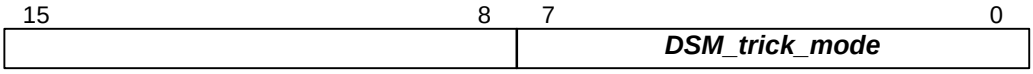
ES_rate Register 1 (0x042)
ES_rate Register 2 (0x044)

These read-only registers hold the ***ES_rate*** value that the GDC21D301A retrieves from the transport packet whose PID value is activated for decoding.



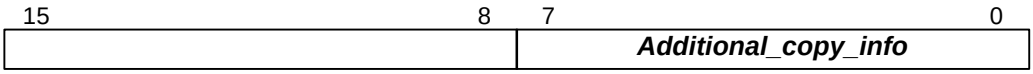
DSM_trick_mode (0x046)

This read-only register holds the ***DSM_trick_mode*** field that the GDC21D301A retrieves from the transport packet whose PID value is activated for decoding.



Additional_copy_info (0x048)

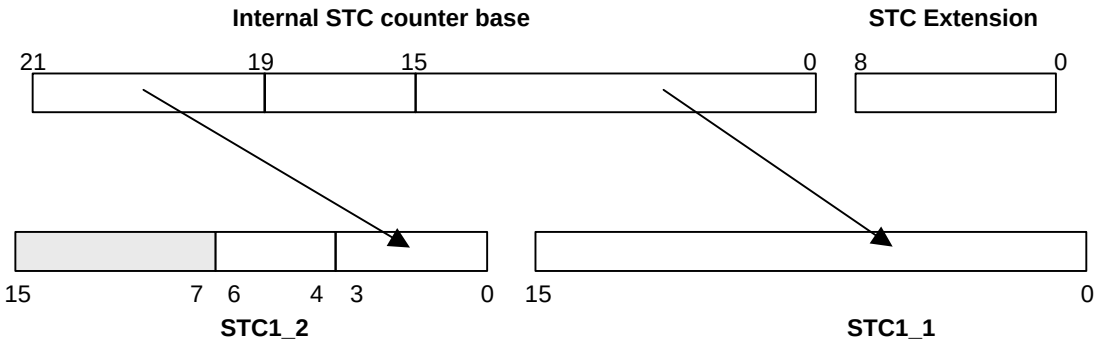
This read-only register holds the ***additional_copy_info*** field that the GDC21D301A retrieves from the transport packet whose PID value is activated for decoding.



STC1 (0x060 ~ 0x062)

STC1 Register 1 (0x060)
STC1 Register 2 (0x062)

These read-only registers hold the lower 20 bits of STC value from the internal STC counter of the GDC21D301A when the GDC21D301A retrieves the PCR value from the transport packet whose PID value is activated for decoding. The internal STC counter is clocked at the frequency of input on **CLOCK_27M** pin (nominally 27 MHz). In the GDC21D301A, STC_Extension is written to *STC1_2[15:7]* and can be read by user. STC1 is also read-only register.



STC2 (0x064 ~ 0x066)

STC2 Register 1 (0x064)
STC2 Register 2 (0x066)

These read-only registers hold the lower 20 bits of STC value from the internal STC counter of the GDC21D301A when external **BOF1** signal is detected.

STC3 (0x068 ~ 0x06a)

STC3 Register 1 (0x068)
STC3 Register 2 (0x06a)

These read-only registers hold the lower 20 bits of STC value from the internal STC counter of the GDC21D301A when external **BOF2** signal is detected.

STC4 (0x06c ~ 0x06e)

STC4 Register 1 (0x06c)
STC4 Register 2 (0x06e)

These read-only registers hold the lower 20 bits of STC value from the internal STC counter of the GDC21D301A when external BOF3 signal is detected.

STC5 (0x070 ~ 0x072)

STC5 Register 1 (0x070)
STC5 Register 2 (0x072)

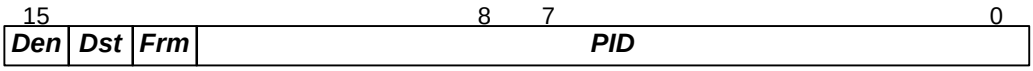
These read-only registers hold the lower 20 bits of STC value from the internal STC counter of the GDC21D301A when STC fetch instruction is activated(see Instruction Register).

PID Registers (0x400 ~ 0x47e)

These registers should be written with certain values during initialization phase, because the values are undefined at first. Video, audio, and auxiliary packet will be respectively transferred to **VAD_DATA** port with **VID_STRB, AUD_STRB, and DATA_STRB** signal in case *Hig* bit in the register is '0'(i.e. High Speed Port has the highest priority. This is equally applied to other packets.). Other data will be transferred to the corresponding buffer in DRAM.

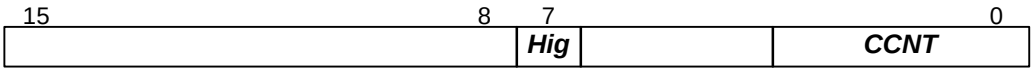
Vid PID Register (0x400, 0x402)

These registers should be written with certain values during initialization phase, because the values are undefined at first. For correct processing, *Dst* should be written to '0'.



Field	Bits	Description	Values	Default
Den	15	PID enable	1 = PID matching enabled	
Dst	14	Decoding state(status reg.)	1 = corresponding PID packet occurred at least once before	
Frm	13	Decoding Type	0 = transfer PES_payload to external port 1 = transfer whole PES packet	
PID	12:0	PID		

These registers should be written with certain values during initialization phase, because the values are undefined at first.



Field	Bits	Description	Values	Default
Hig	7	High Speed out enable	1 = transfer whole TS packet to high speed port	
CCNT	3:0	Continuity Counter	store *continuity_counter* value	

Aud PID Register (0x404, 0x406)

Same as **Vid PID** register, but Audio packet

Aux PID Register (0x408, 0x40a)

Same as **Vid PID** register, but Auxiliary packet

PSI PID Register (0x40c ~ 0x40e)

Same as **Vid PID** register, except the following.

Field	Bits	Description	Values	Default
Frm	13	Decoding Type	0 = This packet is a kind of PES. 1 = This packet is a kind of PSI.	

In PES packet, there is no ***pointer_field***.

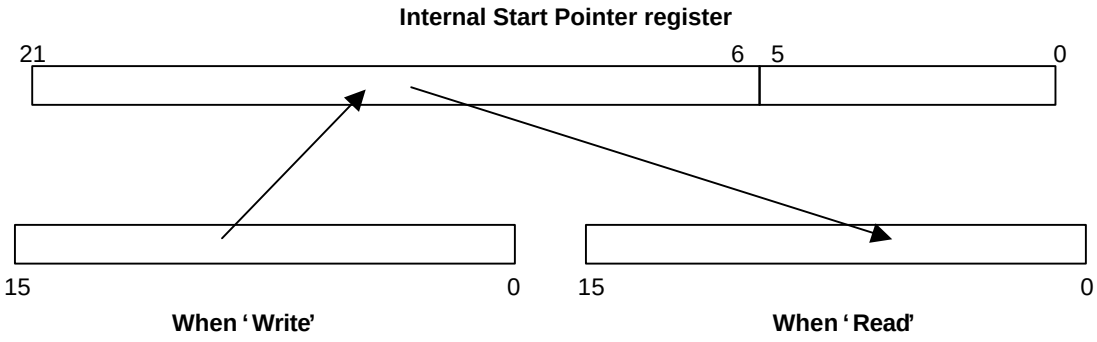
Buffer Pointer Register (0x618 ~ 0x61e)

The values are undefined initially. These values are the memory management registers for local DRAM. These are 22-bit wide registers only whose 16 bits can be accessed by the host.
In the following, N = n-2 and n = 3, 4, 5, ... , 31.

PSI_n's data Buffer Start Pointer Register (0x618 + 4*N)

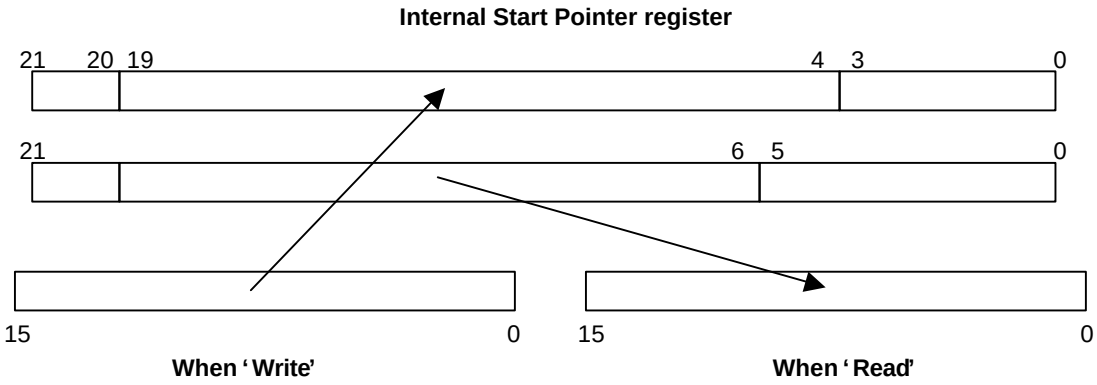
1) When M16 = '1' (16Mbit DRAM used)

When it is 'Write', the lower 6 bits are written to



2) When M16 = ‘0’ (4Mbit DRAM used)

When it is ‘Write’, the lower 4 bits and higher 2 bits are written to



PSI_n's data Buffer End Pointer Register (0x61a+ 4*N)

Same as **Start pointer** register. But the real end address of data buffer is one less than this register value, for example, the real end address of PSI_4 data buffer is equal to 0x61b which is calculated by '0x61c minus 0x001'. The buffer size is calculated by the following.

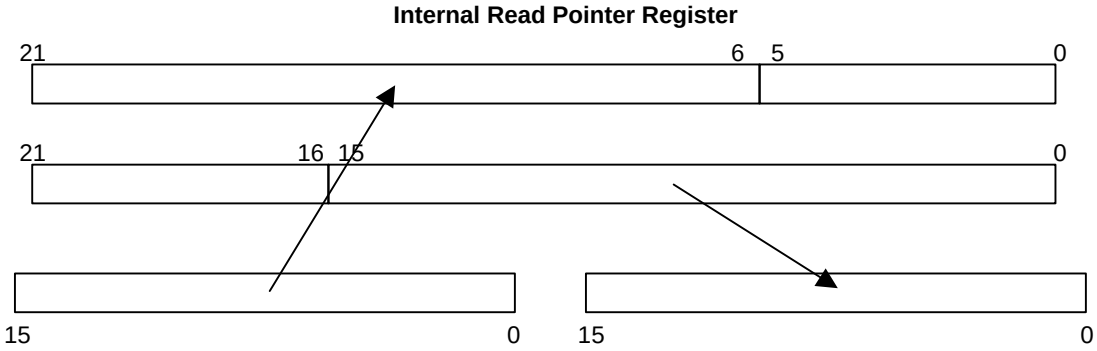
Size = End Pointer - Start Pointer.

PSI_n's data Buffer Read Pointer Register (0x61c + 4*N)

Actually this register is not used. In order to read data in this buffer, you should access local DRAM directly like accessing internal register.

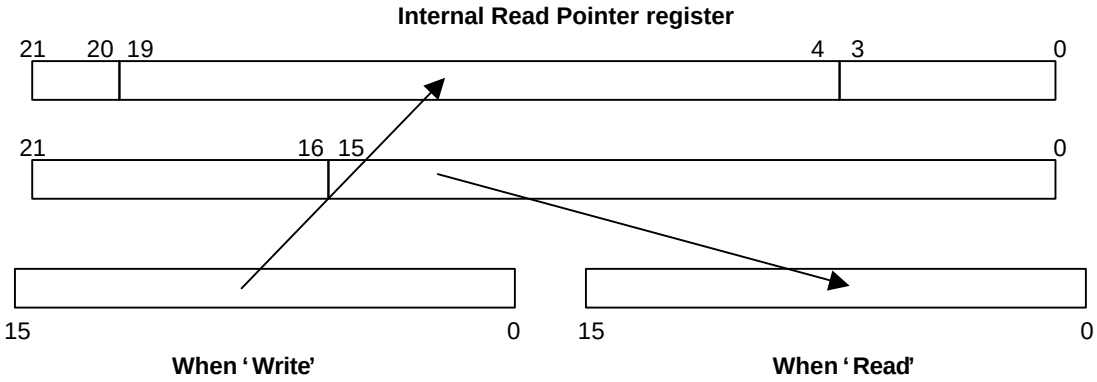
1) When M16 = '1' (16Mbit DRAM used)

When it is 'Write', the lower 6 bits are written to located between start and end pointer. It is recommended that the initial value is the same of the start pointer. When 'Read', the lower 16 bits are read.



2) When M16 = '0' (4Mbit DRAM used)

When it is 'Write', the lower 4 bits and higher 2 bits are written to '0', and the value should be located between start and end pointer. It is recommended that this initial value is the same of start pointer value. When 'Read', the lower 16 bits are read.



PSI_n's data Buffer Write Pointer register (0x61e + 4*N)

Same as **Read pointer** register. This value should be located between start and end pointer. It is recommended that this initial value is the same of start pointer value. (See **Round Buffer** register 0x005)

Channel buffer pointer (0x700 ~ 0x706)

Same as **PSI_n's data buffer pointer** register. This buffer is used to store FEC input data. the GDC21D301A will read the data from this buffer to decode TS packets. The read pointer is used to read data.

Audio compressed data buffer pointer (0x708 ~ 0x70e)

Same as **PSI_n's data buffer pointer** register. This buffer is used to store the data which is sent to external audio decoder. the GDC21D301A will read the data from this buffer to send them to external audio decoder. The read pointer is used to read data.

Audio PES_extension data buffer pointer(0x710 ~ 0x716)

Same as **PSI_n's data buffer pointer** register. This buffer is used to store the PES_extension data of audio packets. Before storing the PES_extension data, the GDC21D301A writes the size of the PES_extension data + ***stuffing_bytes***. The read pointer is not used by the GDC21D301A.

Video PES_extension data buffer pointer (0x718 ~ 0x71e)

Same as **PSI_n's data buffer pointer** register. This buffer is used to store the PES_extension data of video packets. Before storing the PES_extension data, the GDC21D301A writes the size of the PES_extension data + s***tuffing_bytes***. The read pointer is not used by the GDC21D301A.

Auxiliary compressed data buffer pointer (0x720 ~ 0x726)

Same as **PSI_n's data buffer pointer** register. This buffer is used to store the data which is sent to external auxiliary decoder. the GDC21D301A will read the data from this buffer to send them to external auxiliary decoder. The read pointer is used to read data.

Auxiliary PES_extension data buffer pointer (0x728 ~ 0x72e)

Same as **PSI_n's data buffer pointer** register. This buffer is used to store the PES_extension data of auxiliary packets. Before storing the PES_extension data, the GDC21D301A writes the size of the PES_extension data + ***stuffing_bytes***. The read pointer is not used by the GDC21D301A.

Transport_private_data buffer pointer (0x730 ~ 0x736)

Same as **PSI_n's data buffer pointer** register. This buffer is used to store transport_private_data field. The read pointer is not used by the GDC21D301A.

Adf_extension_data buffer pointer (0x738 ~ 0x73e)

Same as **PSI_n's data buffer pointer** register. This buffer is used to store ***Adf_extension_data*** field. The read pointer is not used by the GDC21D301A.

7. Electrical Specification

7.1 Absolute Maximum Rating

SYMBOL	PARAMETERS	VALUES	UNIT
V_{DD}	Power Supply Voltage	-0.33 to 5.5	V
V_I	Digital Input Voltage	-0.33 to V_{DD} + 0.5	V
Vo	Digital Output Voltage	-0.33 to V_{DD} + 0.5	V
T_{stg}	Storage Temperature	-55 to 125	¡ É
P_d	Power Dissipation	1.0	W

Note : Absolute Maximum Ratings means that the safety of the device cannot be guaranteed beyond these values and it doesn't imply that the device should be operated within these limits.

7.2 Recommended Operating Range

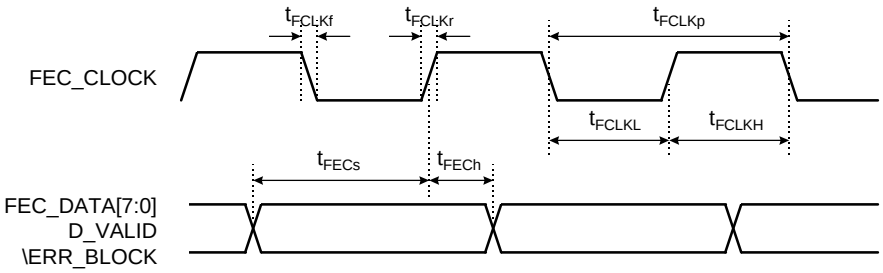
SYMBOL	PARAMETERS	VALUES	UNIT
V_{DD}	Power Supply Voltage	3.3 ± 10%	V
T_{opr}	Operating Temperature	0 to 70	¡ É

7.3 DC Characteristics (VDD = 3.3 V ± 10%, TA = 0 ~ 70 °C)

SYMBOL	PARAMETERS	MIN	MAX	UNIT
V_{IH}	Input High Voltage	0.7 X V_{DD}	V_{DD} + 0.33	V
V_{IL}	Input Low Voltage	-0.33	0.2 X V_{DD}	V
V_{OH}	Output High Voltage	2.4	V_{DD}	V
V_{OL}	Output Low Voltage	0	0.4	V
I_{DD}	Dynamic Supply Current	-	150	mA
I_{DDQ}	Quiescent Supply Current	-	1	uA
F_{opr}	Max. Operating Frequency	-	27	MHz

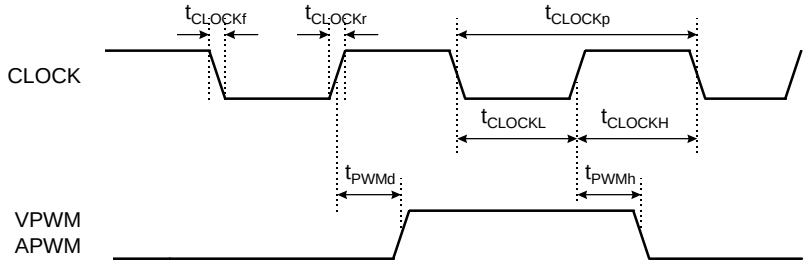
7.4 AC Characteristics (VDD = 3.3 V ± 10%, TA = 0 ~ 70 °C)

7.4.1 Transport Stream Interface Requirements



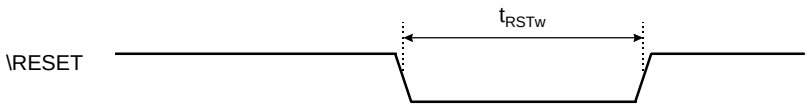
PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
tFECh	FEC_CLOCK to FEC_DATA hold time	5	-	-	ns
tFECs	FEC_CLOCK to FEC_DATA setup time	5	-	-	ns
tFCLKr	FEC_CLOCK rising time	-	-	1.5	ns
tFCLKf	FEC_CLOCK falling time	-	-	1.5	ns
tFCLKH	FEC_CLOCK high duration	10	-	-	ns
tFCLKL	FEC_CLOCK low duration	10	-	-	ns
tFCLKp	FEC_CLOCK period	100	-	-	ns

7.4.2 Clock Interface Requirements



PARAMETER	PARAMETER	MIN	TYP	MAX	UNIT
tCLOCKH	CLOCK high duration	10	-	-	ns
tCLOCKL	CLOCK low duration	10	-	-	ns
tCLOCKr	CLOCK rising edge	-	-	1.5	ns
tCLOCKf	CLOCK falling edge	-	-	1.5	ns
tCLOCKp	CLOCK period	36	-	37	ns
tPWMD	PWM delay time	-	-	18	ns
tPWMH	PWM hold time	-	-	18	ns

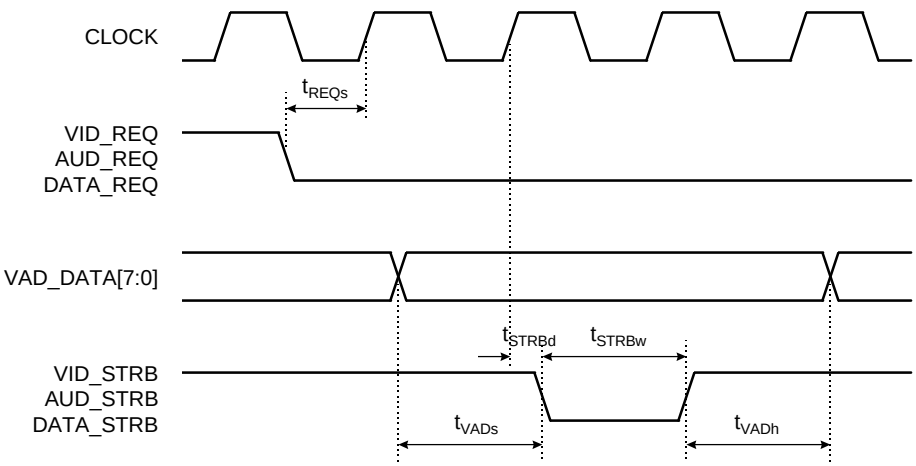
7.4.3 Reset Signal Requirement



PARAMETER	PARAMETER	MIN	TYP	MAX	UNIT
t_{RSTw}	RESET pulse width	t_{CLOCKp}	-	-	ns

The low pulse width of reset signal should be larger than t_{CLCOKp}, the operating clock period.

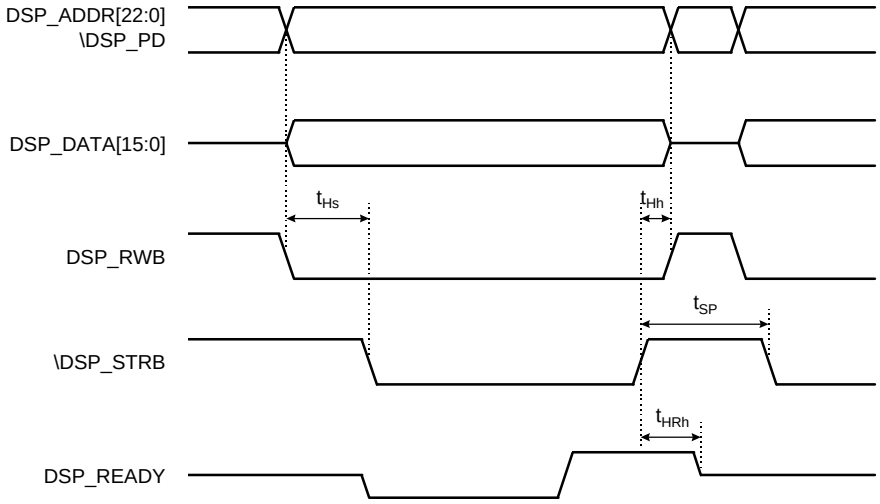
7.4.4 Audio/Video/Data Decoder Interface Requirements



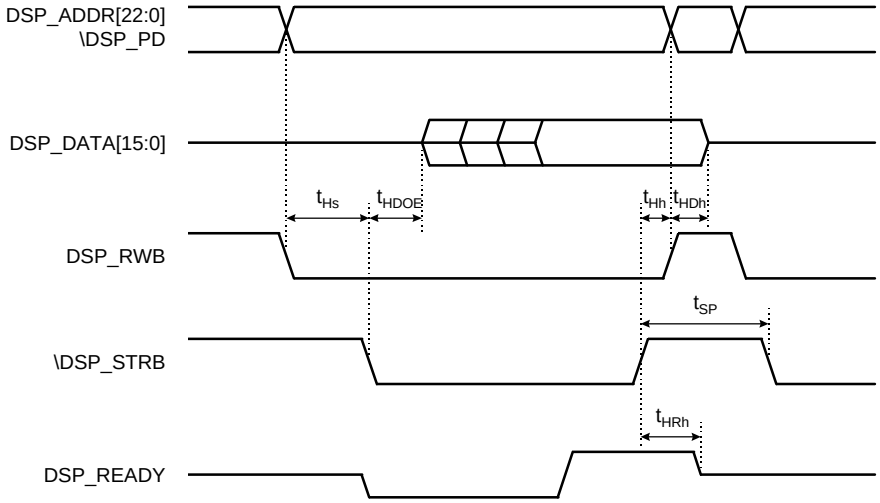
PARAMETER	PARAMETER	MIN	TYP	MAX	UNIT
t_{VADs}	VAD data setup time	30	-	-	ns
t_{VADh}	VAD data hold time	30	-	-	ns
t_{STRBd}	STRB to clock delay time	-	-	18	ns
t_{STRBw}	STRB pulse width	30	-	-	ns
t_{REQs}	REQ setup time	5	-	-	ns

7.4.5 Host Processor Interface Requirements

Host Write Mode



Host Read Mode



PARAMETER	PARAMETER	MIN	TYP	MAX	UNIT
t_{Hs}	Host setup time	0	-	-	ns
t_{Hh}	Host hold time	0	-	-	ns
t_{HRh}	HREADY hold time	-	-	37	ns
t_{HDOE}	Host data output enabled	0	-	-	ns
t_{HDh}	Host data hold time	2	-	-	ns
t_{SP}	Strobe precharge time	37	-	-	ns

8. Package Mechanical Data

8.1 Package Pin out

PIN	TYPE	NAME	PIN	TYPE	NAME
1	I/O	DSP_DATA[13]	45	I	SCAN_TEST
2	I/O	DSP_DATA[14]	46	I	SCAN_IN1 / TA[9]
3	I/O	DSP_DATA[15]	47	I	M16
4	GND	VSS	48	PWR	VDD
5	O	DSP_INT	49	O	DRAM_RWB
6	O	DSP_READY	50	O	DRAM_ROW_COL_ADDR[9]
7	PWR	VDD	51	O	DRAM_ROW_COL_ADDR[8]
8	O	TDO0	52	O	DRAM_ROW_COL_ADDR[7]
9	O	TDO1	53	GND	VSS
10	PWR	VDD	54	O	DRAM_ROW_COL_ADDR[6]
11	O	HSDEN	55	O	DRAM_ROW_COL_ADDR[5]
12	O	HIGH_SP_DATA[1]	56	O	DRAM_ROW_COL_ADDR[4]
13	O	HIGH_SP_DATA[0]	57	O	DRAM_ROW_COL_ADDR[3]
14	O	CLOCK_OUT	58	PWR	VDD
15	GND	VSS	59	O	DRAM_ROW_COL_ADDR[2]
16	I	TA[7]	60	O	DRAM_ROW_COL_ADDR[1]
17	I	TA[6]	61	O	DRAM_ROW_COL_ADDR[0]
18	I	TA[5]	62	O	\DRAM_RAS1
19	I	TA[4]	63	GND	VSS
20	I	TA[3]	64	O	\DRAM_RAS0
21	I	TA[2]	65	O	\DRAM_CAS1
22	I	TA[1]	66	O	\DRAM_CAS0
23	I	TA[0]	67	I/O	DRAM_DATA[15]
24	GND	VSS	68	PWR	VDD
25	I	TWEB	69	I	CLOCK_27M
26	I	TEST	70	PWR	VDD
27	I	TDI	71	-	NC
28	I	P_S_MODE	72	GND	VSS
29	I	F_START	73	I/O	DRAM_DATA[14]
30	I	FEC_DATA[7]	74	I/O	DRAM_DATA[13]
31	I	FEC_DATA[6]	75	I/O	DRAM_DATA[12]
32	I	FEC_CLOCK	76	I/O	DRAM_DATA[11]
33	PWR	VDD	77	GND	VSS
34	-	NC	78	I/O	DRAM_DATA[10]
35	GND	VSS	79	I/O	DRAM_DATA[9]
36	I	FEC_DATA[5]	80	I/O	DRAM_DATA[8]
37	I	FEC_DATA[4]	81	I/O	DRAM_DATA[7]
38	I	FEC_DATA[3]	82	PWR	VDD
39	I	FEC_DATA[2]	83	I/O	DRAM_DATA[6]
40	I	FEC_DATA[1]	84	I/O	DRAM_DATA[5]
41	I	FEC_DATA[0]	85	I/O	DRAM_DATA[4]
42	I	\ERR_BLOCK	86	I/O	DRAM_DATA[3]
43	I	D_VALID	87	GND	VSS
44	I	SCAN_MODE / TA[8]	88	I/O	DRAM_DATA[2]

Package Pin out *(continued)*

PIN	TYPE	NAME	PIN	TYPE	NAME
89	I/O	DRAM_DATA[1]	133	I	DSP_ADDR[22]
90	I/O	DRAM_DATA[0]	134	I	DSP_ADDR[21]
91	I	\DATA_WAIT	135	I	DSP_ADDR[20]
92	I	\DATA_REQ	136	I	DSP_ADDR[19]
93	I	\AUD_WAIT	137	I	DSP_ADDR[18]
94	I	\AUD_REQ	138	I	DSP_ADDR[17]
95	I	\VID_WAIT	139	I	DSP_ADDR[16]
96	I	\VID_REQ	140	I	DSP_ADDR[15]
97	I	BOF_D	141	I	DSP_ADDR[14]
98	I	BOF_A	142	I	DSP_ADDR[13]
99	I	BOF_V	143	I	DSP_ADDR[12]
100	PWR	VDD	144	I	DSP_ADDR[11]
101	O	APWM	145	I	DSP_ADDR[10]
102	GND	VSS	146	I	DSP_ADDR[9]
103	O	\AUD_DCS	147	I	DSP_ADDR[8]
104	O	AUD_SER_DATA	148	I	DSP_ADDR[7]
105	O	\AUD_STRB	149	I	DSP_ADDR[6]
106	GND	VSS	150	I	DSP_ADDR[5]
107	O	\DATA_DCS	151	I	DSP_ADDR[4]
108	O	\DATA_STRB	152	I	DSP_ADDR[3]
109	O	PTS_DTS_STRB	153	I	DSP_ADDR[2]
110	I/O	VAD_DATA[7]	154	I	DSP_ADDR[1]
111	O	SCAN_OUT1	155	I	DSP_ADDR [0]
112	I	\RESET	156	I	BIT8MODE
113	PWR	VDD	157	I	CLOCK
114	I/O	VAD_DATA[6]	158	PWR	VDD
115	I/O	VAD_DATA[5]	159	-	NC
116	I/O	VAD_DATA[4]	160	GND	VSS
117	I/O	VAD_DATA[3]	161	I/O	DSP_DATA[0]
118	GND	VSS	162	I/O	DSP_DATA[1]
119	I/O	VAD_DATA[2]	163	I/O	DSP_DATA[2]
120	I/O	VAD_DATA[1]	164	I/O	DSP_DATA[3]
121	PWR	VDD	165	PWR	VDD
122	I/O	VAD_DATA[0]	166	I/O	DSP_DATA[4]
123	O	\VID_DCS	167	I/O	DSP_DATA[5]
124	PWR	VDD	168	I/O	DSP_DATA[6]
125	O	\VID_STRB	169	I/O	DSP_DATA[7]
126	O	VPWM	170	GND	VSS
127	I	\DSP_STRB	171	I/O	DSP_DATA[8]
128	I	DSP_RWB	172	I/O	DSP_DATA[9]
129	I	\DSP_PD	173	I/O	DSP_DATA[10]
130	GND	VSS	174	I/O	DSP_DATA[11]
131	-	NC	175	PWR	VDD
132	-	NC	176	I/O	DSP_DATA[12]

8.2 Package Dimensions

Package Type : 176 Pin Thin Quad Flat Package
24x24 mm BODY, 1.4 mm THICK

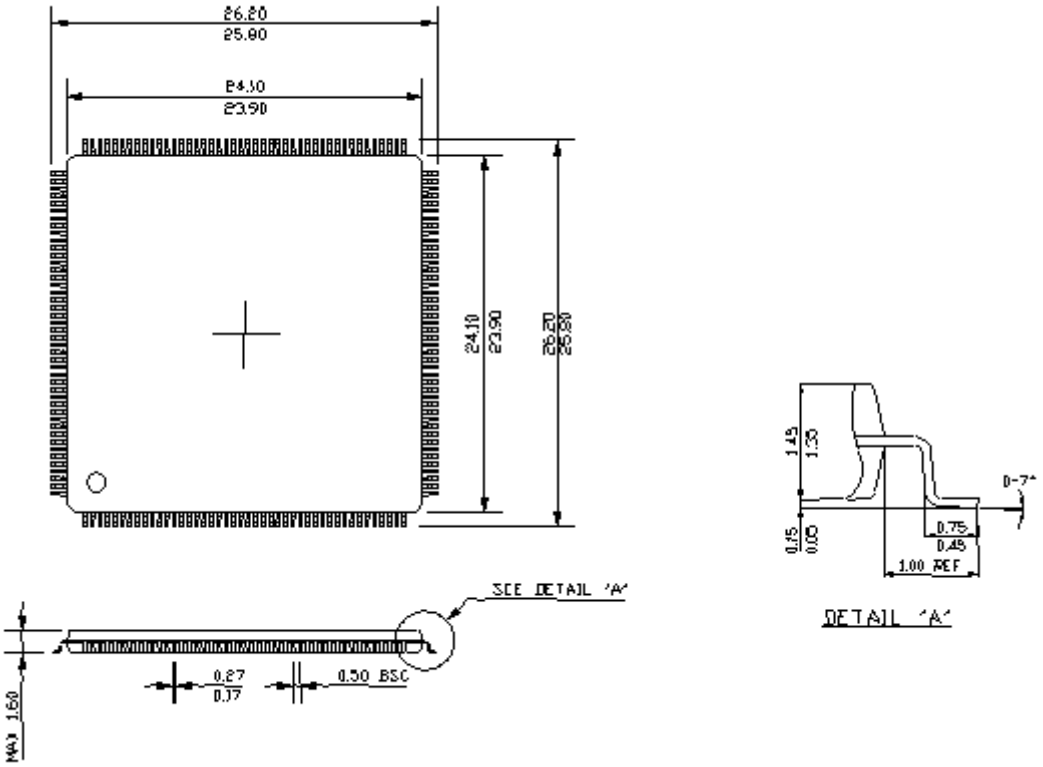


Figure 4. Physical Dimensions