HL14203

LCD Driver IC

Preliminary

2Q. 1999

Hyundai Electronics Industries

System IC Division

Contents

1. General Description

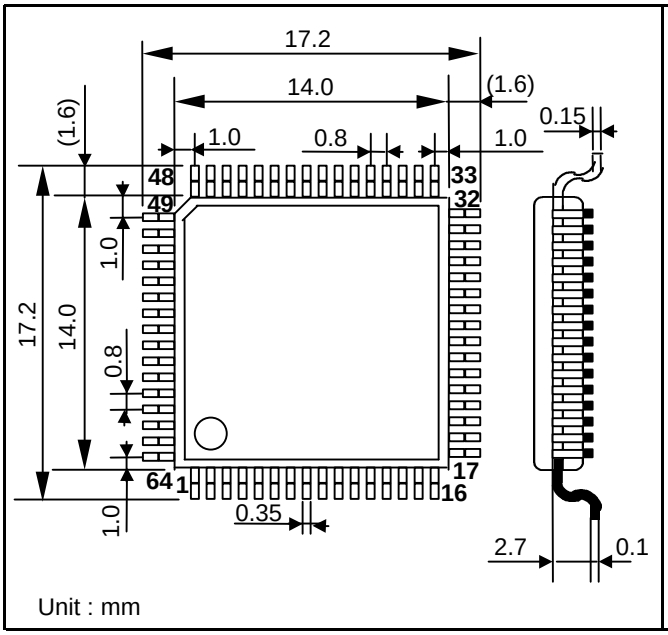
The HL14203 is 1/3 duty LCD display driver. It can drive directly maximum 126 segments. Also it has four general purpose output ports and a key scan function that accepts input from up to 30 keys.

2. Features

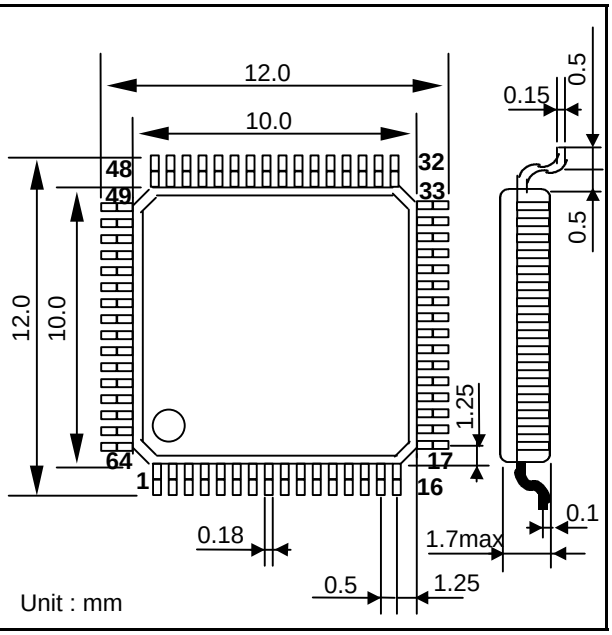
- LCD display ..... 42 segments x 3 commons
  1/3 duty - 1/2 bias
  1/3 duty - 1/3 bias
- Key scan ..... Maximum 30 keys
  Input 5 pins, Output 6 pins
- Power down mode ..... Sleep mode and all segments off mode
- Port
  Output ..... 4 pins
  (Including the LCD segment port)
- Serial I/O ..... Data transfer and receive
- Power on reset ..... Supply voltage detection (SVD)
- RC oscillator
- Package 64QFP

Package Dimensions

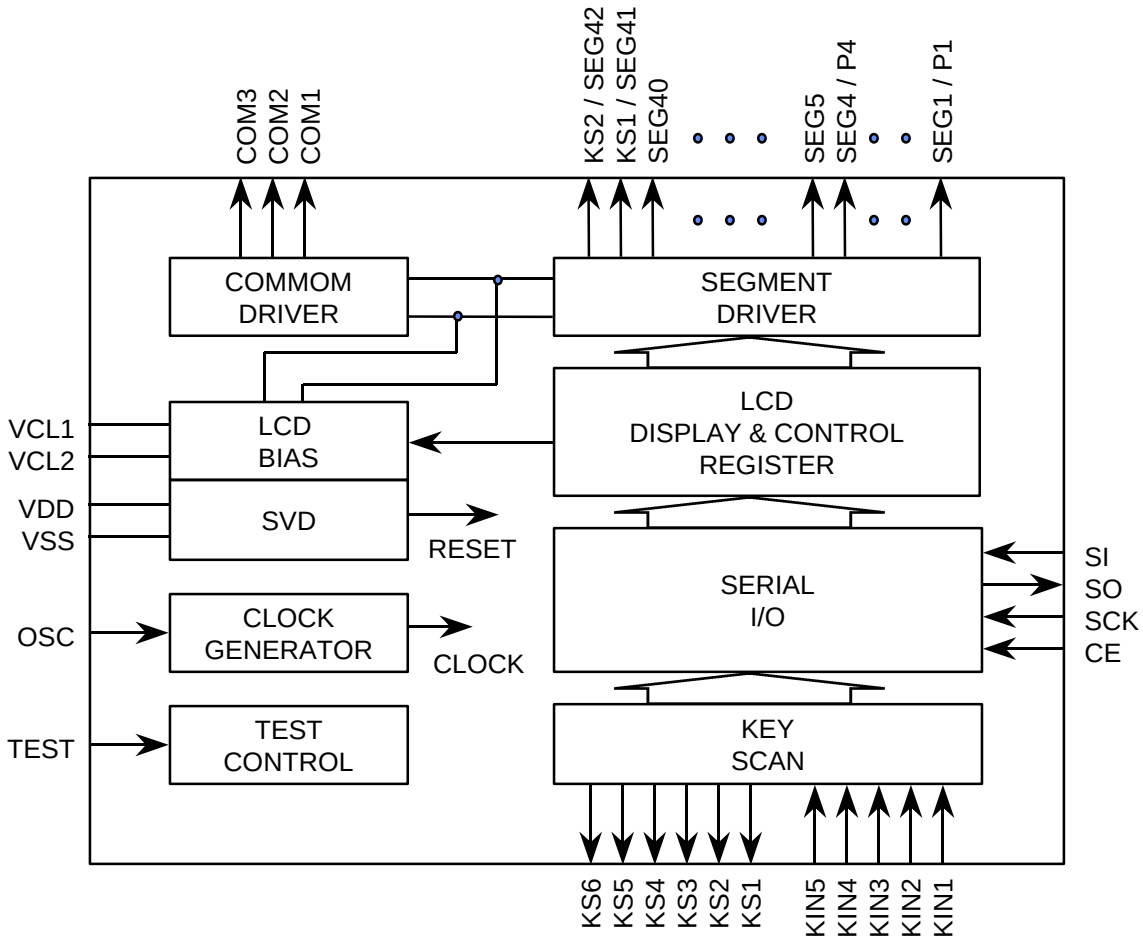
64QFP (14×14)



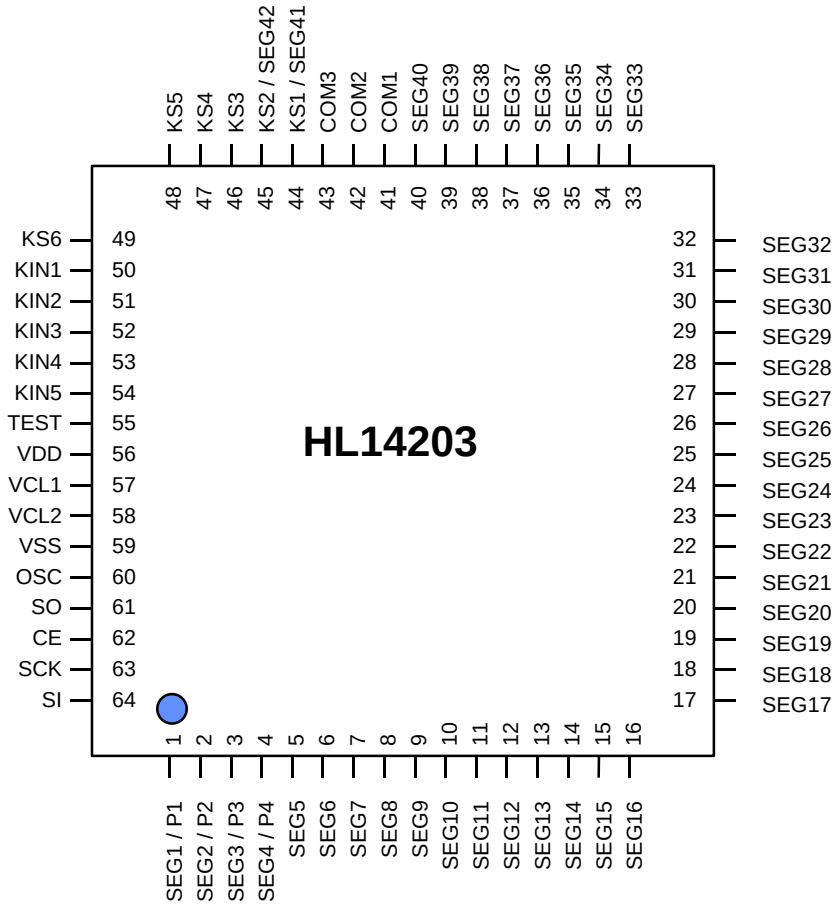
64QFP (10×10)



3. Block Diagram



4. Pin Diagram



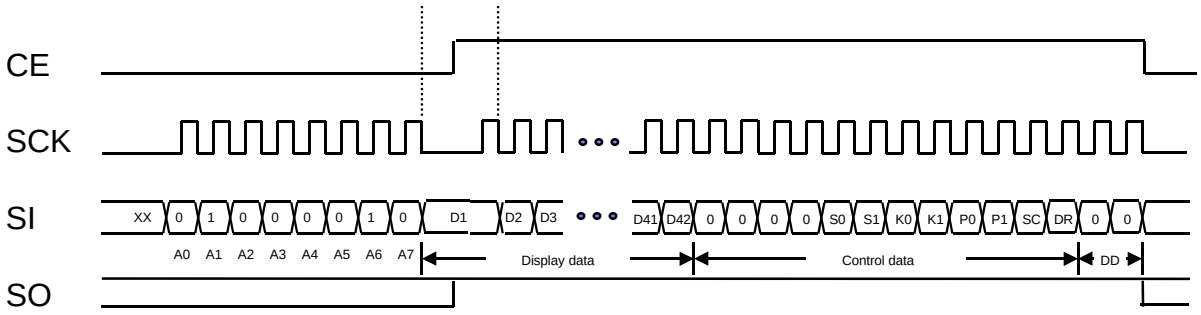
5. Pin Description

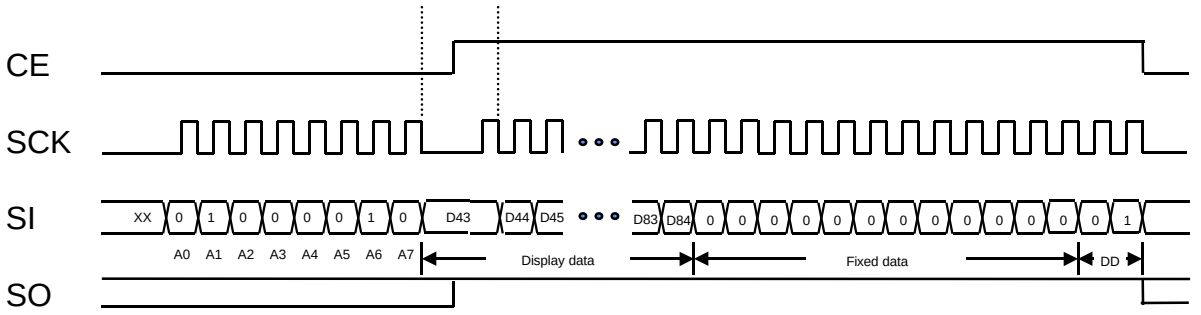
PIN Name	I/O	Pin Number	Contents
SEG[42:1]	O	42	LCD SEG Pins share P1,P2,P3 and P4
COM [3:1]	O	3	LCD Common Pins
VCL[2:1]	I	2	LCD Bias Pins
OSC	I/O	1	Oscillator Input Pin
KS[6:1]	O	6	Key Scan Output Pins
KIN[5:1]	I	5	Key Scan Input Pins
CE	I	1	Serial I/O Control Pin
SCK	I	1	Serial I/O Clock Pin
SO	O	1	Serial I/O Data Output Pin
SI	I	1	Serial I/O Data Input Pin
TEST	I	1	Test Pin. “1” Test mode , “0” Normal Mode
P[4:1]	O	4	Output Port share SEG[4:1]
VDD	I	1	Power Supply Pin
VSS	I	1	Ground Pin

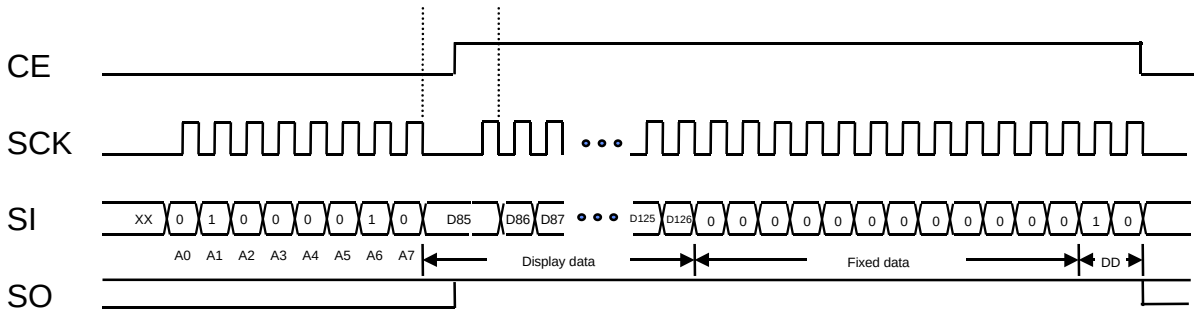
6. Serial I/O Data Format

1) Writing Mode

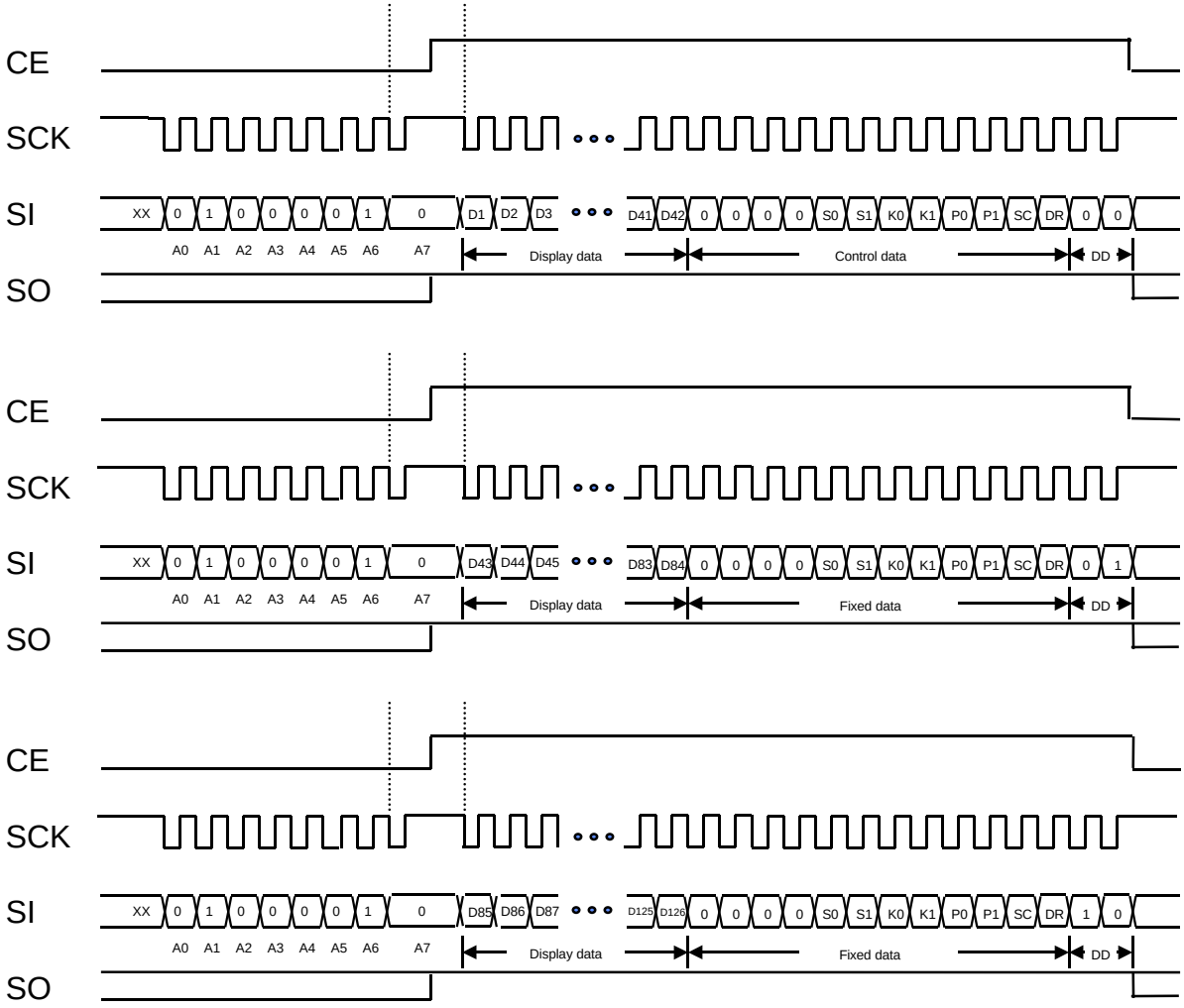
i)SCK is stopped at the low level







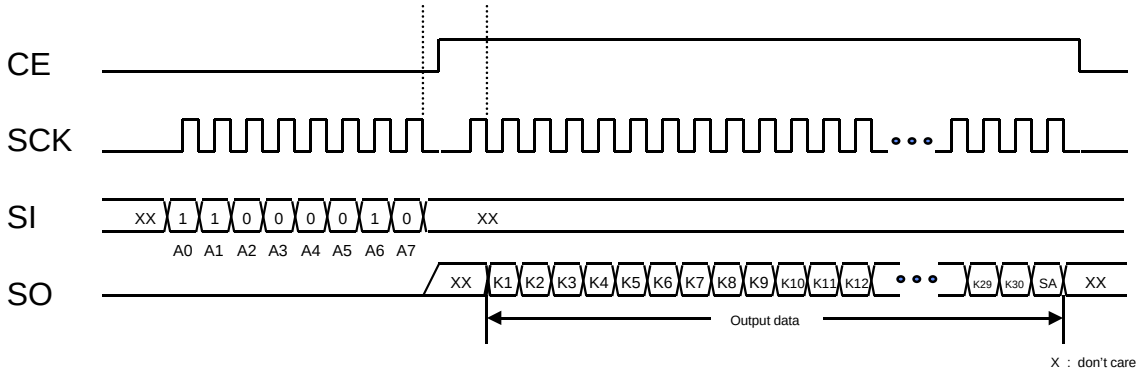
ii)SCK is stopped at the high level



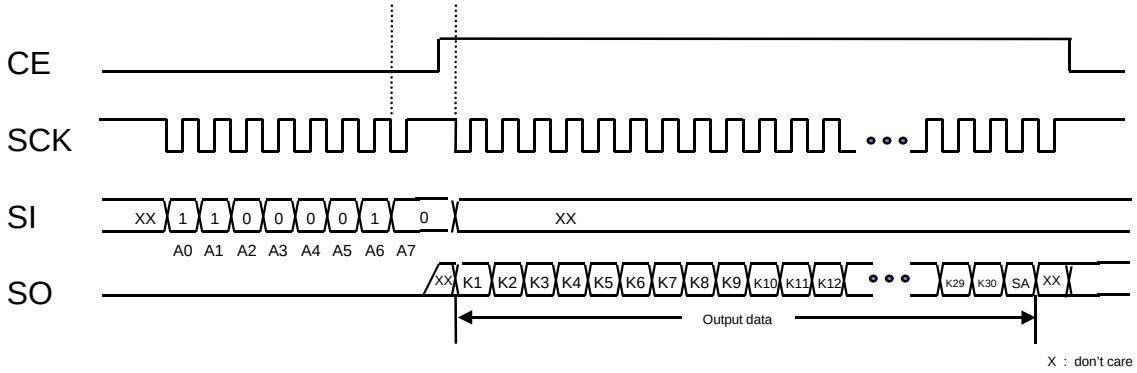
A7~A0 : 42H address
D126~D1 : Data of LCD display registers
S0, S1 : Sleep control data
K0, K1 : Key scan output / Segment output selection data
P0, P1 : Segment output / general-purpose output port selection data
SC : Segment on / off control data
DR : 1/2 bias or 1/3 bias drive selection data

2) Reading Mode

i) SCK is stopped at the low level



ii) SCK is stopped at the high level



A7 ~ A0 : 43H address
K30 ~ K1 : Key data
SA : Sleep acknowledge

7. Registers

1) Display Registers

Output Pin	COM1	COM2	COM3
SEG1	D1	D2	D3
SEG2	D4	D5	D6
SEG3	D7	D8	D9
SEG4	D10	D11	D12
SEG5	D13	D14	D15
SEG6	D16	D17	D18
SEG7	D19	D20	D21
SEG8	D22	D23	D24
SEG9	D25	D26	D27
SEG10	D28	D29	D30
SEG11	D31	D32	D33
SEG12	D34	D35	D36
SEG13	D37	D38	D39
SEG14	D40	D41	D42
SEG15	D43	D44	D45
SEG16	D46	D47	D48
SEG17	D49	D50	D51
SEG18	D52	D53	D54
SEG19	D55	D56	D57
SEG20	D58	D59	D60
SEG21	D61	D62	D63
SEG22	D64	D65	D66
SEG23	D67	D68	D69
SEG24	D70	D71	D72
SEG25	D73	D74	D75
SEG26	D76	D77	D78
SEG27	D79	D80	D81
SEG28	D82	D83	D84
SEG29	D85	D86	D87
SEG30	D88	D89	D90
SEG31	D91	D92	D93
SEG32	D94	D95	D96
SEG33	D97	D98	D99
SEG34	D100	D101	D102
SEG35	D103	D104	D105
SEG36	D106	D107	D108
SEG37	D109	D110	D111
SEG38	D112	D113	D114
SEG39	D115	D116	D117
SEG40	D118	D119	D120
SEG41	D121	D122	D123
SEG42	D124	D125	D126

2) Control Registers

Bias Selection Register

DR	Bias Selection
0	1/3 Bias
1	1/2 Bias

Key Scan / Segment output Selection Register

Control Data		Output Pin Status		Maximum number of Input Pins
K0	K1	KS1/SEG41	KS2/SEG42	
0	0	KS1	KS2	30
0	1	SEG41	KS2	25
1	X	SEG41	SEG42	20

Port Mode Register

Control Data		Output Pin Status			
P0	P1	SEG1/ P1	SEG2/ P2	SEG3/ P3	SEG4/ P4
0	0	SEG1	SEG2	SEG3	SEG4
0	1	P1	P2	SEG3	SEG4
1	0	P1	P2	P3	SEG4
1	1	P1	P2	P3	P4

Port Data Register

Output Pin	Port Data Register
SEG1 / P1	D1
SEG2 / P2	D4
SEG3 / P3	D7
SEG4 / P4	D10

Sleep Mode Control Register

Control Data		Mode	OSC Oscillator	SEG / COMMON Output	Output Pin Status					
S0	S1				KS1	KS2	KS3	KS4	KS5	KS6
0	0	Normal	Operating	Operating	H	H	H	H	H	H
0	1	Sleep	Stopped	L	L	L	L	L	L	H
1	0	Sleep	Stopped	L	L	L	L	L	H	H
1	1	Sleep	Stopped	L	H	H	H	H	H	H

Display On/Off Control Register

Control Data	Display Status
SC	SEG1 ~ SEG42
0	On
1	Off

Key Scan Data & Sleep Acknowledge Read

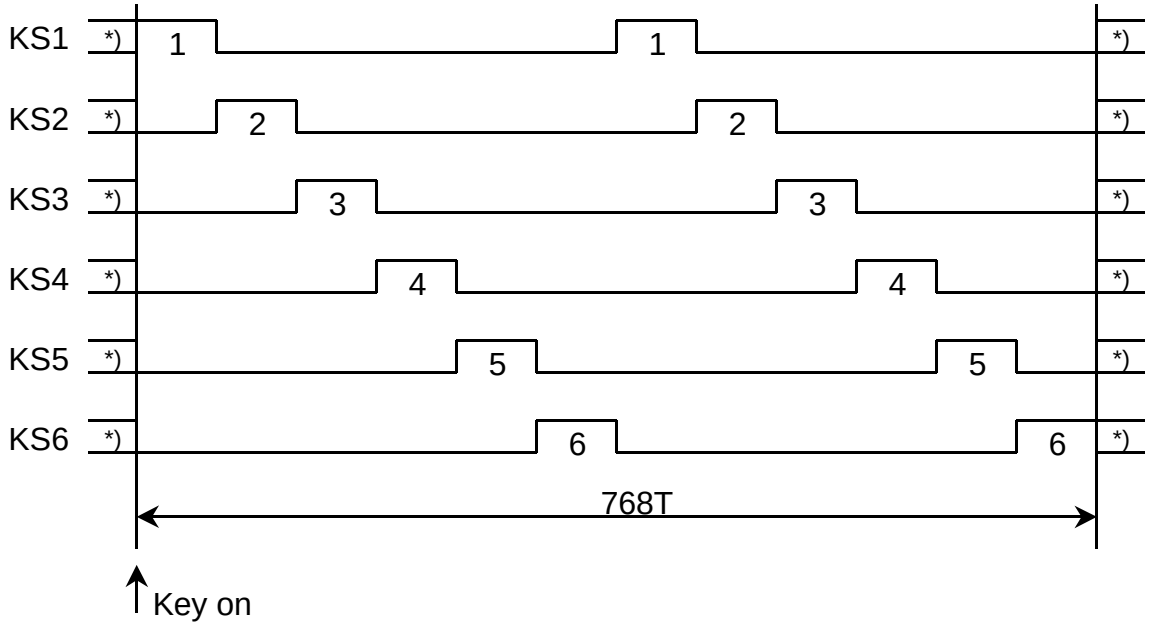
ADDRESS	Read Data
43H	K1 ~ K30, SA

	KIN1	KIN1	KIN1	KIN1	KIN1
KS1 / SEG41	K1	K2	K3	K4	K5
KS2 / SEG42	K6	K7	K8	K9	K10
KS3	K11	K12	K13	K14	K15
KS4	K16	K17	K18	K19	K20
KS5	K21	K22	K23	K24	K25
KS6	K26	K27	K28	K29	K30

8. Key Scan Function

1) Key Scan Timing

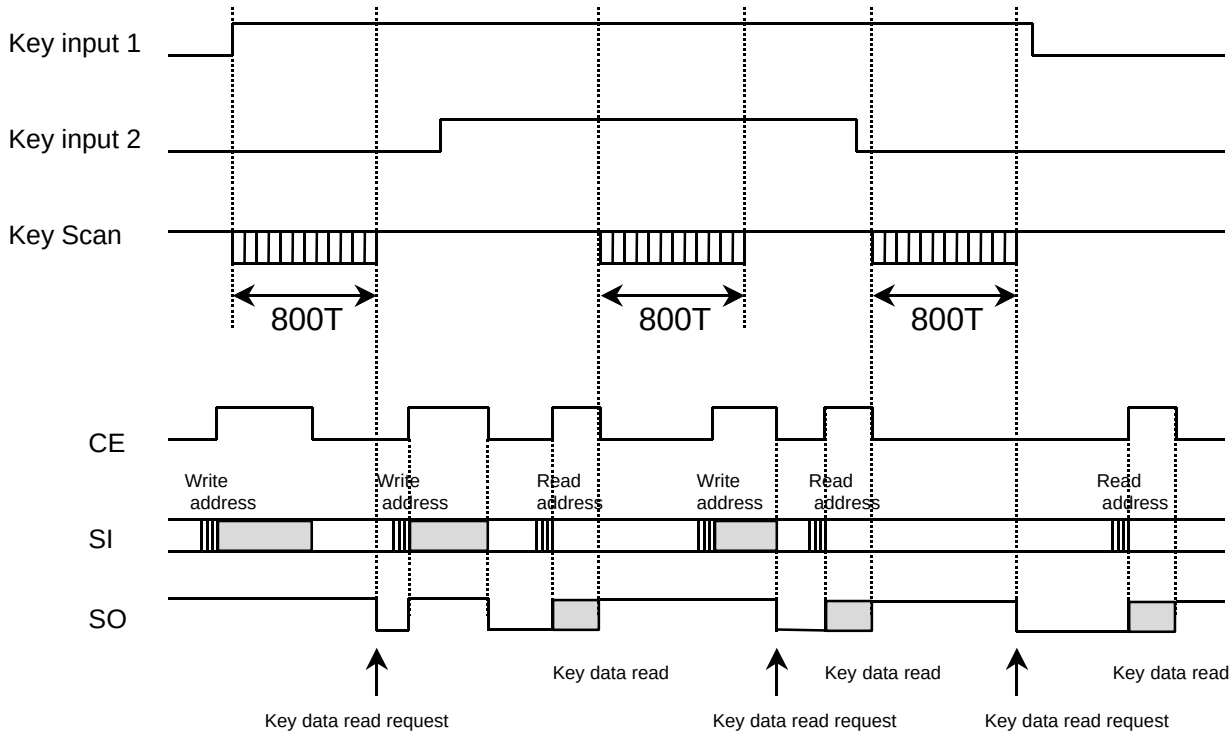
The key scan period is 384T. The HL14203 scans the key twice and determines that a key has been pressed when the key data agrees. It outputs a key data read request 800T after starting a key scan. If the key data does not agree and a key was pressed at that point, it scans the key again.Thus the HL14203 cannot detect a key press shorter than 800T.



*) In sleep mode the high / low state of these pins is determined by the S0,S1 bits in the control data. Key scan output signals are not output from pins that are set low.

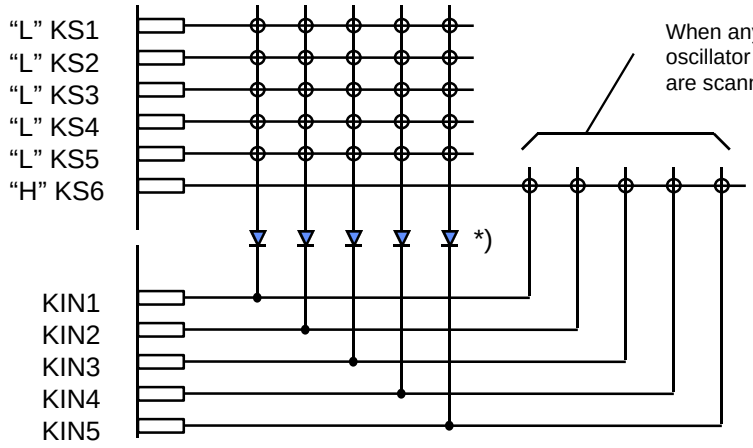
2) In normal mode

- The pins KS1 to KS6 are set high.
- When a key is pressed a key scan is started and the keys are scanned until all keys are released. Multiple key presses are recognized by determining whether multiple key data bits are set.
- If a key is pressed for longer than 800T (where T=1/fosc) the HL14203 outputs a key data read request (a low level on SO pin) to the controller. The controller acknowledges this request and reads the key data. However, if CE is high during a serial data transfer, SO will be set high.
- After the controller reads the key data, the key data read requests is cleared (SO pin is set high) and the HL14203 performs another key scan. Also note that SO pin, being an open-drain output, requires a pull-up resistor.

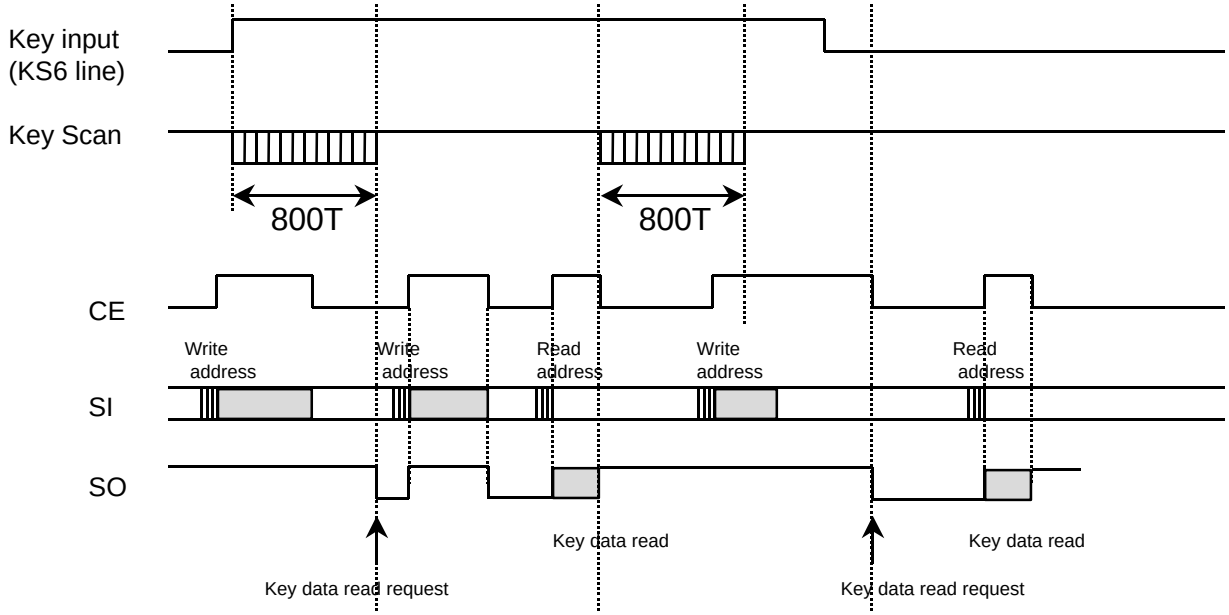


3) In sleep mode

- The pins KS1 to KS6 are set to high or low by the S0 and S1 bits in the sleep mode control register.
- If a key on one of the lines corresponding to a KS1 to KS6 pin which is set high is pressed, the oscillator on the OSC pin is started and a key scan is performed. Keys are scanned until all keys are released. Multiple key presses are recognized by determining whether multiple key data bits are set.
- If a key is pressed for longer than 800T (where T=1/fosc) the HL14203 outputs a key data read request (a low level on SO) to the controller. The controller acknowledges this request and reads the key data. However, if CE is high during a serial data transfer, SO will be set high.
- After the controller reads the key data, the key data read request is cleared (SO is set high) and the HL14203 performs another key scan. However this does not clear sleep mode. Also note that SO, being an open-drain output, requires a pull-up resistor (between 1 and 10 K).
- Sleep mode key scan example
  Example : S0 = 0, S1 = 1 (sleep with only KS6 high)



*) These diodes are required to reliable recognize multiple key presses on the KS6 line when sleep mode state with only KS6 high, as in the above example. That is, these diodes prevent incorrect operation due to sneak currents in the KS6 key scan output signal when keys on the KS1 to KS5 lines are pressed at the same time.

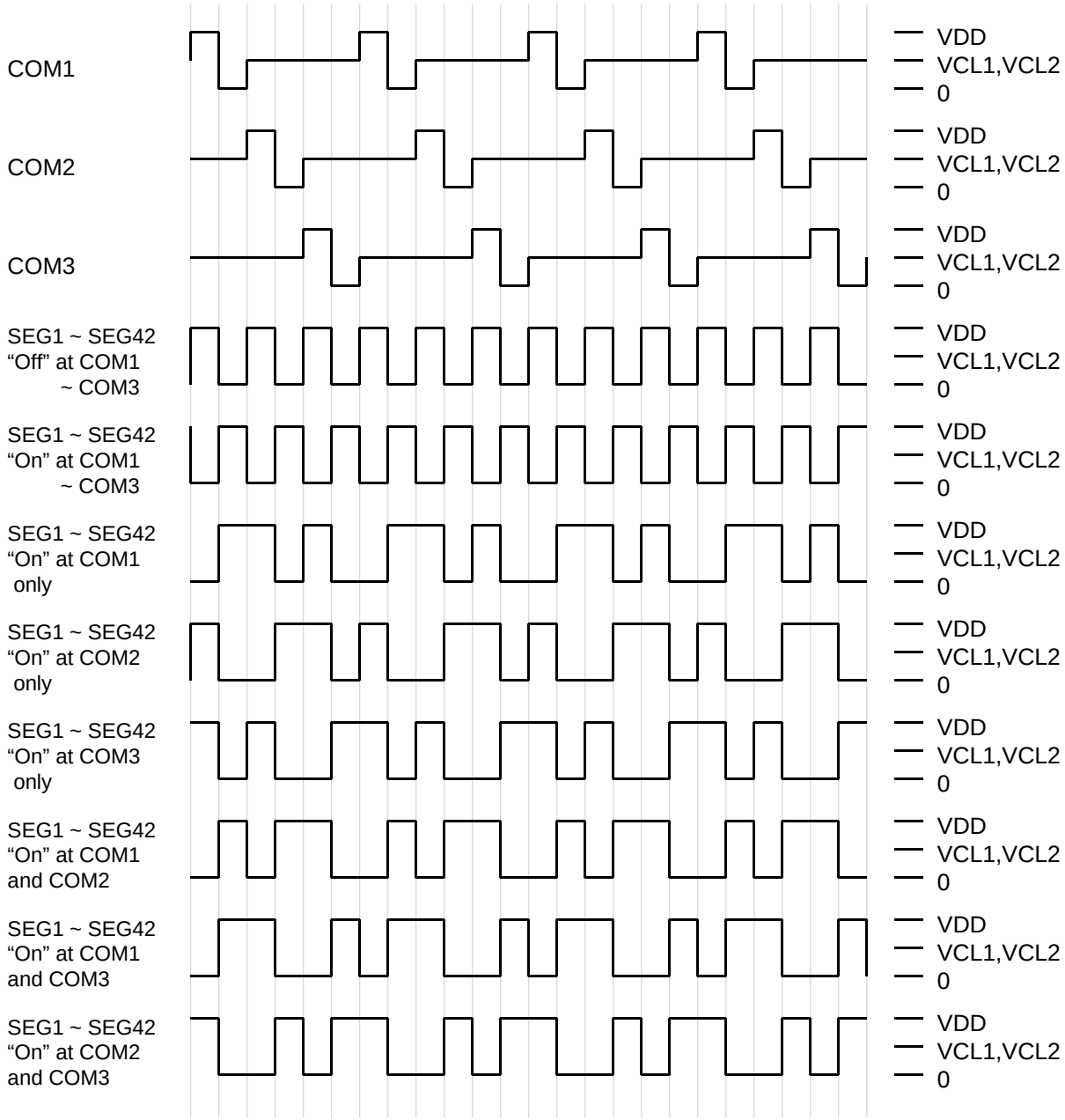


Multiple Key Presses

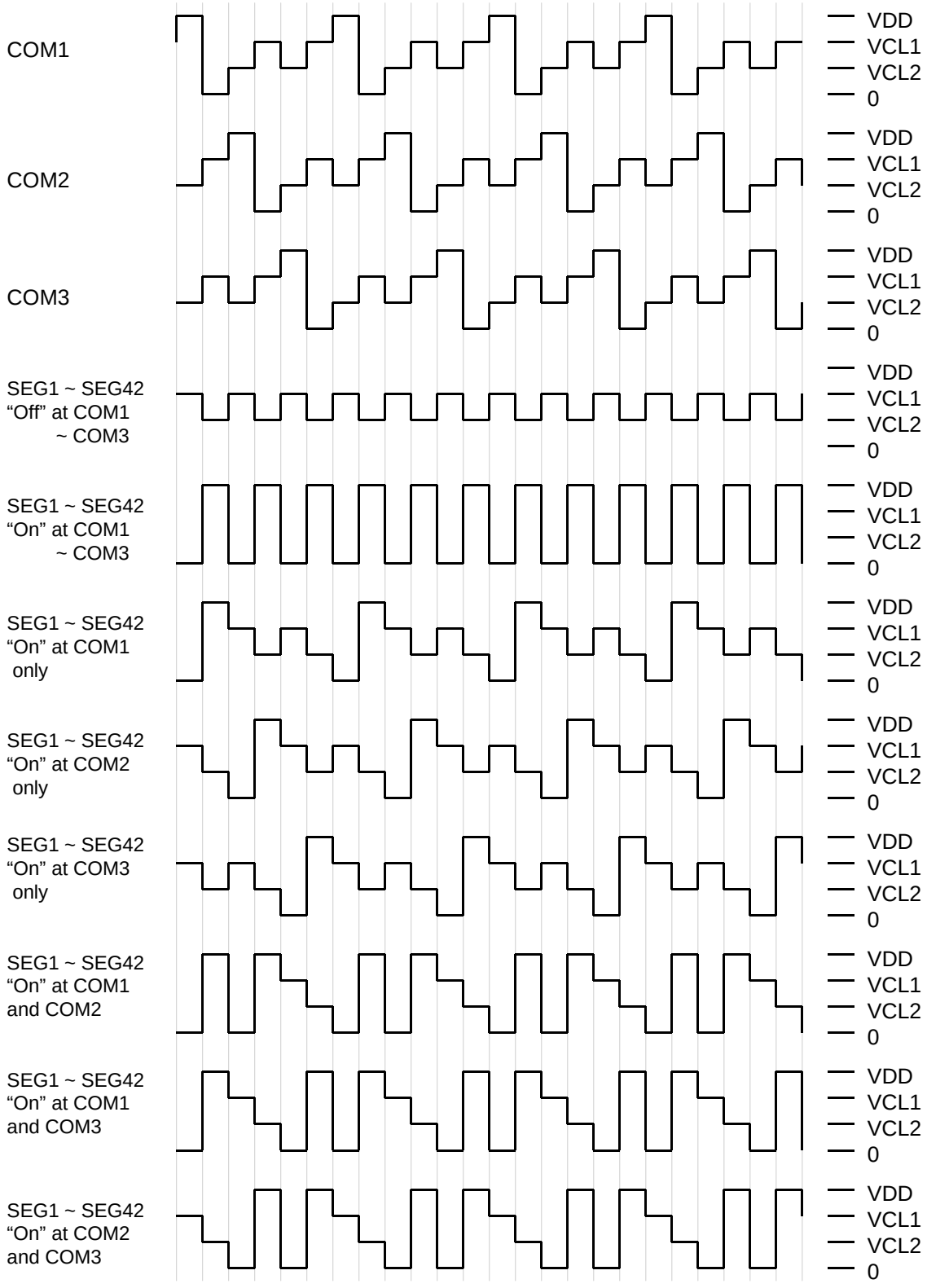
Although the HL14203 is capable of key scanning without inserting diodes for dual key presses, triple key presses on the KIN1 to KIN5 input pin lines, or multiple key presses on the KS1 to KS6 output pin lines, multiple presses other than these cases may result in keys that were not pressed recognized as having been pressed. Therefore, a diode must be inserted in series with each key. Application that do not recognize multiple key presses of threes or keys should check the key data for three or more 1 bits and ignore such data.

9. LCD Display Function

1) 1/3 Duty 1/2 Bias Waveforms



2) 1/3 Duty 1/3 Bias Waveforms



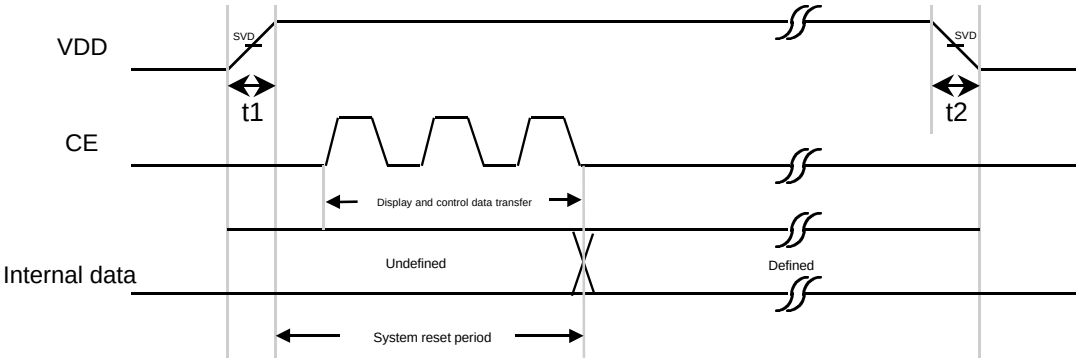
10. Power On Reset

1) Supply Voltage Detection (SVD)

The SVD generates an output signal and resets the system when power is first applied and when the voltage drops, I.e.,when the power supply voltage is less than or equal to the power down detection voltage, which is 2.5V, typical. To assure that this function operates reliably, a capacitor must be added to the power supply voltage Vdd rise time when power is first applied and the power supply voltage Vdd fall time when the voltage drops are both at least 1ms.

2) System Reset

If at least 1ms is assured as the supply voltage Vdd rise time when power is applied, a system reset will be applied by the SVD output signal when the supply voltage is brought up. If at least 1ms is assured as the supply voltage Vdd fall time when power drops, a system reset will be applied in the same manner by the SVD output signal when the supply voltage is lowered.



Power supply voltage Vdd rise time : t1 ≥ 1ms
Power supply voltage Vdd fall time : t2 ≥ 1ms

3) Internal block states during the reset period

- Clock generator
  Reset is applied and the base clock is stopped and OSC pin state is low.
- Common , segment drive and display data
  Reset is applied and the display is turned off but display data is not cleared.
- Key scan
  Reset is applied and all the key data is set to low.

4) Output pin states during the reset period

- SEG1/P1 to SEG4/P4 : Low *)
- SEG5 to SEG40 : Low
- COM1 to COM3 : Low
- KS1/SEG41, KS2/SEG42 : Low *)
- KS3 to KS5 : X
- KS6 : High
- SO : High

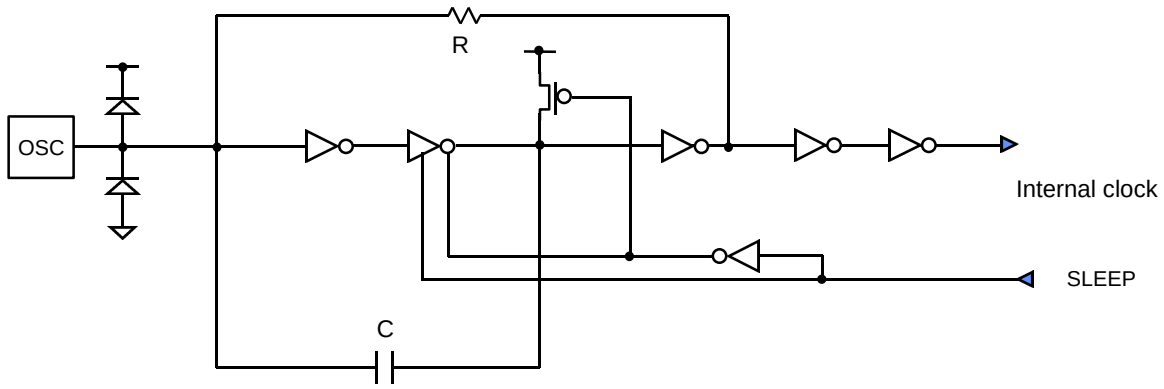
*) These output pins are forcibly set to the segment output function and held low.

11. Power Down Mode

Sleep mode is set up by setting S0 or S1 in the control data to 1. The segment outputs will all go low and the common outputs will also go low, and the oscillator on the OSC pin will stop (it will be started by a key press). This reduces power dissipation. This mode is cleared by sending control data with both S0 and S1 set to 0. Note that the SEG1/P1 to SEG4/P4 outputs can be used as general purpose output ports according to the state of the P0 and P1 control data bits, even in sleep mode.

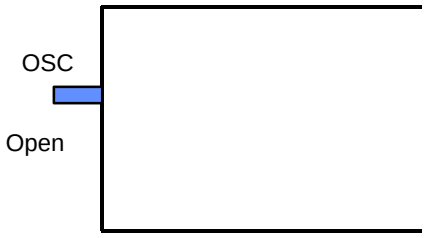
12. Oscillator Port

OSC Pin Diagram

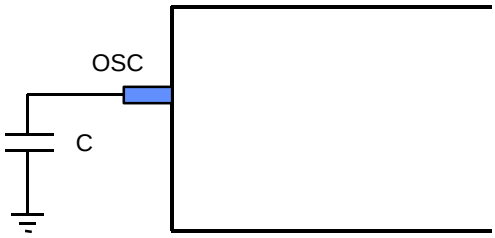


Oscillator circuit consists of internal R and C.

No Capacitor



Using Capacitor



HL14203 has internal resistor and capacitor, so it can be oscillation without external capacitor.
If you want to adjust the clock period then you can adjust it using external capacitor.

13. Electrical Characteristics

Absolute Maximum Rating at Ta=25¡ ÉVss = 0V

Parameter	Symbol	Condition	Rating	unit
Maximum supply voltage	VDD max	VDD	-0.3 to +7.0	V
Input voltage	Vin1	CE,SCK,SI	-0.3 to +7.0	V
	Vin2	OSC,KIN1 to KIN5, TEST,VCL1,2	-0.3 to VDD+0.3	V
Output voltage	Vout1	SO	-0.3 to +7.0	V
	Vout2	OSC, SEG1 to SEG42, COM1 to COM3, KS1 to KS6, P1 to P4	-0.3 to VDD+0.3	V
Output current	Iout1	SEG1 to SEG42	300	uA
	Iout2	COM1 to COM3	3	mA
	Iout3	KS1 to KS6	1	mA
	Iout4	P1 to P4	5	mA
Allowable power dissipation	Pd max	Ta = 85¡ É	200	mW
Operating temperature	Topr		-40 to +85	¡ É
Storage temperature	Tstg		-55 to +125	¡ É

Recommend operating ranges at Ta= -40¡ Ìto +85¡ ÉVss = 0V

Parameter	Symbol	Condition	min	typ	max	unit
Supply voltage	VDD	VDD	4.5		6.0	V
Input voltage	VCL1	VCL1		2/3VDD	VDD	V
	VCL2	VCL2		1/3VDD	VDD	V
Input high level voltage	VIH1	CE,SCK,SI	0.8VDD		6.0	V
	VIH2	KIN1 to KIN5	0.6VDD		VDD	V
Input low level voltage	VIL	CE,SCK,SI,KIN1 to KIN5	0		0.2VDD	V
Recommended external capacitance	COSC	OSC		TBD		pF
Guaranteed oscillation range	fOSC	OSC	TBD	38	TBD	KHz
Data setup time	tds	SCK,SI	160			ns
Data hold time	tdh	SCK,SI	160			ns
CE wait time	tcp	CE,SCK	160			ns
CE setup time	tcs	CE,SCK	160			ns
CE hold time	tch	CE,SCK	160			ns
High level clock pulse width	t0H	SCK	160			ns
Low level clock pulse width	toL	SCK	160			ns
Rise time	tr	CE,SCK,SI		160		ns
Fall time	tf	CE,SCK,SI		160		ns
SO output delay time	tdc	SO,RPU = 4.7kΩ, CL = 10pF*1			1.5	µs
SO rise time	tdr	SO,RPU = 4.7kΩ, CL = 10pF*1			1.5	µs

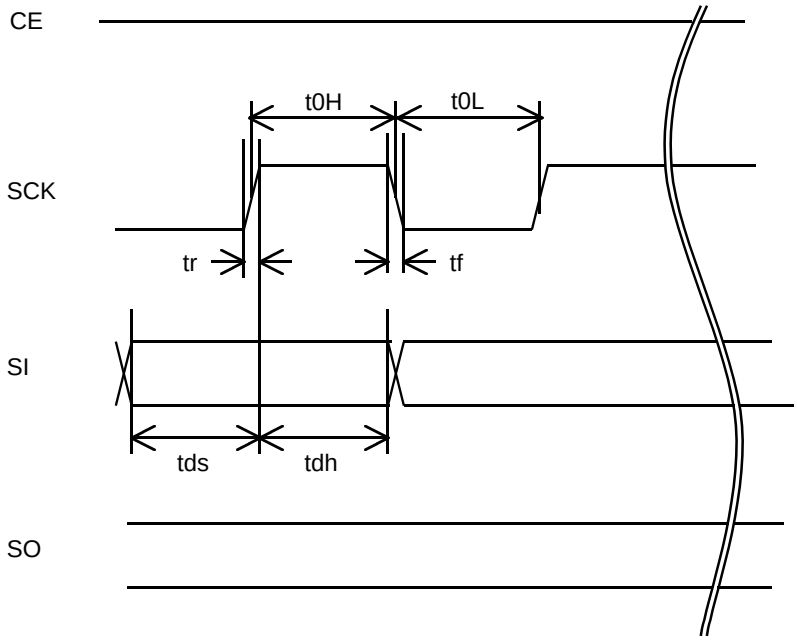
Note : *1.Since SO is an open-drain output, these values depend on the resistance of the pull-up resistor RPU and load capacitance CL .

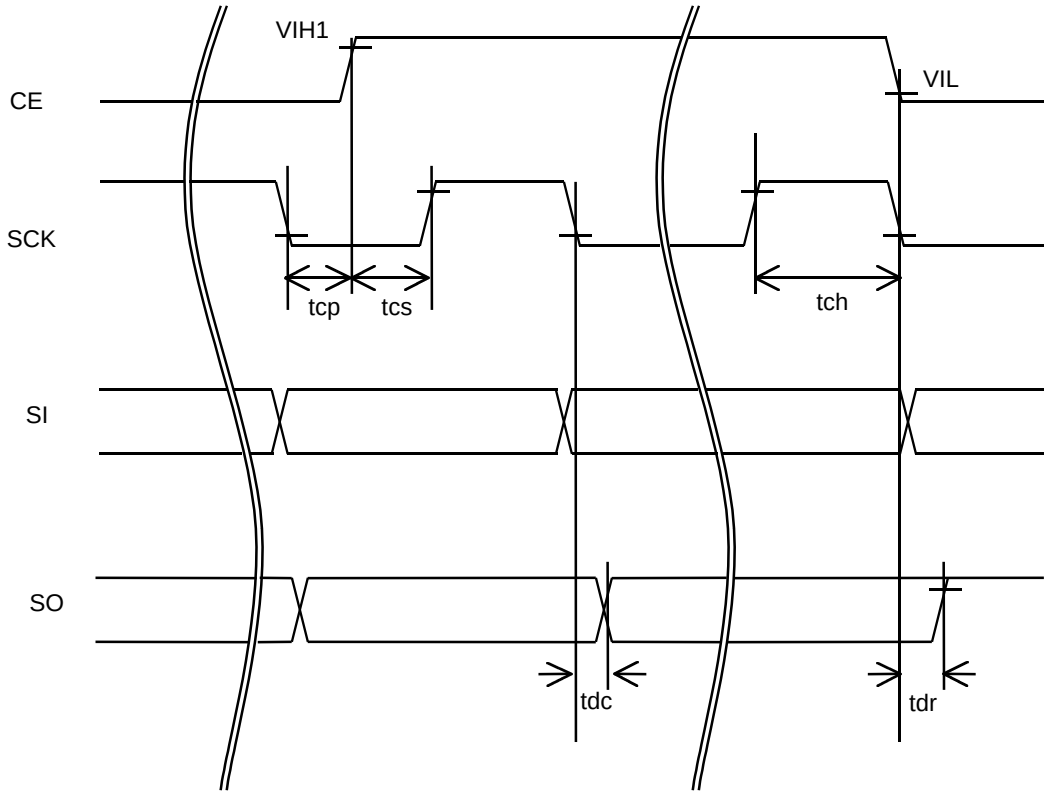
Electrical Characteristics for the Allowable Operating Ranges

Parameter	Symbol	Condition	min	typ	max	unit
Hysteresis	VH	CE,SCK,SI		O.1VDD		V
Supply voltage detection	SVD		TBD	2.5	TBD	V
Input high level current	IIH	CE,SCK,SI : V1 = 6.0V			5.0	µA
Input low level current	IIL	CE,SCK,SI : V1 = 0V	-5.0			µA
Input floating voltage	VIF	KIN1 to KIN5			0.05VDD	V
Pull-down resistance	RPD	KIN1 to KIN5 : VDD = 5.0V	50	100	250	kΩ
Output off leakage current	IOFFH	SO : VO = 6.0V			6.0	µA
Output high level voltage	VOH1	KS1 to KS6 : I0 = -500µA	VDD -1.2	VDD -0.5	VDD -0.2	V
	VOH2	P1 to P4 : I0 = -1mA	VDD -1.0			V
	VOH3	SEG1 to SEG42 : I0 = -20µA	VDD -1.0			V
	VOH4	COM1 to COM3 : I0= -100µA	VDD -1.0			V
Output low level voltage	VOL1	KS1 to KS6 : I0 = 25µA	0.2	0.5	1.5	V
	VOL2	P1 to P4 : I0 = 1mA			1.0	V
	VOL3	SEG1 to SEG42 : I0 = 20µA			1.0	V
	VOL4	COM1 to COM3 : I0 = 100µA			1.0	V
	VOL5	SO : I0 = 1 mA		0.1	0.5	V
Output middle level voltage*2	VMID1	COM to COM3 : 1/2 bias, Io = ¡ 100µA	1/2 VDD -1.0		1/2VDD +1.0	V
	VMID2	SEG1 to SEG42 : 1/3 bias, Io = ¡ 20µA	2/3VDD -1.0		2/3VDD +1.0	V
	VMID3	SEG1 to SEG42 : 1/3 bias, Io = ¡ 20µA	1/3VDD -1.0		1/3VDD +1.0	V
	VMID4	COM to COM3 : 1/3 bias, Io = ¡ 100µA	2/3VDD -1.0		2/3VDD +1.0	V
	VMID5	COM to COM3 : 1/3 bias, Io = ¡ 100µA	1/3VDD -1.0		1/3VDD +1.0	V
Oscillator frequency	fOSC	OSC : C = TBD	TBD	38	TBD	KHz
Current drain	IDD1	Sleep mode			100	µA
	IDD2	VDD = 6.0V, output open, 1/2 bias,fOSC = 38 KHz		350	700	µA
	IDD3	VDD = 6.0V, output open, 1/3 bias,fOSC = 38 KHz		300	600	µA

Note : *2. Excluding the bias voltage generation divider resistor built into VCL1 and VCL2

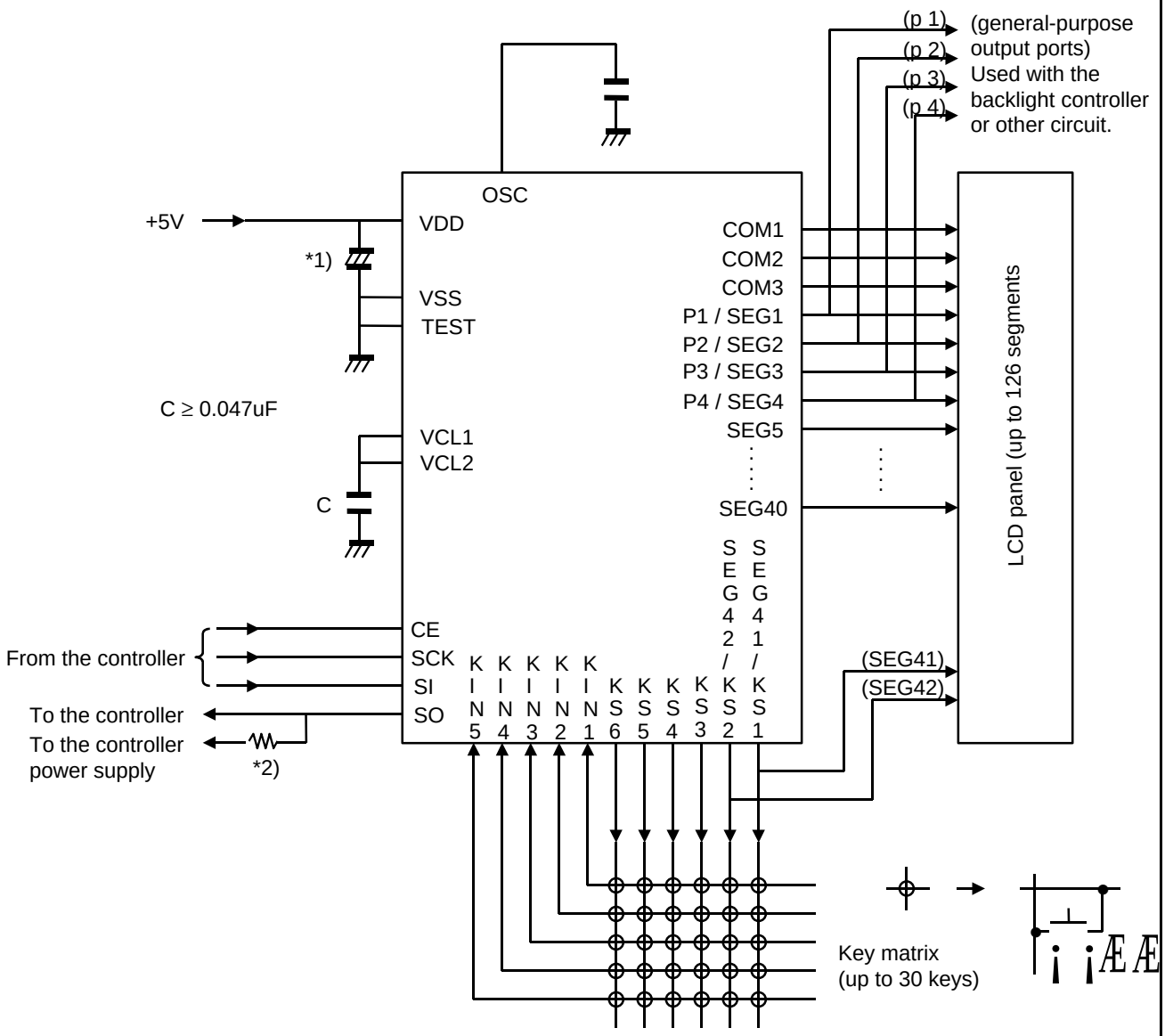
Timing diagram of SIO





14. Application

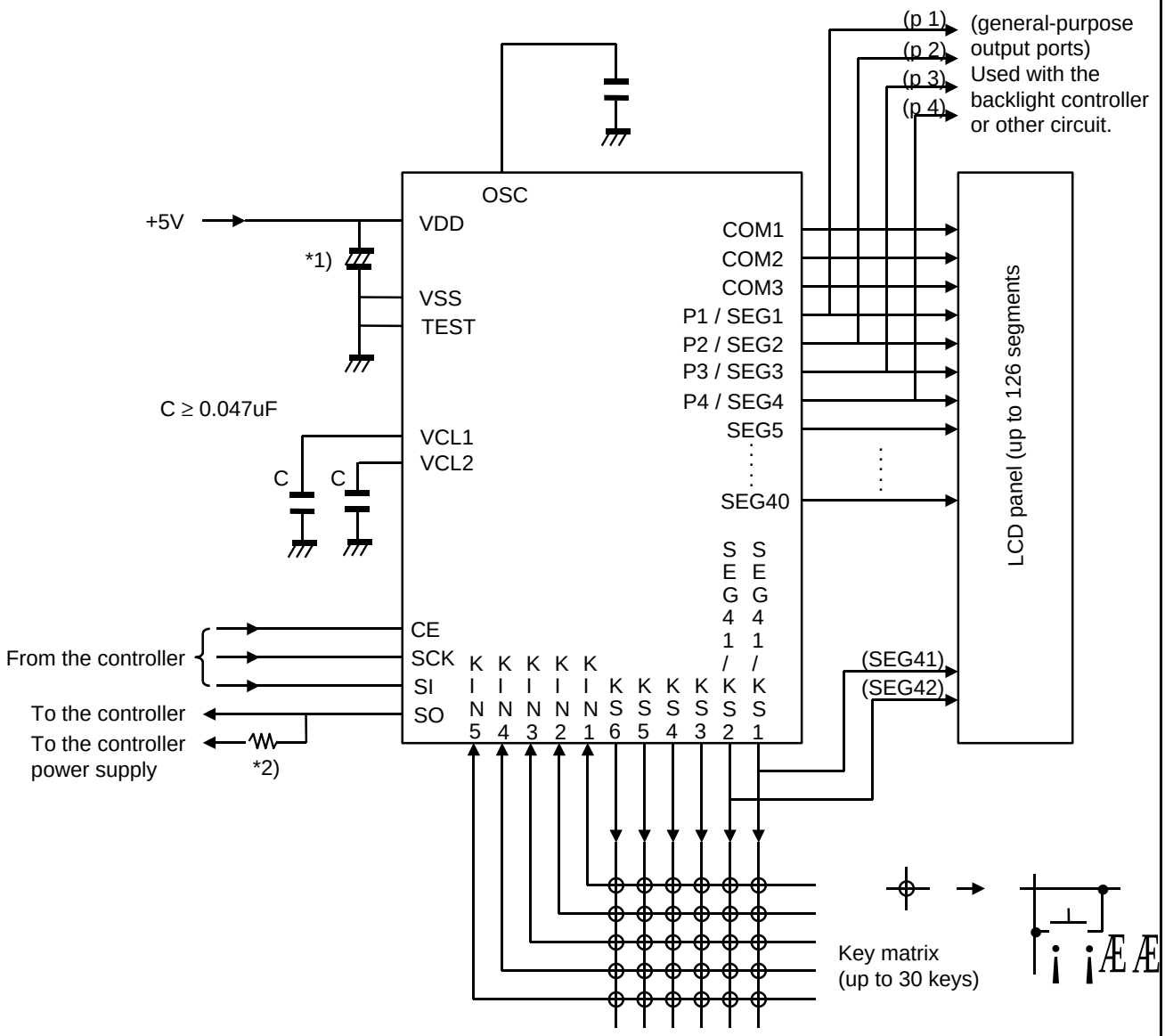
1/2 bias (for use with normal panels)



Note : *1). Add a capacitor to the power supply line so that the power supply voltage VDD rise time when power is applied and the power supply voltage VDD fall time when power drops are both at least 1 ms, as the HL14203 is reset by the SVD.

*2). The SO pin, being an open-drain output, requires a pull-up resistor, Select a resistance (between 1 to 10kΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.

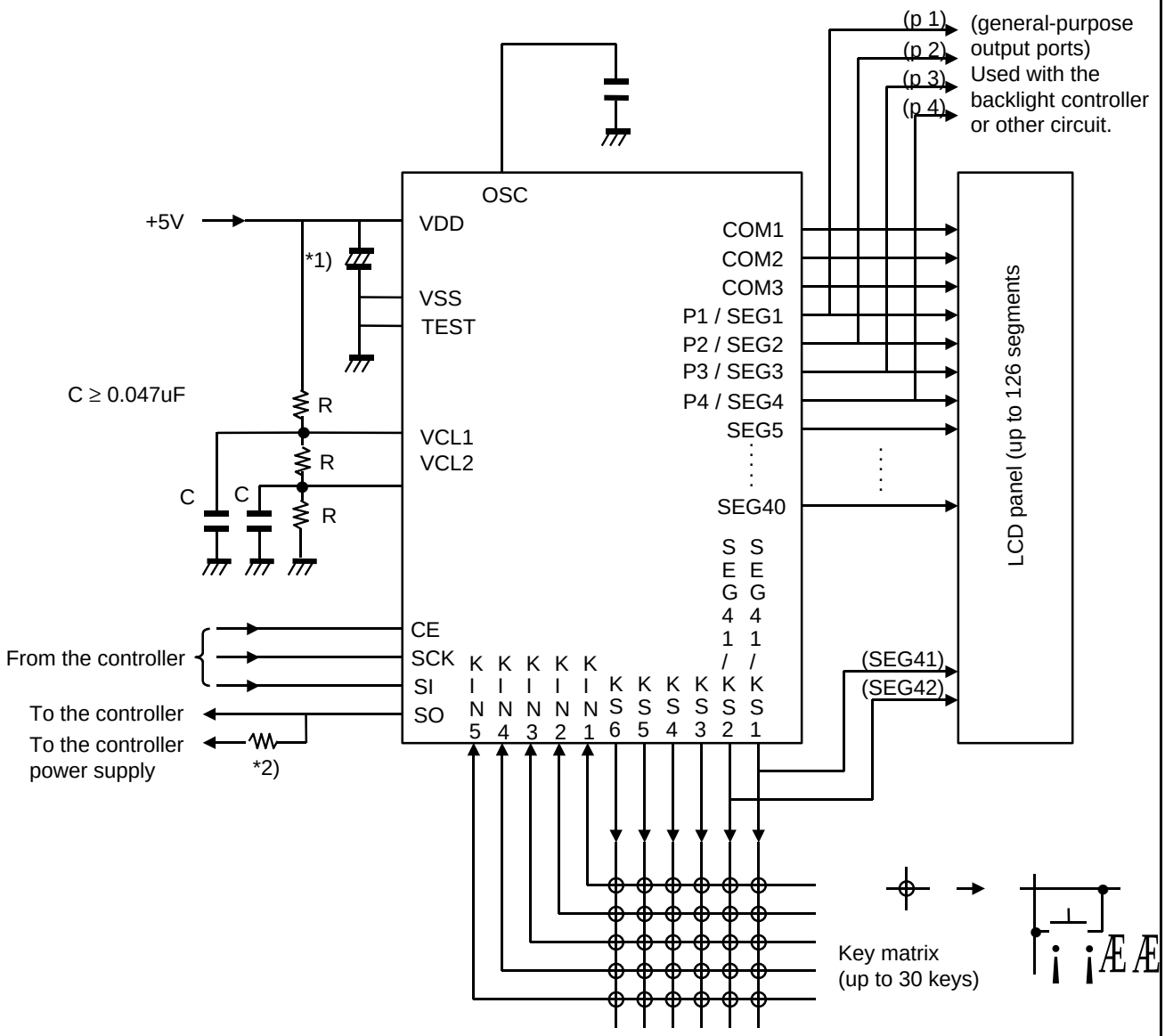
1/3 bias (for use with normal panels)



Note : *1). Add a capacitor to the power supply line so that the power supply voltage VDD rise time when power is applied and the power supply voltage VDD fall time when power drops are both at least 1 ms, as the HL14203 is reset by the SVD.

*2). The SO pin, being an open-drain output, requires a pull-up resistor, Select a resistance (between 1 to 10kΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.

1/3 bias (for use with large panels)



Note : *1). Add a capacitor to the power supply line so that the power supply voltage VDD rise time when power is applied and the power supply voltage VDD fall time when power drops are both at least 1 ms, as the HL14203 is reset by the SVD.

*2). The SO pin, being an open-drain output, requires a pull-up resistor, Select a resistance (between 1 to 10kΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.