HYUNDAI SEMICONDUCTOR HY6264

8K×8-Bit CMOS SRAM

M221201B-MAY92

T-46-23-12

DESCRIPTION

The HY6264 is a high speed, low power 8,192 words by 8-bit CMOS static RAM fabricated using high performance CMOS process technology. This high reliability process coupled with innovative circuit design techniques, yields maximum access time of 70ns.

The HY6264 has a data retention mode that guarantees data to remain valid at a minimum power supply voltage of 2.0 volt.

Using CMOS technology, supply voltages from 2.0 to 5.5 volts have little effect on supply current in data retention mode. Reducing the supply voltage to minimize current drain is unnecessary with the HY6264 family.

FEATURES

- High speed – 70/85/100/120/150ns (max.)
- Low power consumption
  - 200 mW typical operating
  - 10 μW typical standby (L-version)
- Battery back up (L-version)
  - 2 volt data retention
- Fully static operation
  - No clock or refresh required
- All inputs and outputs directly TTL compatible
- Tri-state output
- High reliability 28-pin 600 mil P-DIP and 330 mil SOP

		HY6264-70	HY6264-85	HY6264-10	HY6264-12	HY6264-15
Maximum Access Time (ns)		70	85	100	120	150
Maximum Operating Current (mA)		70	70	70	70	70
Maximum Standby Current (mA)		2	2	2	2	2
	L	0.1	0.1	0.1	0.1	0.1

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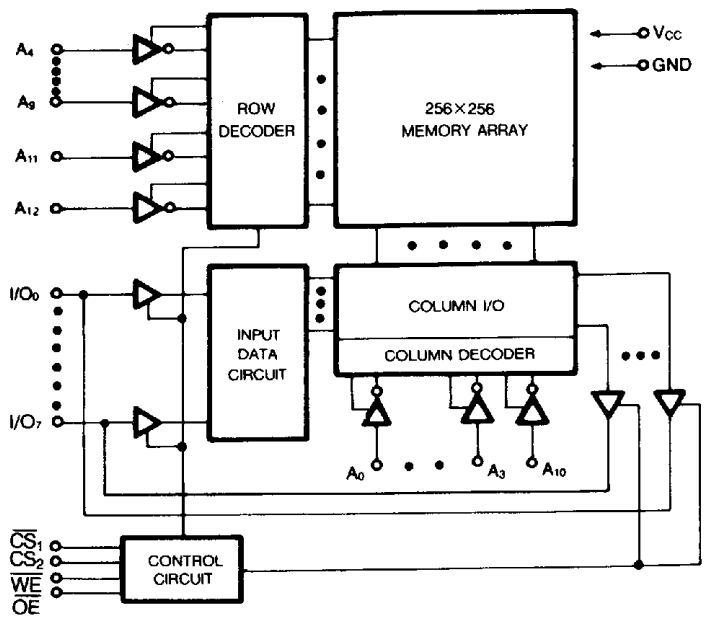
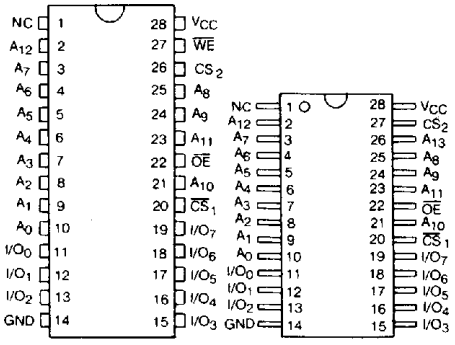
BLOCK DIAGRAM



PIN CONNECTIONS



DIP SOP

PIN NAMES

A_0-A_{12}	ADDRESS INPUT
I/O_0-I/O_7	DATA INPUT/OUTPUT
$\overline{CS_1}$	CHIP SELECT ONE
CS_2	CHIP SELECT TWO
$\overline{WE}$	WRITE ENABLE
$\overline{OE}$	OUTPUT ENABLE
V_{CC}	POWER
GND	GROUND

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ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}, V_{IN}, $V_{I/O}$	Power Supply, Input, Input/Output Voltage	−0.5[2] to 7.0	V
T_{BIAS}	Temperature Under Bias	−10 to 125	°C
T_{STG}	Storage Temperature	−65 to 150	°C
P_D	Power Dissipation	1.0	W
I_{OUT}	Data Output Current	50	mA

NOTES :
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. −3.5V for 20ns pulse.

RECOMMENDED DC OPERATING CONDITIONS
(T_A=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	3.5	6.0	V
V_{IL}	Input Low Voltage	−0.5	0	0.8	V

TRUTH TABLE

MODE	$\overline{WE}$	$\overline{CS_1}$	CS_2	$\overline{OE}$	I/O OPERATION	V_{CC} CURRENT	NOTE
Not Selected (Power Down)	X	H	X	X	High-Z	I_{SB}, I_{SB1}	
	X	X	L	X	High-Z	I_{SB}, I_{SB2}	
Output Disabled	H	L	H	H	High-Z	I_{CC}, I_{CC1}	
Read	H	L	H	L	D_{OUT}	I_{CC}, I_{CC1}	
Write	L	L	H	H	D_{IN}	I_{CC}, I_{CC1}	Write Cycle 1
	L	L	H	L	D_{IN}	I_{CC}, I_{CC1}	Write Cycle 2

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DC CHARACTERISTICS

(V_{CC}=5V± 10%, T_A=0°C to 70°C)

SYMBOL	PARAMETER	TEST CONDITIONS		HY6264 MIN.	HY6264 TYP.(1)	HY6264 MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{IN}=GND to V_{CC}		–	–	2	μA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS_1}$=V_{IH}, CS_2=V_{IL} or $\overline{OE}$=V_{IH}, $V_{I/O}$=GND to V_{CC}		–	–	2	μA
I_{CC}	Operating Power Supply Current	$\overline{CS_1}$=V_{IL}, CS_2=V_{IH}, $I_{I/O}$=0mA		–	30	50	mA
I_{CC1}	Average Operating Current	Min. Duty Cycle=100%, $\overline{CS_1}$=V_{IL}, CS_2=V_{IH}		–	40	70	mA
I_{SB}	Standby Power Supply Current	$\overline{CS_1}$=V_{IH} or CS_2=V_{IL}		–	1	3	mA
I_{SB1}(2)		$\overline{CS_1}$≥V_{CC}−0.2V, CS_2≤ 0.2V or ≥ V_{CC}−0.2V		–	20	2000	μA
			L	–	2	100	
I_{SB2}(2)		$\overline{CS_1}$≤0.2V or ≥V_{CC}−0.2V, CS_2≤0.2V		–	20	2000	μA
			L	–	2	100	
V_{OL}	Output Low Voltage	I_{OL}=2.1mA		–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH}=−1.0mA		2.4	–	–	V

NOTES :
1. Typical limits are at V_{CC}=5.0V, T_A=25°C and specified loading
2. V_{IL} min=−0.5V

AC CHARACTERISTICS

(V_{CC}=5V± 10%, T_A= 0°C to 70°C)

READ CYCLE

SYMBOL	PARAMETER		HY6264-70 MIN.	HY6264-70 MAX.	HY6264-85 MIN.	HY6264-85 MAX.	HY6264-10 MIN.	HY6264-10 MAX.	HY6264-12 MIN.	HY6264-12 MAX.	HY6264-15 MIN.	HY6264-15 MAX.	UNIT
t_{RC}	Read Cycle Time		70	–	85	–	100	–	120	–	150	–	ns
t_{AA}	Address Access Time		–	70	–	85	–	100	–	120	–	150	ns
t_{ACS1}	Chip Select Access Time	$\overline{CS_1}$	–	70	–	85	–	100	–	120	–	150	ns
t_{ACS2}		CS_2	–	70	–	85	–	100	–	120	–	150	ns
t_{OE}	Output Enable to Output Valid		–	45	–	50	–	55	–	60	–	70	ns
t_{CLZ1}	Chip Select to Output in Low-Z	$\overline{CS_1}$	10	–	10	–	10	–	10	–	15	–	ns
t_{CLZ2}		CS_2	10	–	10	–	10	–	10	–	15	–	ns
t_{OLZ}	Output Enable to Output in Low-Z		5	–	5	–	5	–	5	–	5	–	ns
t_{CHZ1}	Chip Deselect to Output in High-Z	$\overline{CS_1}$	0	30	0	35	0	35	0	40	0	50	ns
t_{CHZ2}		CS_2	0	30	0	35	0	35	0	40	0	50	ns
t_{OHZ}	Output Disable to Output in High-Z		0	30	0	35	0	35	0	40	0	50	ns
t_{OH}	Output Hold from Address Change		10	–	10	–	10	–	10	–	15	–	ns

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WRITE CYCLE

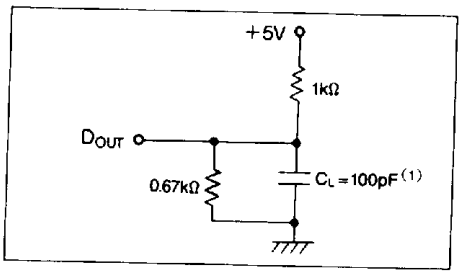
SYMBOL	PARAMETER		HY6264-70		HY6264-85		HY6264-10		HY6264-12		HY6264-15		UNIT
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time		70	–	85	–	100	–	120	–	150	–	ns
t_{CW}	Chip Select to End of Write		55	–	60	–	70	–	85	–	100	–	ns
t_{AS}	Address Setup Time		0	–	0	–	0	–	0	–	0	–	ns
t_{AW}	Address Valid to End of Write		60	–	70	–	80	–	85	–	100	–	ns
t_{WP}	Write Pulse Width		50	–	55	–	60	–	70	–	90	–	ns
t_{WR1}	Write Recovery Time	$\overline{CS_1}$,$\overline{WE}$	5	–	5	–	5	–	10	–	10	–	ns
t_{WR2}		CS_2	5	–	10	–	10	–	15	–	15	–	ns
t_{WHZ}	Write to Output in High-Z		0	30	0	35	0	35	0	40	0	50	ns
t_{DW}	Data to Write Time Overlap		30	–	35	–	40	–	50	–	60	–	ns
t_{DH}	Data Hold from Write Time		0	–	0	–	0	–	0	–	0	–	ns
t_{OHZ}	Output Enable to Output in High-Z		0	30	0	35	0	35	0	40	0	50	ns
t_{OW}	Output Active from End of Write		5	–	5	–	5	–	5	–	10	–	ns

AC TEST CONDITIONS

(T_A=0°C to 70°C)

Input Pulse Level	0.8V to 2.4V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Level	1.5V

OUTPUT LOAD



NOTE :
1. Including scope and the jig

CAPACITANCE(1)

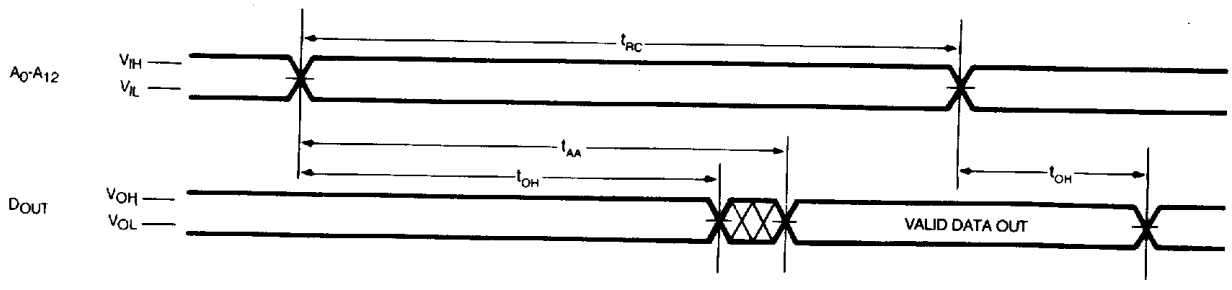
(T_A=25°C, f=1.0MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$=0V	8	pF

NOTE :
1. This parameter is sampled and not 100% tested.

TIMING DIAGRAMS

READ CYCLE 1(1,2,4)



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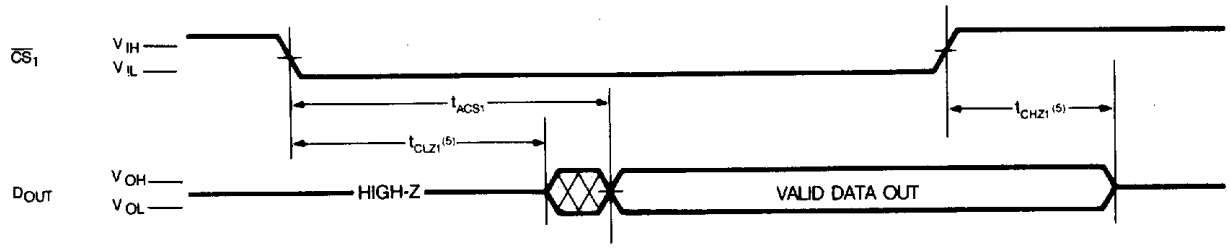
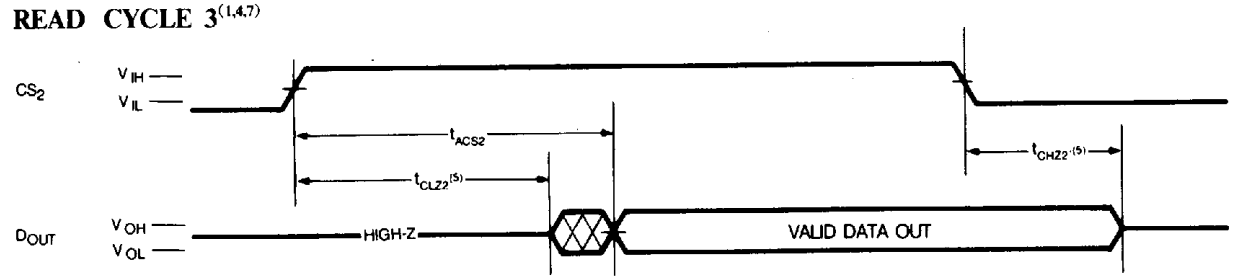
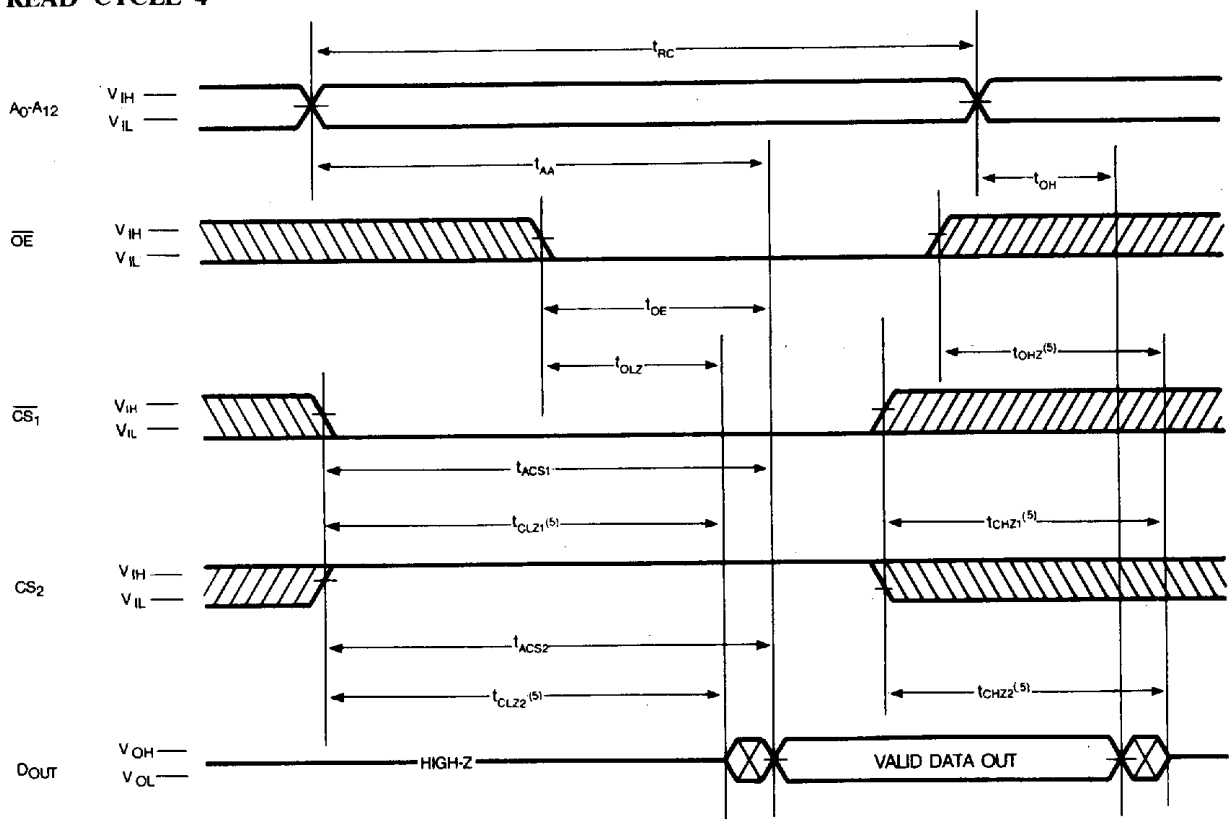
READ CYCLE 2[1,3,4,6]



READ CYCLE 3[1,4,7]

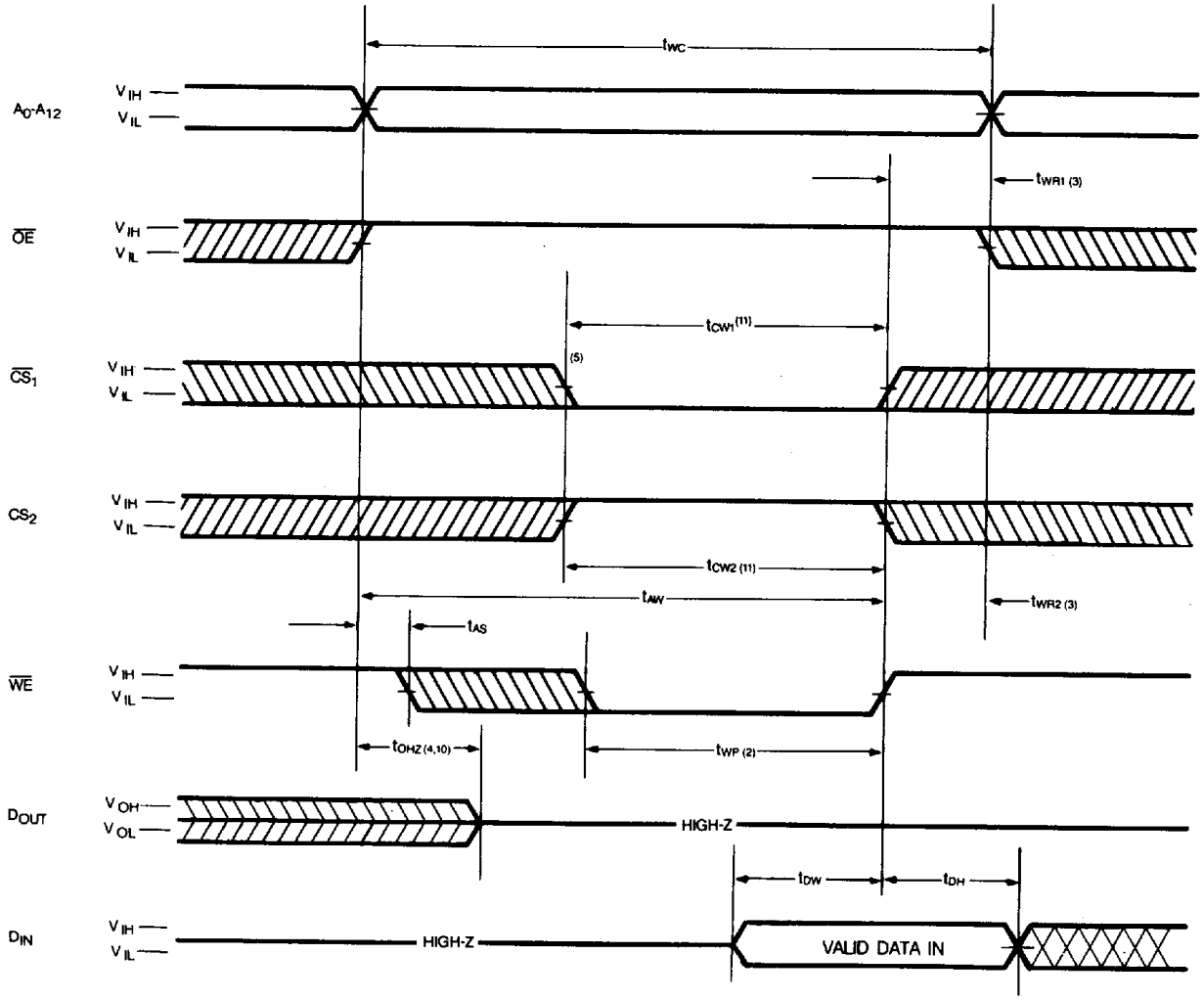


READ CYCLE 4[1,2]



NOTES :
1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected $\overline{CS_1}=V_{IL}$ and $CS_2=V_{IH}$.
3. Addresses are valid prior to or coincident with $\overline{CS_1}$ transition low.
4. $\overline{OE}=V_{IL}$.
5. Transition is measured ± 500mV from steady state. This parameter is sampled and not 100% tested.
6. CS_2 is high.
7. $\overline{CS_1}$ is low.

WRITE CYCLE 1[1]



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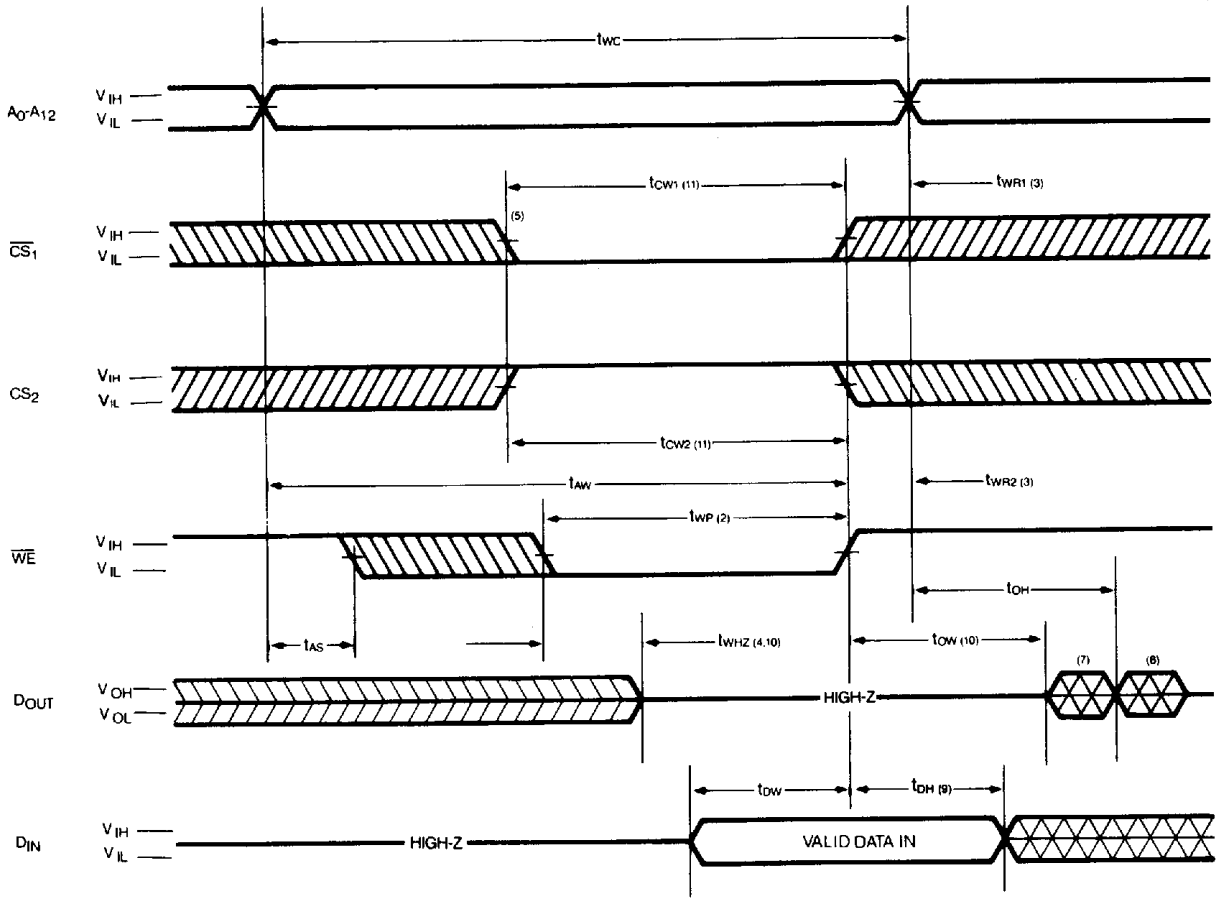
WRITE CYCLE 2[1,6]



NOTES :

1. $\overline{WE}$ must be high during address transitions.
2. A write occurs during the overlap(t_{WP}) of low $\overline{CS_1}$, high CS_2 and low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS_1}$ or $\overline{WE}$ going high or CS_2 going low to the end of write cycle.
4. During this period, I/O pins are in output state so that the input signals of opposite phase to the output must not be applied.
5. If the $\overline{CS_1}$ low transition or the CS_2 high transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low($\overline{OE} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{CS_1}$ is low and CS_2 is high during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the output must not be applied to them.
10. Transition is measured ± 500mV from steady state.
11. t_{CW} is measured from the later of $\overline{CS_1}$ going low or CS_2 going high to the end of write.

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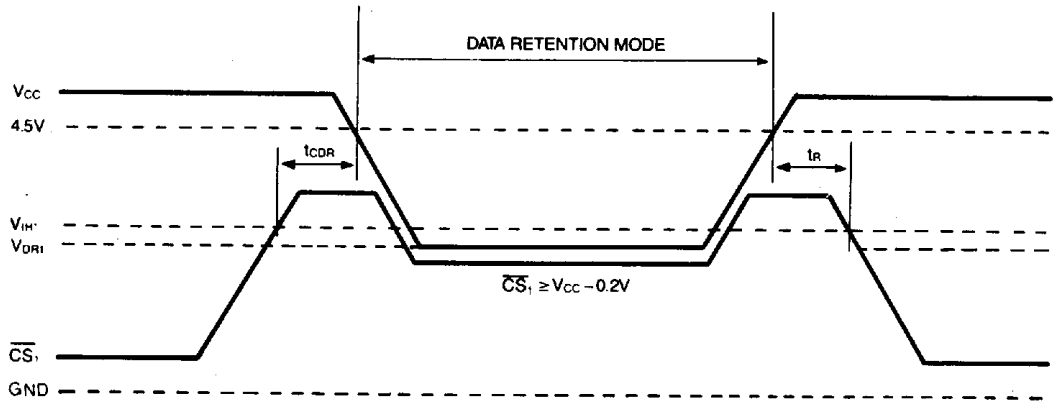
DATA RETENTION CHARACTERISTICS[1]

(T_A=0°C to 70°C)

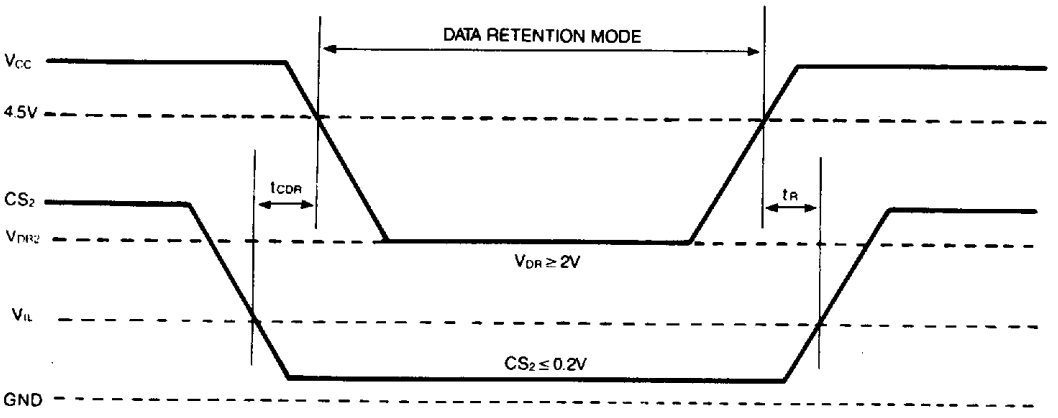
SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.[2]	MAX.	UNIT
V_{DR1}	Data Retention Supply Voltage	$\overline{CS_1} \geq V_{CC}-0.2V$, $CS_2 \geq V_{CC}-0.2V$ or $CS_2 \leq 0.2V$	2.0	–	–	V
V_{DR2}		$CS_2 \leq 0.2V$, $\overline{CS_1} \geq V_{CC}-0.2V$ or $\overline{CS_1} \leq 0.2V$	2.0	–	–	V
I_{CCDR1}	Data Retention Current	V_{CC}=3V, V_{IN}= 0V to V_{CC} $\overline{CS_1} \geq V_{CC}-0.2V$, $CS_2 \geq V_{CC}-0.2V$ or $CS_2 \leq 0.2V$	–	2	50	μA
I_{CCDR2}		V_{CC}=3V, V_{IN}= 0V to V_{CC} $CS_2 \leq 0.2V$, $\overline{CS_1} \geq V_{CC}-0.2V$ or $\overline{CS_1} \leq 0.2V$	–	2	50	μA
t_{CDR}	Chip Deselect to Data Retention Time	See Data Retention Timing Diagram	0	–	–	ns
t_R	Operation Recovery Time		t_{RC}[3]	–	–	ns

NOTES :
1. These characteristics are guaranteed only for L-version
2. T_A= 25°C
3. t_{RC}=Read Cycle Time

DATA RETENTION TIMING DIAGRAM 1 ($\overline{CS_1}$ Controlled)



DATA RETENTION TIMING DIAGRAM 2 ($\overline{CS_2}$ Controlled)



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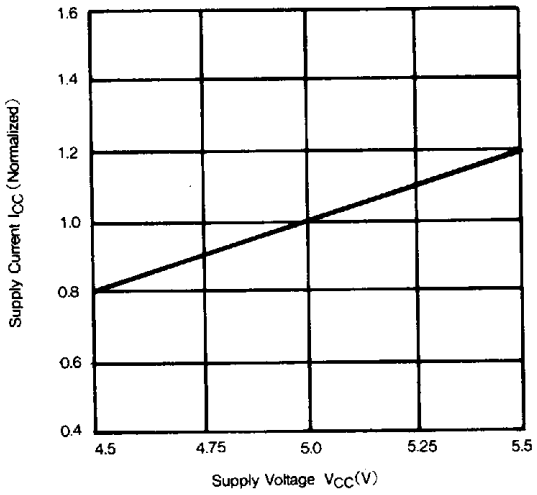
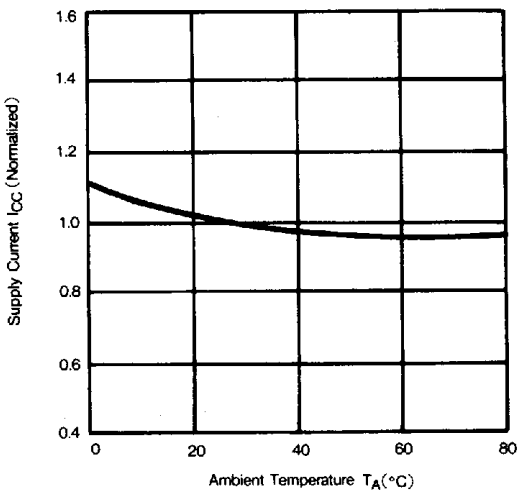
ELECTRICAL CHARACTERISTIC CURVES

(V_{CC}=5V, T_A=25°C, unless otherwise noted)

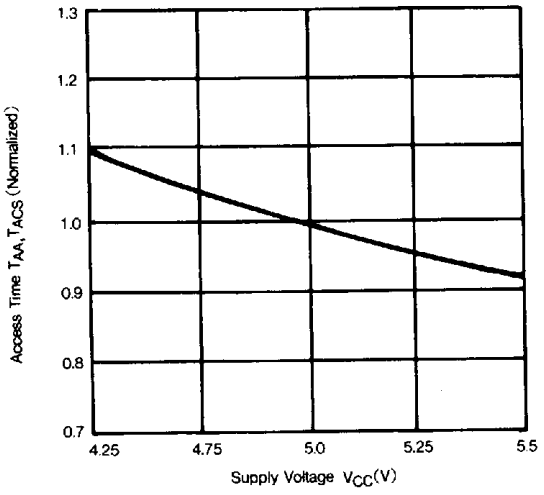
SUPPLY CURRENT vs. SUPPLY VOLTAGE



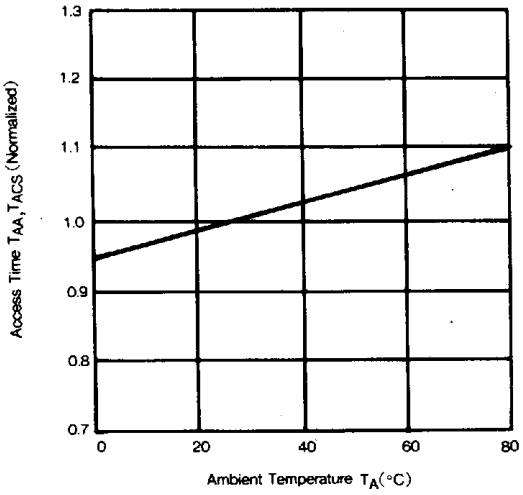
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



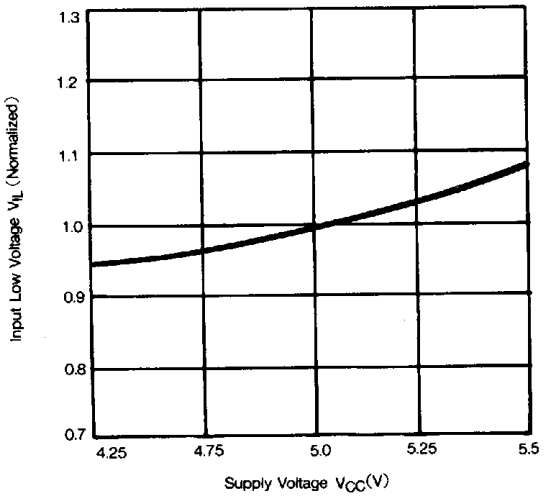
ACCESS TIME vs. SUPPLY VOLTAGE



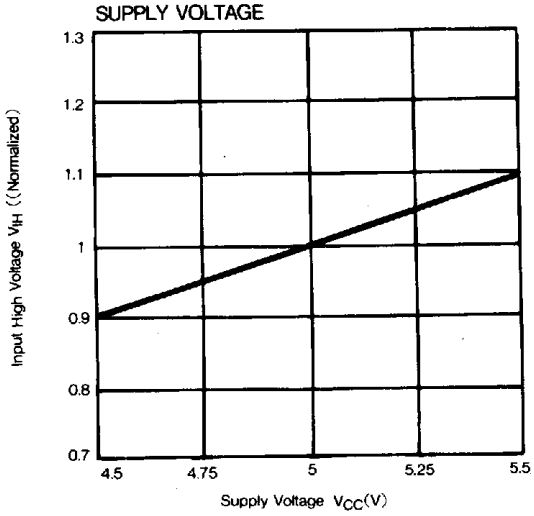
ACCESS TIME vs. AMBIENT TEMPERATURE



INPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



INPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



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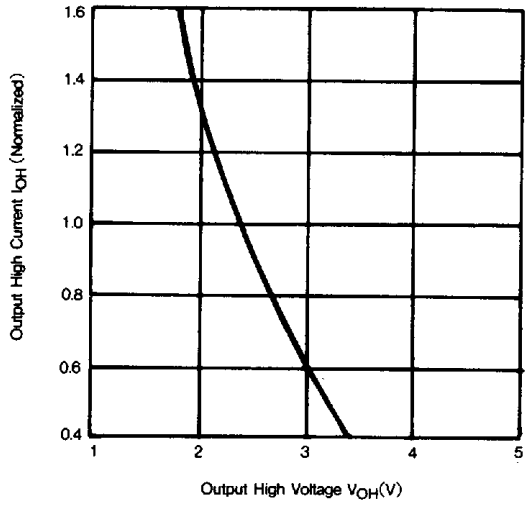
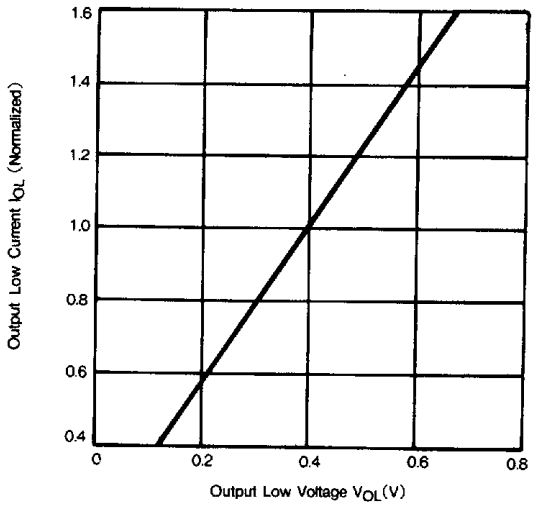
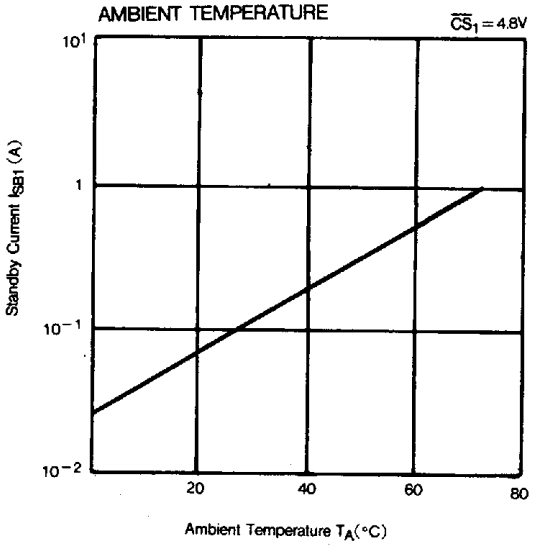
OUTPUT CURRENT vs. OUTPUT VOLTAGE



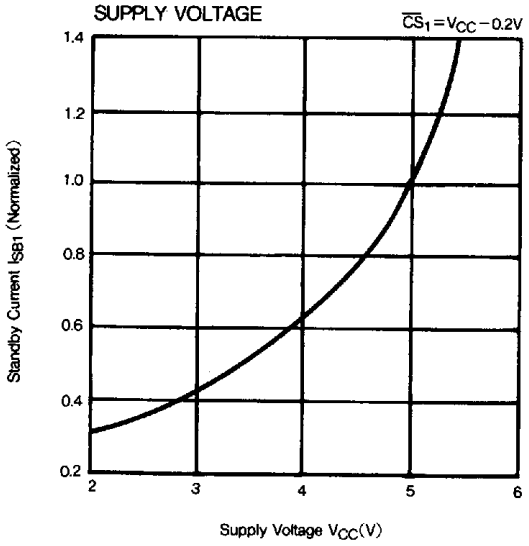
OUTPUT CURRENT vs. OUTPUT VOLTAGE



STANDBY CURRENT vs. AMBIENT TEMPERATURE



STANDBY CURRENT vs. SUPPLY VOLTAGE



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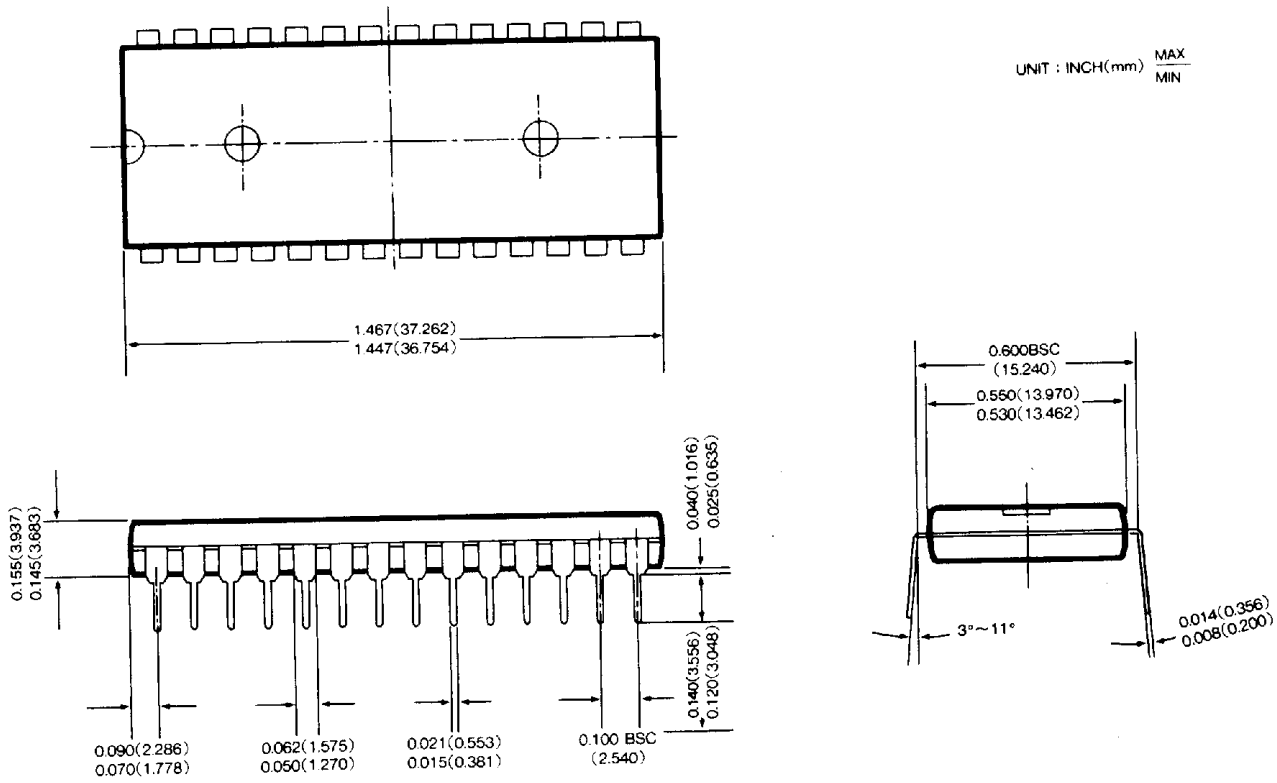
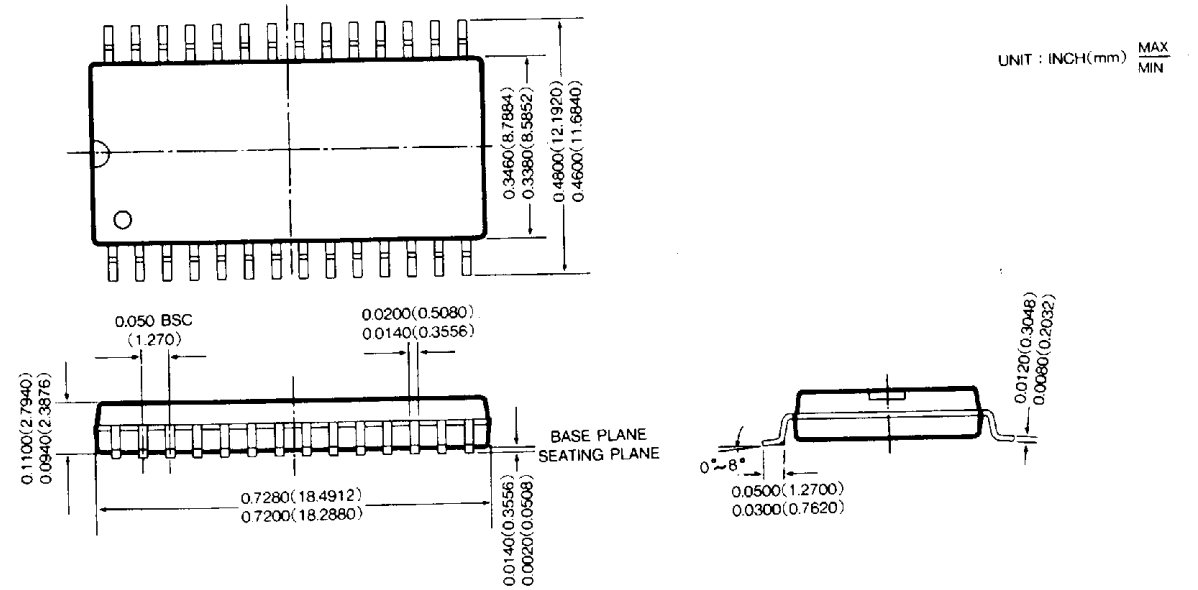
PACKAGE INFORMATION

• 28 PIN PLASTIC DUAL IN LINE PACKAGE−600MIL



• 28 PIN SMALL OUTLINE PACKAGE−330MIL



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