HA17384SPS/SRP, HA17384HPS/HRP, HA17385HPS/HRP

High Speed Current Mode PWM Control IC
for Switching Power Supply

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Description

The HA17384S/H and HA17385H are PWM control switching regulator IC series suitable for highspeed, current-mode switching power supplies. With ICs from this series and a few external parts, a small, low cost flyback-transformer switching power supply can be constructed, which facilitates good line regulation by current mode control. Synchronous operation driven after an external signal can also be easily obtained which offers various applications such as a power supply for monitors small multi-output power supply.

The IC series are composed of circuits required for a switching regulator IC. That is a under-voltage lockout (UVL), a high precision reference voltage regulator (5.0 V ± 2%), a triangular wave oscillator for timing generation, a high-gain error amplifier, and as totem pole output driver circuit which directly drives the gate of power MOSFETs found in main switching devices. In addition, a pulse-by-pulse type, high-speed, current-detection comparator circuit with variable detection level is incorporated which is required for current mode control.

The HA17384SPS includes the above basic function circuits. In addition to these basic functions, the H Series incorporates thermal shut-down protection (TSD) and overvoltage protection (OVP) functions, for configuration of switching power supplies that meet the demand for high safety levels.

Between the HA17384 and HA17385, only the UVL threshold voltages differ as shown in the product lineup table.(See next page.)

This IC is pin compatible with the "3842 family" ICs made by other companies in the electronics industry. However, due to the characteristics of linear ICs, it is not possible to achieve ICs that offer full compatibility in every detail.

Therefore, when using one of these ICs to replace another manufacturer's IC, it must be recognized that it has different electrical characteristics, and it is necessary to confirm that there is no problem with the power supply (mounting) set used.

HA17384SPS/SRP, HA17384HPS/HRP, HA17385HPS/HRP

Functions

- Under-voltage lockout system
- Reference voltage regulator of 5.0 V ± 2%
- Triangular wave (sawtooth) oscillator
- Error amplifier
- Totem pole output driver circuit (direct driving for power MOSFETs)
- Current-detection comparator circuit for current mode
- OVP function (over voltage protection) [1]
- TSD function (thermal shut-down protection) [1]
- Protect function by zener diode (between power input and GND)

Note: 1. H series only.

Features

- High-safety UVL circuit is used (Both V_{IN} and Vref are monitored)
- High speed operation:
  — Current detection response time: 100 ns Typ
  — Maximum oscillation frequency: 500 kHz
- Low standby current: 170 µA Typ
- Wide range dead band time
  (Discharge current of timing capacitance is constant 8.4 mA Typ)
- Able to drive power MOSFET directly
  (Absolute maximum rating of output current is ±1 A peak)
- OVP function (over voltage protection) is included [1]
  (Output stops when FB terminal voltage is 7.0 V Typ or higher)
- TSD function (thermal shut-down protection) is included [1]
  (Output stops when the temperature is 160°C Typ or higher)
- Zener protection is included
  (Clamp voltage between V_{IN} and GND is 34 V Typ)
- Wide operating temperature range:
  — Operating temperature: –20°C to +105°C
  — Junction temperature: 150°C [2]

Note: 1. H series only.
      2. S series only.

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Product Line-up

Package		Additional Function		UVL Power Supply Threshold Voltage	
DILP8 (DP-8)	SOP8 (FP-8DC)	TSD (Thermal shut-down protection)	OVP (Over voltage protection)	$V_{TH\ UVL}$ (V) Typ	$V_{TL\ UVL}$ (V) Typ
HA17384SPS	HA17384SRP	—	—	16.0	10.0
HA17384HPS	HA17384HRP	❍	❍		
HA17385HPS	HA17385HRP	❍	❍	8.4	7.6

Pin Arrangement

COMP | 1   8 | Vref
FB | 2   7 | V_{IN}
CS | 3   6 | OUT
R_T/C_T | 4   5 | GND

(Top view)
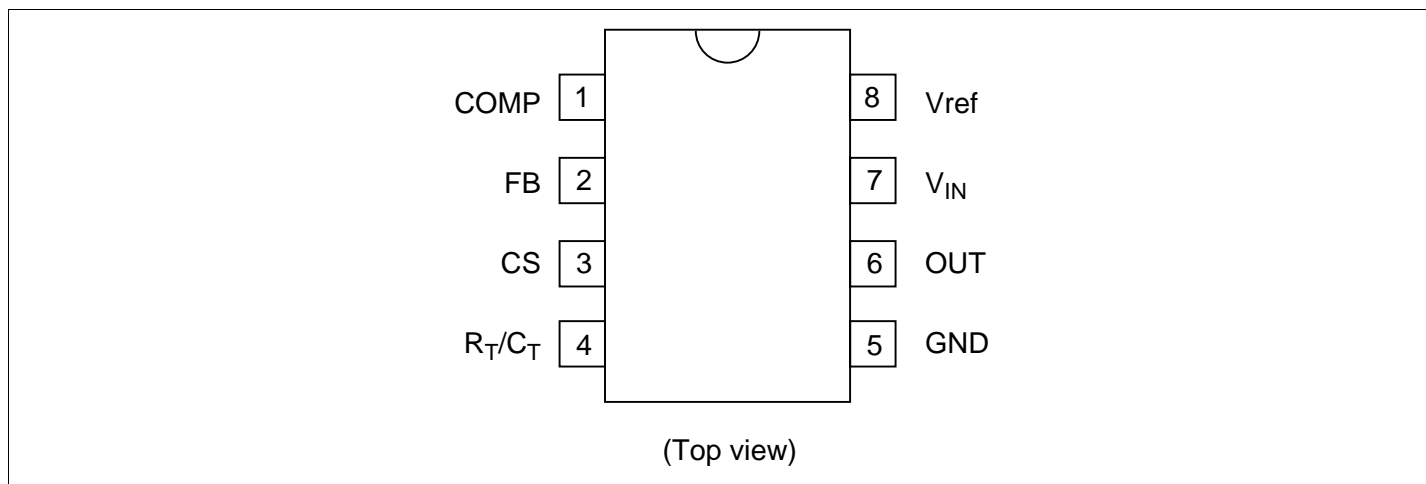
Pin Function

Pin No.	Symbol	Function	Note
1	COMP	Error amplifier output pin	
2	FB	Inverting input of error amp./OVP input pin	1
3	CS	Current sensing signal input pin	
4	R_T/C_T	Timing resistance, timing capacitance connect pin	
5	GND	Groung pin	
6	OUT	PWM Pulse output pin	
7	V_{IN}	Power supply voltage input pin	
8	Vref	Reference voltage 5V output pin	

Note: 1.   Overvoltage protection (OVP) input is usable only for the HA17384H and HA17385H.

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Block Diagram

0.8mA

COMP 1

EA

$\frac{1}{2}$ Vref

6.5V

OVP (2.5V)

*1

7.0V

2V$_F$

2R

1V R

FB (OVP input) 2

UVL1

H
L
VL VH

5V band gap reference regulator

OVP latch
$\overline{R}$ Q
S

UVL2
Vref > 4.7V

TSD sense
160°C

OR

8 Vref

7 V$_{IN}$

34V

CS latch
R
S $\overline{Q}$
PWM LOGIC

CS 3

CS

NOR

OUT

Totem pole output circuit

6 OUT

5 GND

Oscillator

Vref

2.8 V

1.2V

8.4 mA

Latch set pulse

RT/CT 4
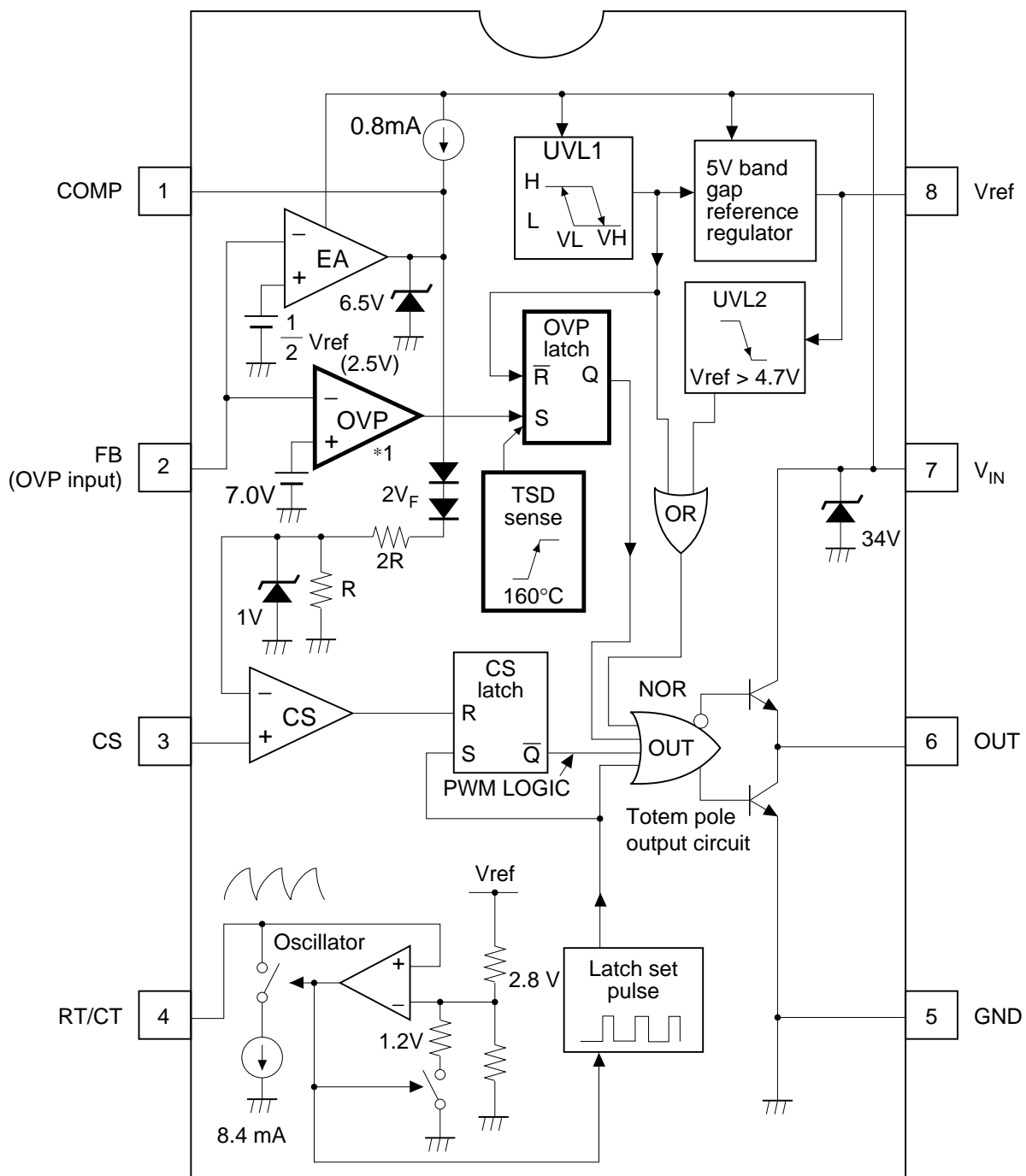
Note: 1. Blocks with bold line are not included in HA17384SPS/SRP.

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Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Note
Supply voltage	V_{IN}	30	V	
DC output current	I_O	±0.1	A	
Peak output current	$I_{O PEAK}$	±1.0	A	
Error amplifier input voltage	V_{FB}	−0.3 to V_{IN}	V	
COMP terminal input voltage	V_{COMP}	−0.3 to +7.5	V	
Error output sink current	I_{OEA}	10	mA	
Power dissipation	P_T	680	mW	1, 2
Operating temperature	Topr	−20 to +105	°C	
Junction temperature	Tj	125	°C	3
		150	°C	4
Storage temperature	Tstg	−55 to +125	°C	3
		−55 to +150	°C	4

Notes: 1. For the HA17384HPS and HA17385HPS,

This value applies up to Ta = 43°C; at temperatures above this, 8.3 mW/°C derating should be applied.

For the HA17384SPS,

This value applies up to Ta = 68°C; at temperatures above this, 8.3 mW/°C derating should be applied.

HA17384SPS/SRP, HA17384HPS/HRP, HA17385HPS/HRP
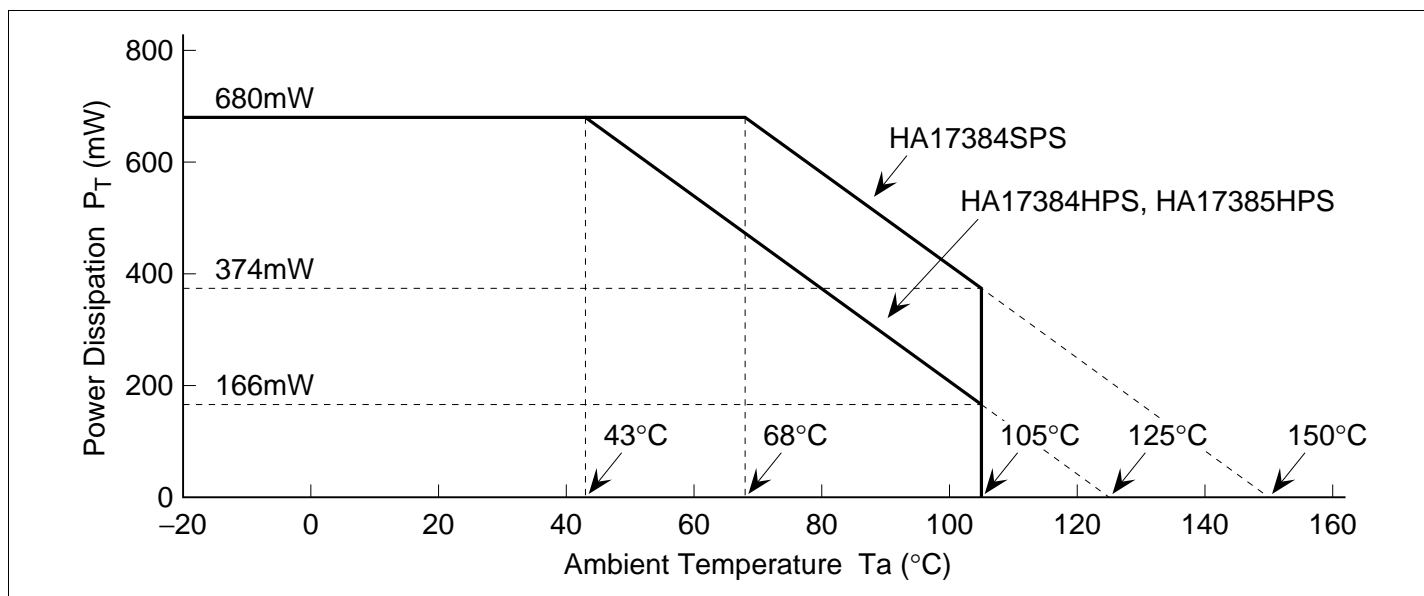
Absolute Maximum Ratings (cont)

Notes: 2. This is the value when the device is mounted on a glass-epoxy substrate (40 mm $\times$ 40 mm $\times$ 1.6 mm). However,
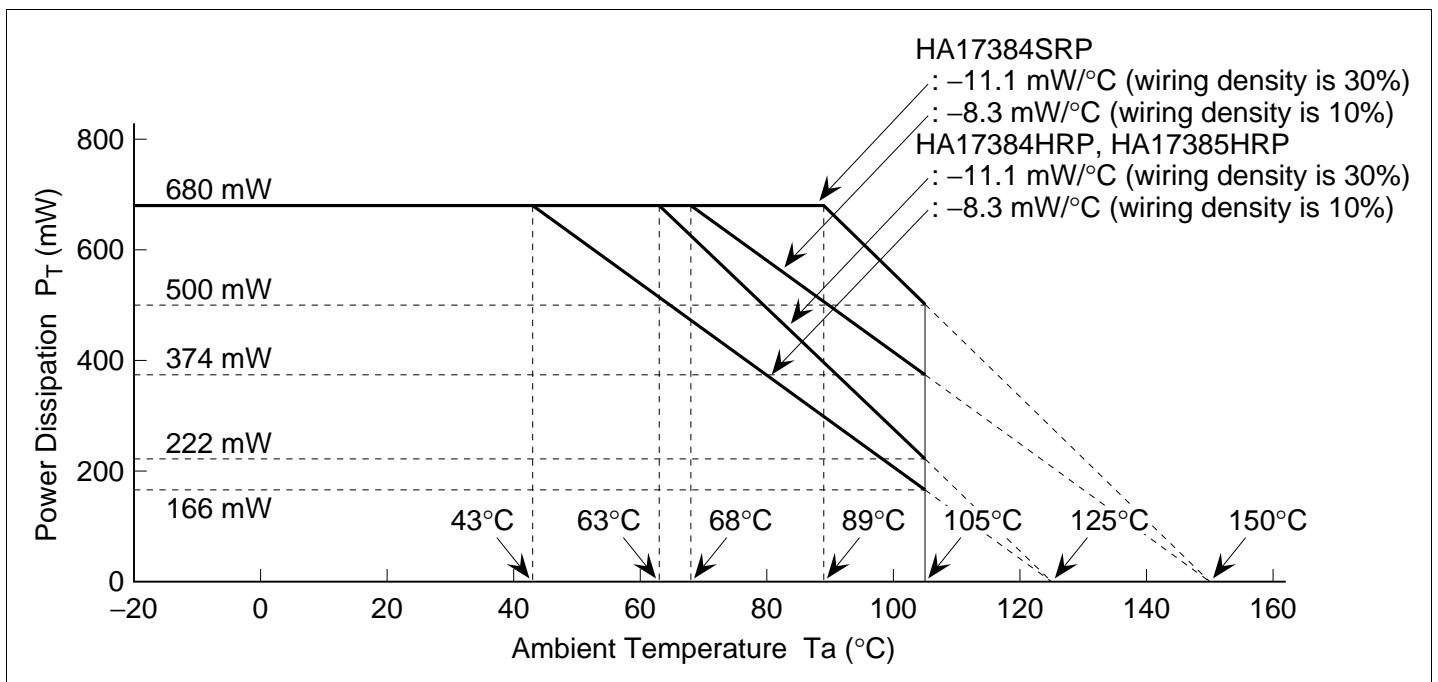
For the HA17384HRP and HA17385HRP,

Derating should be performed with 8.3 mW/°C in the Ta $\geq$ 43°C range if the substrate wiring density is 10%.

Derating should be performed with 11.1 mW/°C in the Ta $\geq$ 63°C range if the substrate wiring density is 30%.

For the HA17384SRP,

Derating should be performed with 8.3 mW/°C in the Ta $\geq$ 68°C range if the substrate wiring density is 10%.

Derating should be performed with 11.1 mW/°C in the Ta $\geq$ 89°C range if the substrate wiring density is 10%.

3. Applies to the HA17384HPS/HRP and HA17385HPS/HRP.

4. Applies to the HA17384SPS/SRP.

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Electrical Characteristics

(The condition is: Ta = 25°C, V_{IN} = 15 V, C_T = 3300 pF, R_T = 10 kΩ without notice)

Reference Part

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Note
Reference output voltage	Vref	4.9	5.0	5.1	V	Io = 1 mA	
Line regulation	Regline	—	20	50	mV	12 V ≤ V_{IN} ≤ 25 V	
Load regulation	Regload	—	10	25	mV	−1 mA ≥ Io ≥ −20 mA	
Output short current	Ios	−30	−100	−180	mA	Vref = 0V	
Temperature stability	ΔVref	—	80	—	ppm/°C	Io = −1 mA, −20°C ≤ Ta ≤ 105°C	1
Output noise voltage	V_N	—	100	—	μV	10 Hz ≤ fnoise ≤ 10 kHz	1

Notes: 1. Reference value for design.

Triangular Wave Oscillator Part

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Note
Typical oscillating frequency	fosc Typ	47	52	57	kHz	C_T = 3300 pF, R_T = 10 kΩ	
Maximum oscillating frequency	fosc Max	500	—	—	kHz		
Supply voltage dependency of oscillating frequency	Δfosc 1	—	±0.5	±2.0	%	12 V ≤ V_{IN} ≤ 25 V	
Temperature dependency of oscillating frequency	Δfosc 2	—	±5.0	—	%	−20°C ≤ Ta ≤ 105°C	1
Discharge current of C_T	Isink$_{CT}$	7.5	8.4	9.3	mA	V_{CT} = 2.0 V	
Low level threshold voltage	V_{TLCT}	—	1.2	—	V		1
High level threshold voltage	V_{THCT}	—	2.8	—	V		1
Triangular wave amplitude	$ΔV_{CT}$	—	1.6	—	V	$ΔV_{CT} = V_{THCT} − V_{TLCT}$	1

Notes: 1. Reference value for design.

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Electrical Characteristics (cont)

Error Amplifire Part / OVP Part

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Note
Non-inverting input voltage	V_{FB}	2.42	2.50	2.58	V	V_{COMP} = 2.5 V	
Input bias current	I_{IB}	—	−0.2	−2.0	µA	V_{FB} = 5.0 V	
Open loop voltage gain	A_{VOL}	65	90	—	dB	2.0 V ≤ V_O ≤ 4.0 V	
Unity gain bank width	BW	0.7	1.0	—	MHz		
Power supply voltage rejection ratio	PSRR	60	70	—	dB	12 V ≤ V_{IN} ≤ 25 V	
Output sink current	$I_{Osink\ EA}$	3.0	9.0	—	mA	V_{FB} = 2.7 V, V_{COMP} = 1.1 V	
Output source current	$I_{Osource\ EA}$	−0.5	−0.8	—	mA	V_{FB} = 2.3 V, V_{COMP} = 5.0 V	
High level output voltage	$V_{OH\ EA}$	5.5	6.5	7.5	V	V_{FB} = 2.3 V, R_L = 15 kΩ(GND)	
Low level output voltage	$V_{OL\ EA}$	—	0.7	1.1	V	V_{FB} = 2.7 V, R_L = 15 kΩ(Vref)	
OVP latch threshold voltage	V_{OVP}	6.0	7.0	8.0	V	Increase FB terminal voltage	1
OVP (FB) terminal input current	$I_{FB(OVP)}$	—	30	50	µA	V_{FB} = 8.0 V	1
OVP latch reset V_{IN} voltage	$V_{IN(OVP\ RES)}$	6.0	7.0	8.0	V	Decreasing V_{IN} after OVP latched	1

Note: 1. These values are not prescribe to the HA17384SPS/SRP because OVP function is not included.

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Electrical Characteristics (cont)

Current Sensing Part

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Note
Voltage gain	A_{VCS}	2.85	3.00	3.15	V/V	$V_{FB} = 0$ V	1
Maximum sensing voltage	Vth_{CS}	0.9	1.0	1.1	V		
Power supply voltage rejection ratio	PSRR	—	70	—	dB	12 V ≤ V_{IN} ≤ 25 V	2
Input bias current	I_{BCS}	—	–2	–10	μA	$V_{CS} = 2$ V	
Current sensing response time	tpd	50	100	150	ns	Time from when V_{CS} becomes 2 V to when output becomes "L" (2 V)	3

Notes: 1. The gain this case is the ratio of error amplifier output change to the current-sensing threshold voltage change.
2. Reference value for design.
3. Current sensing response time tpd is definded a shown in the figure 1.
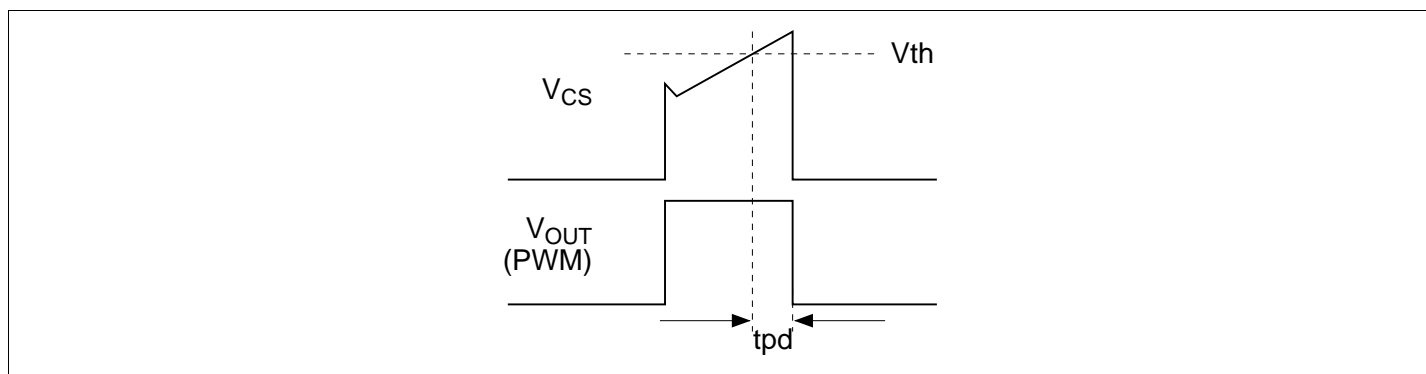
Figure 1 Definition of Current Sensing Response Time tpd

PWM Output Part

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Note
Output low voltage 1	V_{OL1}	—	0.7	1.5	V	Iosink = 20 mA	
Output low voltage 2	V_{OL2}	—	1.5	2.2	V	Iosink = 200 mA	1
Output high voltage 1	V_{OH1}	13.0	13.5	—	V	Iosource = –20 mA	
Output high voltage 2	V_{OH2}	12.0	13.3	—	V	Iosource = –200 mA	1
Output low voltage at standby mode	$V_{OL\ STB}$	—	0.8	1.1	V	$V_{IN} = 5$ V, Iosink = 1 mA	
Rise time	t_r	—	80	150	ns	$C_L = 1000$ pF	
Fall time	t_f	—	70	130	ns	$C_L = 1000$ pF	
Maximum ON duty	Du max	94	96	100	%		
Minimum ON duty	Du min	—	—	0	%		

Notes: 1. Pulse application test

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Electrical Characteristics (cont)

UVL Part

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Note
Threshold voltage for	$V_{TH\ UVL}$	14.5	16.0	17.5	V	Turn-ON voltage	1
high V_{IN} level		7.6	8.4	9.2	V	when V_{IN} is rising	2
Threshold voltage for	$V_{TL\ UVL}$	9.0	10.0	11.0	V	Minimum operating	1
low V_{IN} level		6.8	7.6	8.4	V	voltage after turn-ON	2
V_{IN} UVL hysteresis voltage	$V_{HYS\ UVL}$	5.0	6.0	7.0	V	$V_{HYS\ UVL} = V_{TH\ UVL} - V_{TL\ UVL}$	1
		0.6	0.8	1.0	V		2
Vref UVL threshold voltage	$V_{T\ Vref}$	4.3	4.7	Vref	V	Voltage is forced toVref terminal	

Notes: 1. For the HA17384S/H.
2. For the HA17385H.

Total Characteristics

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Note
Operating current	I_{IN}	7.0	10.0	13.0	mA	C_L = 1000 pF, $V_{FB} = V_{CS}$ = 0 V	
Standby current	I_{STBY}	120	170	230	μA	Current at start up	
Current of latch	I_{LATCH}	200	270	340	μA	V_{FB} = 0 V after $V_{FB} = V_{OVP}$	1, 2
Power supply zener voltage	V_{INZ}	31	34	37	V	I_{IN} + 2.5 mA	
Overheat protection starting temperature	Tj_{TSD}	—	160	—	°C		3, 4

Notes: 1. These values are not prescribe to the HA17384SPS/SRP because OVP function is not included.
2. V_{IN} = 8.5 V in case of the HA17384H.
2. These values are not prescribe to the HA17384SPS/SRP because TSD function is not included.
4. Reference value for design.

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Timing Chart

Signal Name	Waveform timing (Outline)

Power ON   IC turn ON   OVP input   Power OFF

Stationary operation   OVP latched condition   Reset of OVP latch

Input voltage V_{IN} Pin 7 — 16 V (8.4 V) — This voltage is determined by the transformer — 10 V (7.6 V) — 7.0 V — 2 V — 0V — 2 V

( ) shows the case using HA17385H

UVL1 Internal signal which cannot be externally monitored. — 0V

Reference voltage Vref Pin 8 — 0V — 5 V — 4.7 V — 4.7 V

UVL2 Internal signal which cannot be externally monitored. — 0V

Oscillation voltage of triangular wave R_T/C_T Pin 4 — 0V — 2.8 V — 1.2 V

IC operates and PWM output stops.

Start up signal Internal signal which cannot be externally monitored. — 0V — Start up latch release

PWM latch setting signal internal signal which cannot be externally monitored. — 0V

Error amplifier input signal V_{FB} Pin 2 — 0V — 7.0 V typ (OVP input)

Error amplifier output signal V_{COMP} Pin 1 I_D [1] — 0V — V_{COMP} — I_D

OVP latch signal Internal signal which cannot be externally monitored. — 0V

PWM output voltage V_{OUT} Pin 6 — 0V — V_{IN}

Note: 1. I_D indicates the power MOSFET drain current; it is actually observed as voltage V_S generated by power MOSFET current detection source resistance R_S.
V_{COMP} indicates the error amp output voltage waveform. Current mode operation is performed so that a voltage 1/3 that of V_{COMP} is the current limiter level.

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Operation (Description of Timing Chart)

From Power ON to Turn On

After the power is switched ON, the power supply terminal voltage (V_{IN}) of this IC rises by charging through bleeder resistor R_B. At this time, when the power voltage is in the range of 2 V to 16 V[*1]. The low-voltage, lock out UVL1 operates and accordingly the OUT voltage, that is, the gate voltage of the power MOSFET, is fixed at 1.3 V or a lower value, resulting in the power MOSFET remaining in the OFF state.

When the power supply voltage reaches 16 V, UVL1 of this IC is reset and the reference voltage (Vref) generating part turns ON. However, until Vref becomes 4.7 V, the low-voltage, lock out UVL2 operates to keep the OUT terminal voltage low. After Vref terminal voltage becomes 4.7 V or higher, OUT terminal outputs a PWM pulse.

Note: 1. The value is for the HA17384S/H.
The value is 8.4 V for the HA17385H.

Generation of Triangular Wave and PWM Pulse

After the output of the Vref, each blocks begins to operate. The triangular wave is generated on the R_T/C_T terminal. For PWM pulses, the triangular wave rise time is taken as the variable on-duty on-time. The triangular wave fall time is taken as the dead-band time. The initial rise of the triangular wave starts from 0 V, and to prevent a large on-duty at this time, the initial PWM pulse is masked and not output. PWM pulses are outputted after the second triangular wave. The above operation is enabled by the charge energy which is charged through the bleeder resistor R_B into the capacitor C_B of V_{IN}.

Stationary Operation

PWM pulses are outputted after the second wave of the triangular wave and stationary operation as the switching power supply starts.

By switching operation from ON/OFF to OFF/ON in the switching device (power MOSFET), the transformer converts the voltage. The power supply of IC V_{IN} is fed by the back-up winding of the transformer.

In the current mode of the IC, the current in the switcing device is always monitored by a source resistor R_{CS}. Then the current limiter level is varied according to the error voltage (COMP terminal voltage) for PWM control. One third of the error voltage level, which is divided by resistors "2R" and "R" in the IC, is used to sense the current (R = 25 kΩ).

Two diodes between the error output and the 2R-R circuit act only as a DC level shifter. Actually, these diodes are connected between the 2R-R circuit and GND, and, the current sensing comparator and GND, respectively. Therefore, these blocks operate 1.4 V higher than the GND level. Accordingly, the error of the current sensing level caused by the switching noise on the GND voltage level is eliminated. The zener diode of 1 V symbolically indicates that the maximum sensing voltage level of the CS terminal is 1 V.

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Power OFF

At power OFF, the input voltage of the transformer gradually decreases and then V_{IN} of IC also decreases according to the input voltage. When V_{IN} becomes lower than 10 V*[2] or Vref becomes lower than 4.7 V, UVL1 (UVL2) operates again and the PWM pulse stops.

Note: 2. The value is for the HA17384S/H.
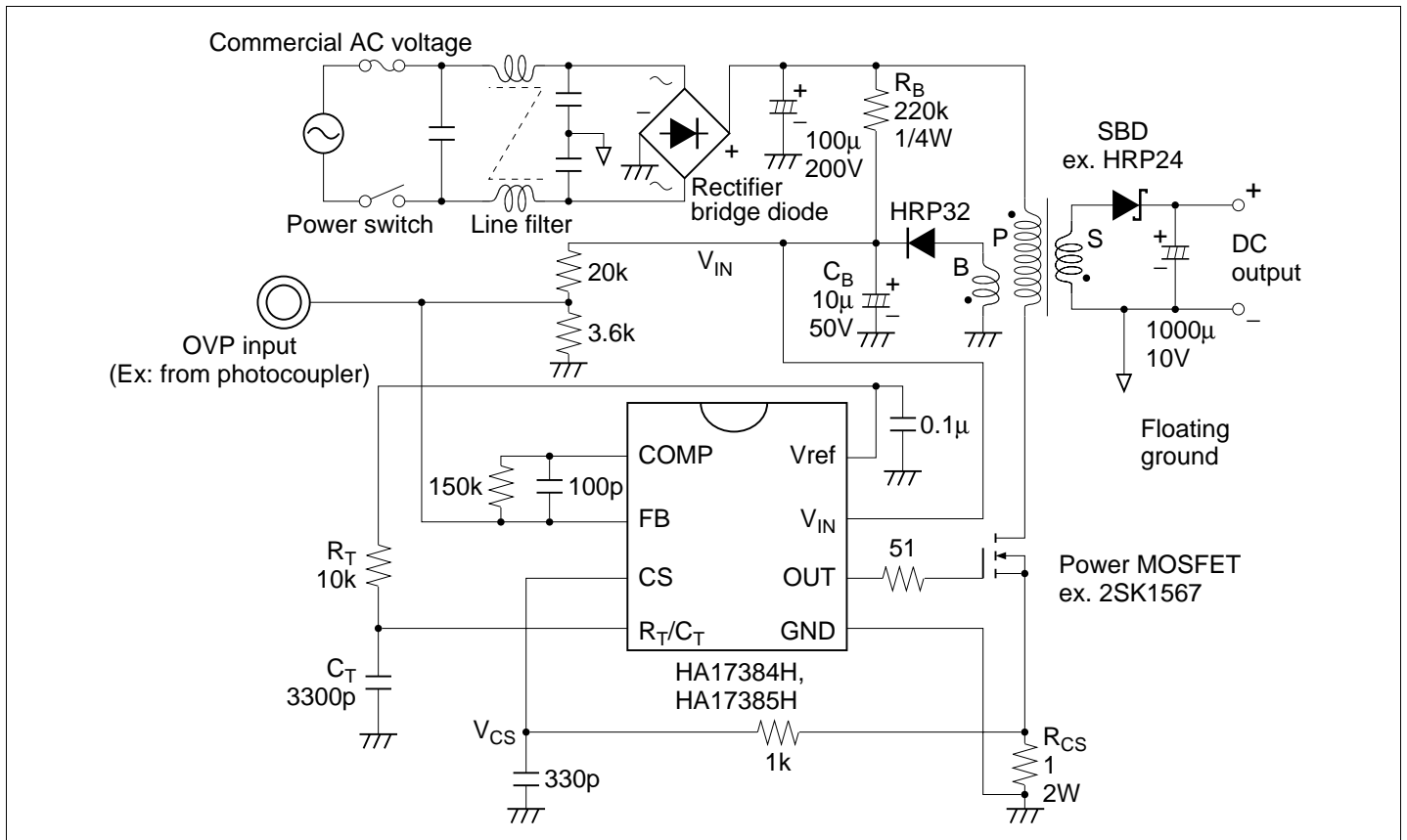   The value is 7.6 V for the HA17385H.

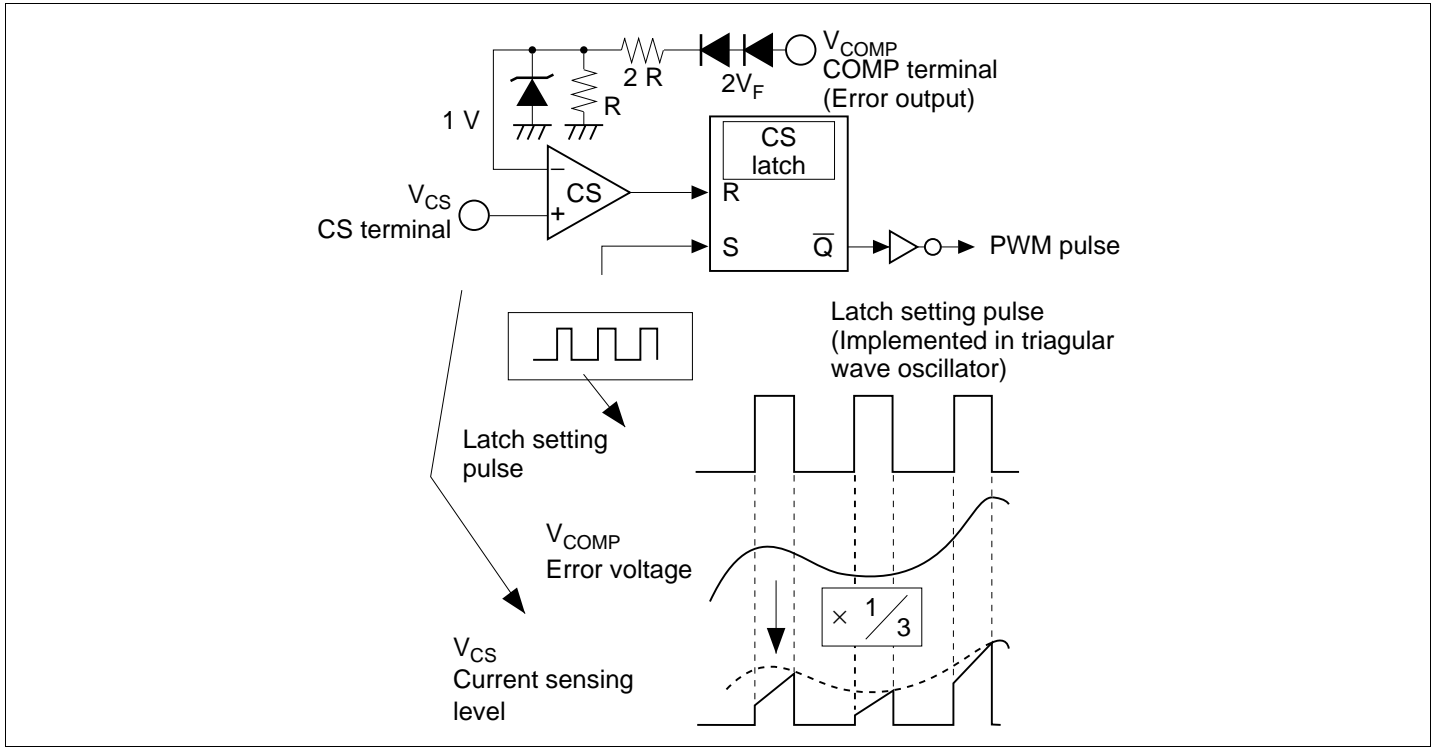**Figure 2   Mounting Circut Diagram for Operation Expression**

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Figure 3   Operation Diagram of Current Sensing Part

Point: 1) At maximum rated load, the setting should be made to give
approximately 90% of area A below.
2) When the OVP latch is operated, the setting should be made
in area B or C.

A : Stationary operation / PWM
(Current-mode operation)
B : Current limit operation / Max duty cycle
C : No sensitivity area / No PWM output
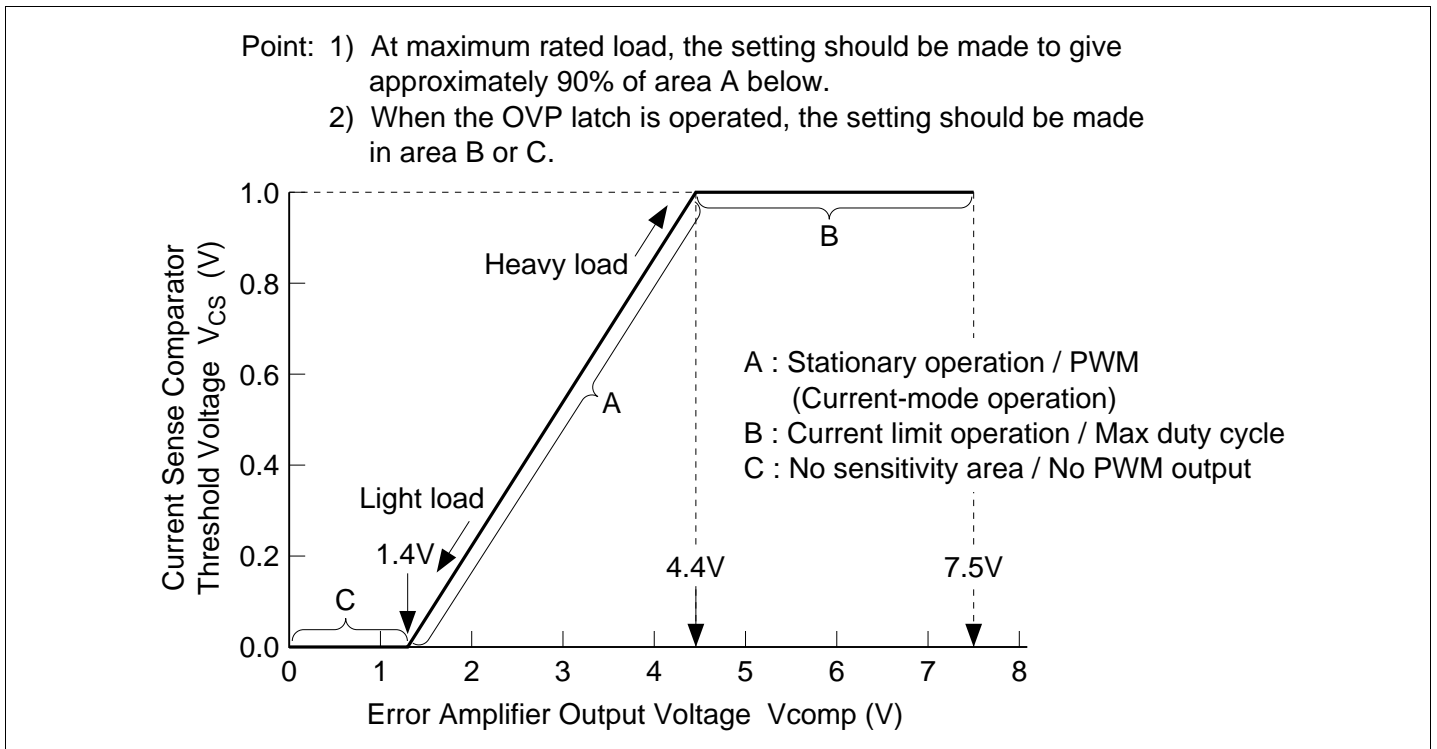
Figure 4   Current Sense Characteristics

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Features and Theory of Current Mode Control

Features of Current Mode Control

- Switch element current detection is performed every cycle, giving a high feedback response speed.
- Operation with a constant transformer winding current gives a highly stable output voltage (with excellent line regulation characteristics, in particular).
- Suitable for flyback transformer use.
- External synchronous operation is easily achieved. (This feature, for example, is applicable to synchronization with a forizontal synchronizing signal of CRT monitor.)

Theory of Current Mode Control

In current mode control, a PWM pulse is generated not by comparing an error voltage with a triangular wave voltage in the voltage mode, but by changing the current limiter level in accordance with the error voltage (COMP terminal in this IC, that is,output of the error amplifier output) which is obtained by constantly monitoring the current of the switching device (power MOSFET) using source resistor R_{CS}.

One of the features of current mode control is that the current limited operates in all cycles of PWM as described by the above theory.

In voltage mode, only one feedback loop is made by an output voltage. In current mode, on the other hand, two loops are used. One is an output voltage loop and the other is a loop of the switching device current itself. The current of the switching device can be controlled switch high speed. In current mode control, the current in the transformer winding is kept constant, resulting in high stability. An important consequence is that the line regulation in terms of total characteristics is better than that in voltage mode.
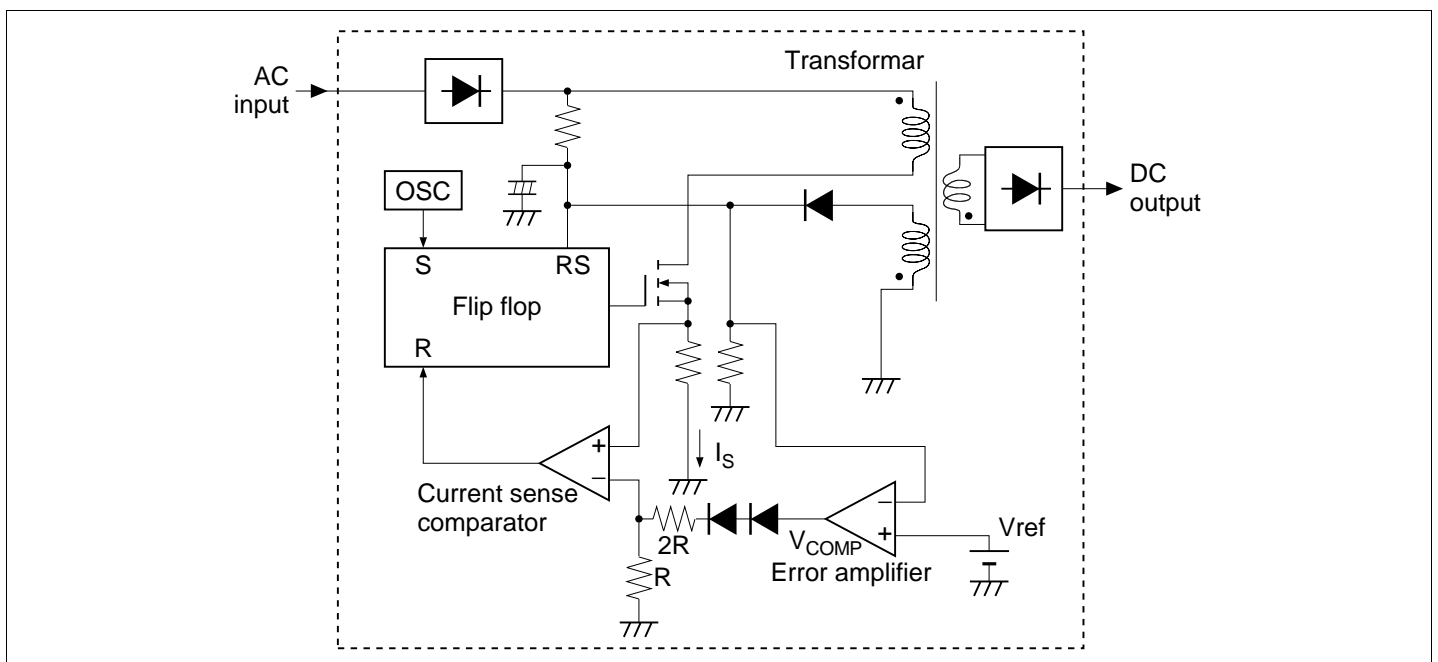
Figure 5   Block Diagram of Current Mode Switching Power Spply

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A. Control in the case of heavy load

V_{CS}

I_S
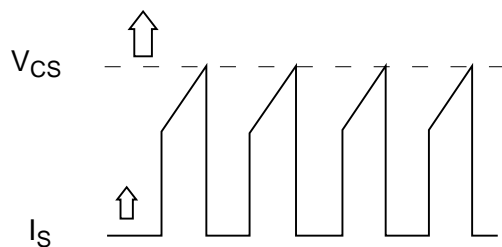
B. Control in the case of light load

V_{CS}

I_S
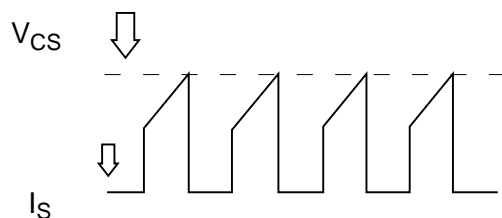
As the load becomes heavy and the DC output decreases, the current sensing level is raised as shown in A. above in order to increase the current in the switching device in each cycle. When the load decreases, inverse control is carried out as shown in B. above.

Figure 6   Primary Current Control of Transformer in Current Mode (Conceptual Diagram)

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Main Characteristics

Supply Current vs. Supply Voltage (HA17384S/H)
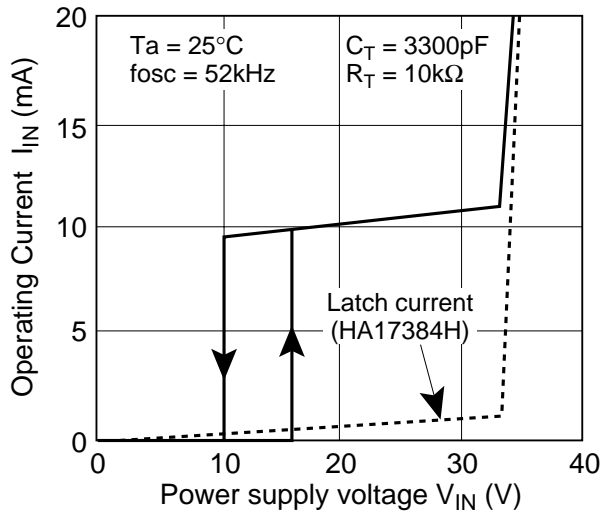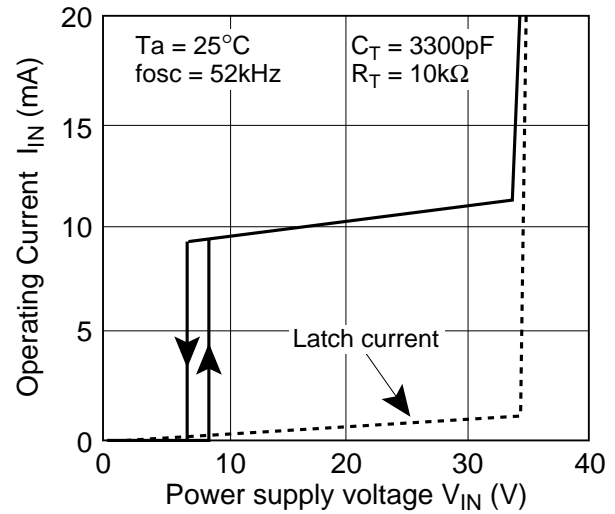
Ta = 25°C
fosc = 52kHz
C_T = 3300pF
R_T = 10kΩ

Latch current
(HA17384H)

Supply Current vs. Supply Voltage (HA17385H)

Ta = 25°C
fosc = 52kHz
C_T = 3300pF
R_T = 10kΩ

Latch current

Standby Current/Latch Current vs. Supply Voltage
Exploded diagram of the small current part from the above figure
(HA17384S/H)

Ta = 25°C

Latch current
(HA17384H)
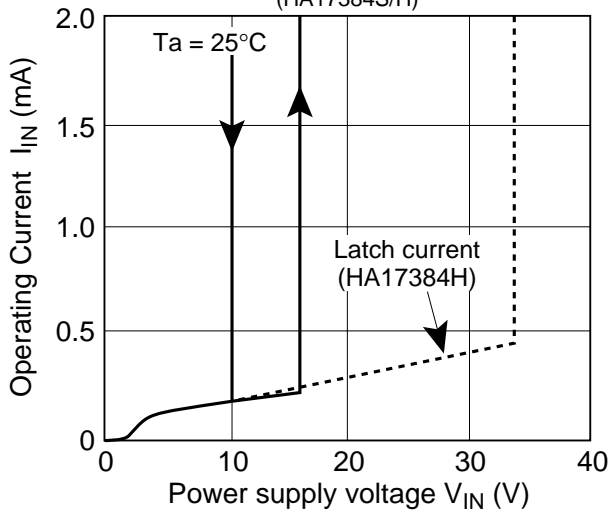
Standby Current/Latch Current vs. Supply Voltage
Exploded diagram of the small current part from the above figure
(HA17385H)

Ta = 25°C
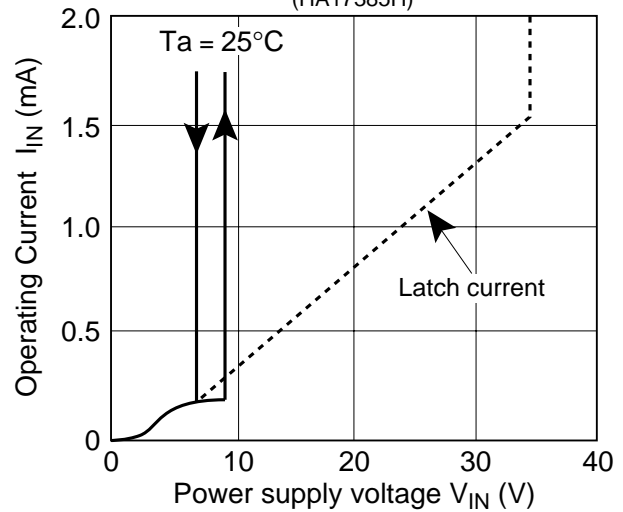
Latch current

Operating Current vs. Ambient Temperature

V_{IN} = 15V
fosc = 52kHz
C_T = 3300pF
R_T = 10kΩ
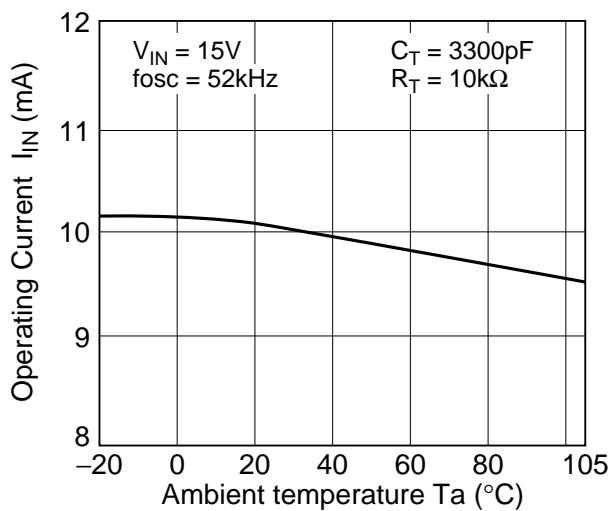
Standby Current/Latch Current vs. Ambient Temperature

Latch current
V_{IN} = 15V (HA17384H)
V_{IN} = 8.5V (HA17385H)

Stanby current

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HA17384SPS/SRP, HA17384HPS/HRP, HA17385HPS/HRP
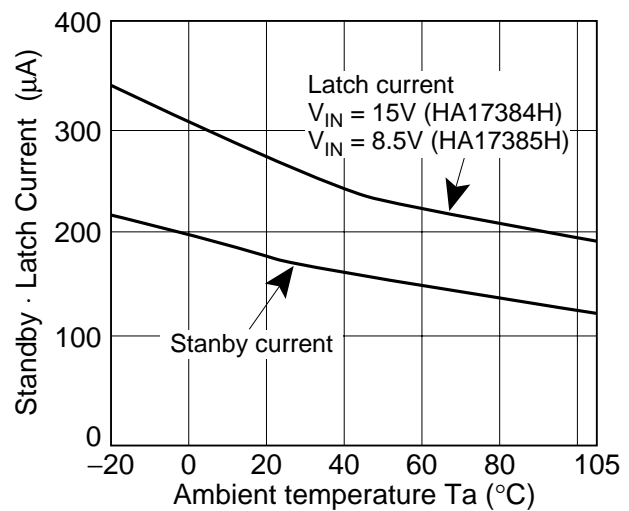
UVL Threshold Voltage vs. Ambient Temperature
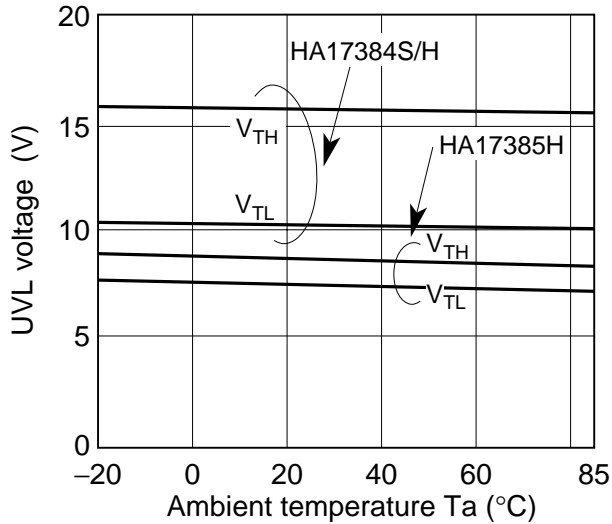
HA17384S/H

V_{TH}

V_{TL}

HA17385H

V_{TH}

V_{TL}

UVL voltage (V) vs. Ambient temperature Ta (°C)

Line Regulation Characteristics of Reference Voltage

Ta = 25°C
V_{IN} = 10V or more (HA17384S/H)
V_{IN} = 7.6V or more (HA17385H)
C_T = 3300pF
R_T = 10kΩ

Reference voltage Vref (V) vs. Supply voltage V_{IN} (V)

Load Regulation Characteristics of Reference Voltage

Ta = 25°C
V_{IN} = 15V
C_T = 3300pF
R_T = 10kΩ

Vref short protection operates

Reference voltage Vref (V) vs. Output current of Vref terminal (mA)

Reference Voltage vs. Ambient Temperature

V_{IN} = 15V
C_T = 3300pF
R_T = 10kΩ

Reference voltage Vref (V) vs. Ambient temperature Ta (°C)
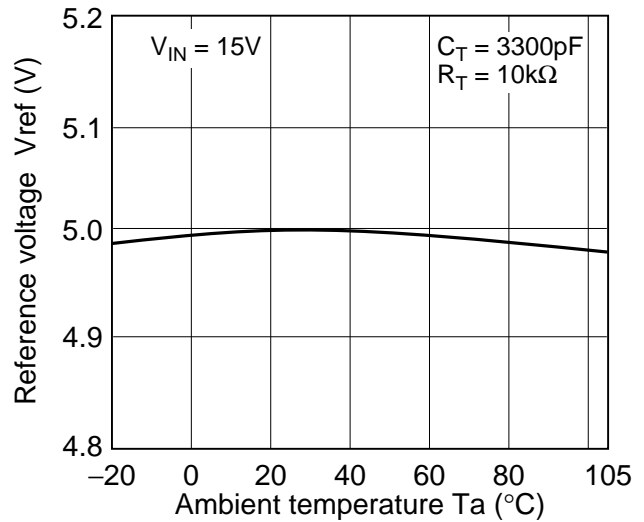
C_T Discharge Current vs. R_T/C_T Terminal Voltage

Ta = 25°C
V_{IN} = 15V
Measured when R_T/C_T terminal voltage is externally supplied

Minimum voltage of triangular wave

Maximum voltage of triangular wave

C_T discharge current I_{CT} (mA) vs. R_T/C_T terminal voltage V_{CT} (V)
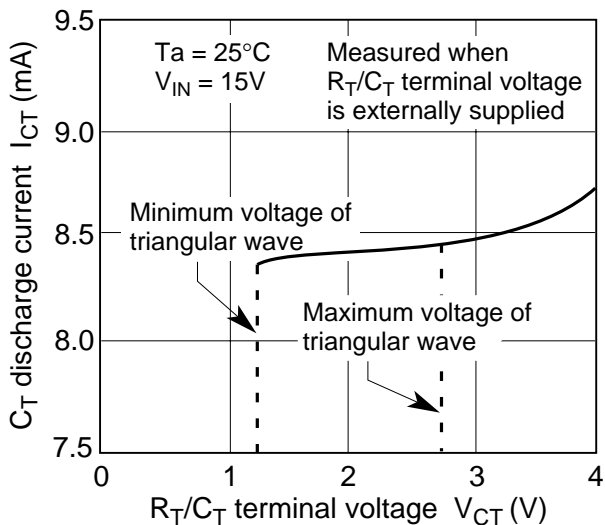
C_T Discharge Current vs. Ambient Temperature

V_{IN}=15 V

Measured when R_T/C_T terminal voltage of 2 V is externally supplied

C_T discharge current Isink$_{CT}$ (mA) vs. Ambient temperature Ta (°C)

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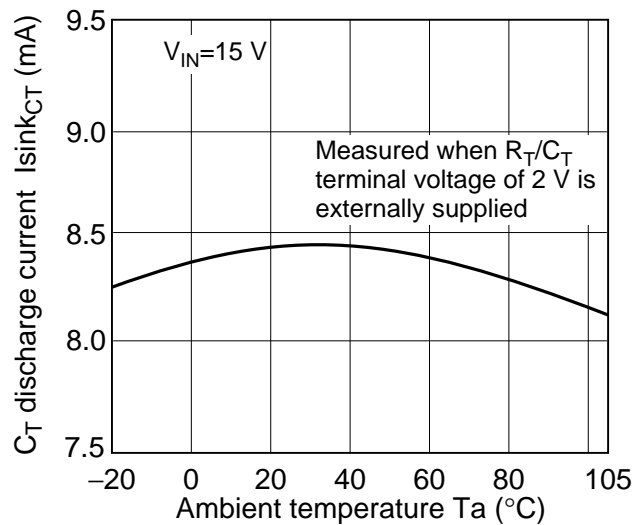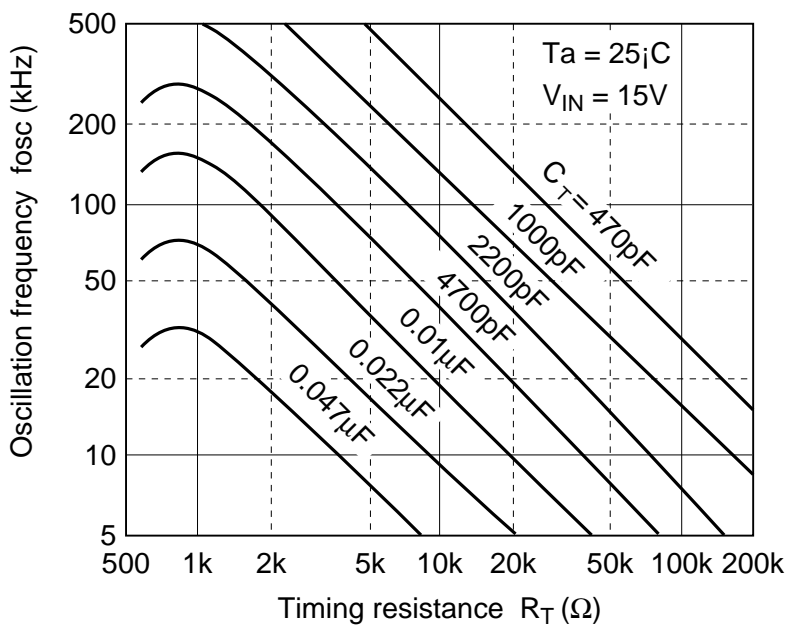
Figure 7   Oscillation Frequency vs. Timing Resistance

Case 1.
Setting large maximum duty cycle.

Triangular wave

PWM maximum ON pulse
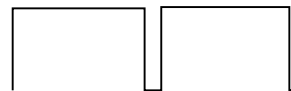
Du max = 95%
fosc = 52kHz

In the case of small C_T and large R_T
(ex. C_T = 3300pF, R_T = 10kΩ)

Case 2.
Setting small maximum duty cycle.

Triangular wave

PWM maximum ON pulse

Du max = 40%
fosc = 52kHz

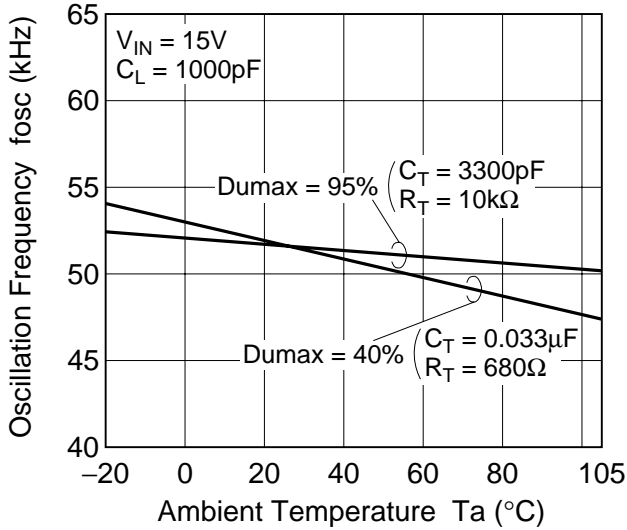In the case of large C_T and small R_T
(ex. C_T = 0.033μF, R_T = 680Ω)

Figure 8   Relationship Between Triangular Wave and Maximum ON Duty of PWM Pulse

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Figure 9   PWM Pulse ON Duty vs. Timing Resistance
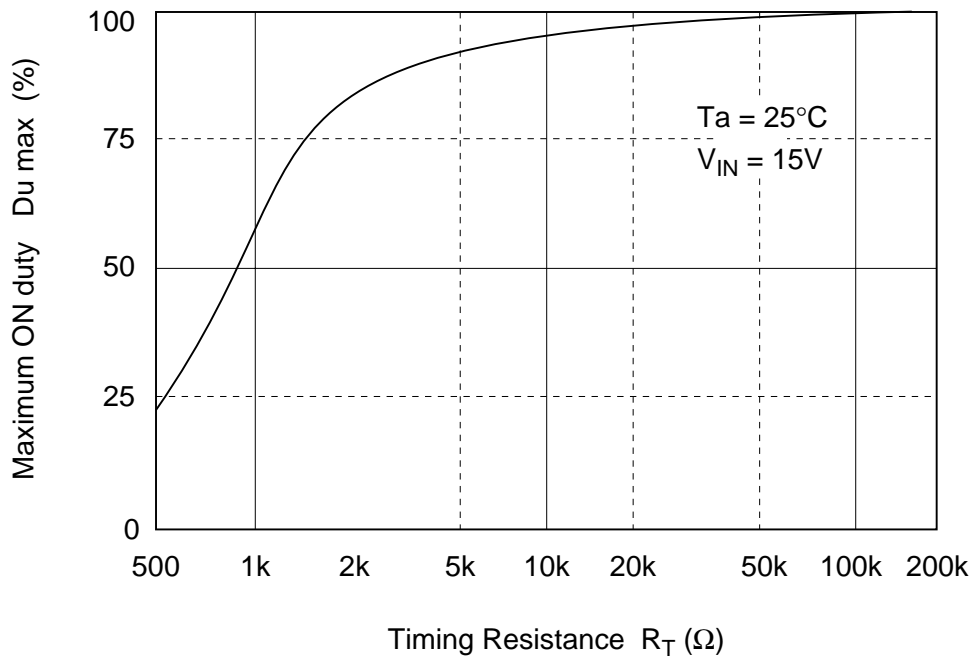
Note: In the oscillation system of this IC, a constant discharging current of 8.4mA flows the timing capacitor during triangular wave fall. Therefore, note that a small maximum ON duty (large dead band) leads to a large supply current. Refer to the equations of oscillation frequency and supply current for details.

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Oscillation Frequency vs. Ambient Temperature

V_{IN} = 15V
C_L = 1000pF

Dumax = 95% (C_T = 3300pF, R_T = 10kΩ)

Dumax = 40% (C_T = 0.033μF, R_T = 680Ω)

Oscillation Frequency f_{osc} (kHz) vs. Ambient Temperature Ta (°C)

Operating Current vs. Maximum ON Duty

V_{IN} = 15V
Ta=25°C
C_L = 1000pF
V_{CS} = 0V
V_{FB} = 0V

f_{osc}=300kHz

f_{osc}=50kHz

Operating Current I_{IN} (mA) vs. Maximum ON Duty Du max (%)
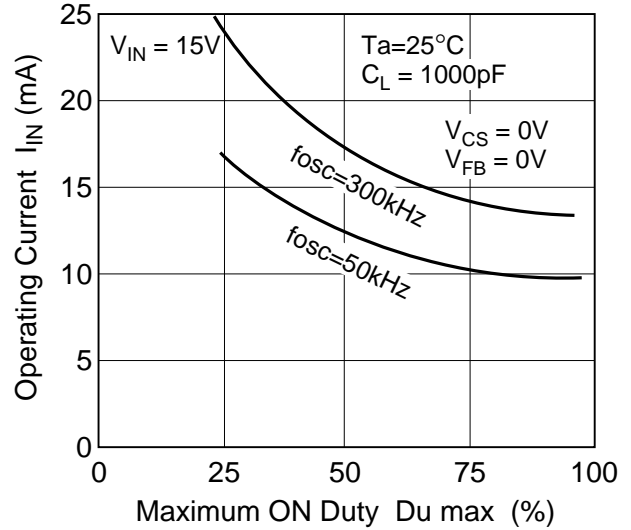
Rise/Fall Time of Output Pulse vs. Load Capacitance

V_{IN} = 15V
V_{CS} = 0V
V_{FB} = 0V

Ta = 25°C
C_T = 3300pF
R_T = 10kΩ

Rise time tr

Fall Time tf

Rise/Fall Time (ns) vs. Output load capacitance C_L (pF)
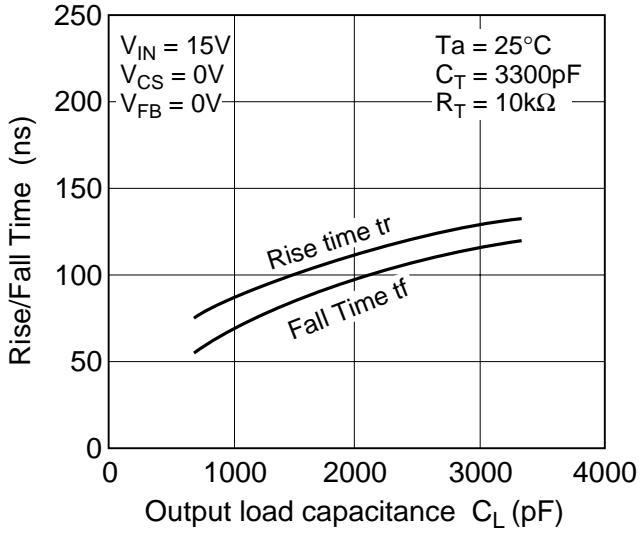
Rise/Fall Time of Output Pulse vs. Ambient Temperature

V_{IN} = 15V
V_{CS} = 0V
V_{FB} = 0V

C_L = 1000pF

C_T = 3300pF
R_T = 10kΩ

Rise time t_r

Fall Time t_f

Rise/Fall Time (ns) vs. Ambient temperature Ta (°C)
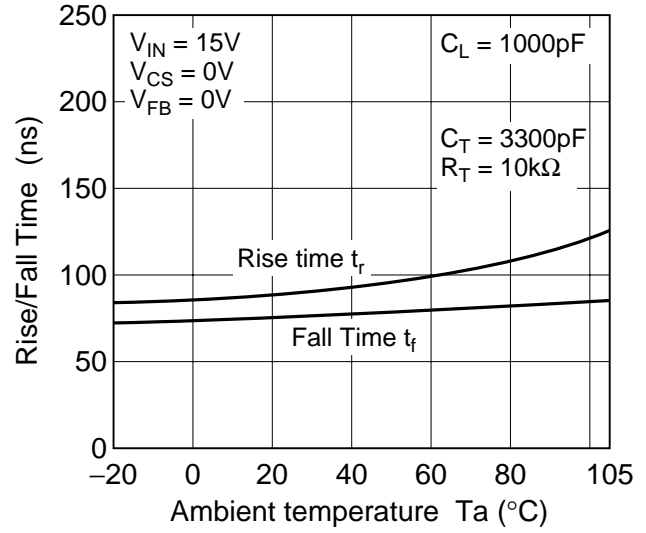
Current Sensing Level vs. Ambient Temperature

V_{IN} = 15V
V_{FB} = 0V

Measured when COMP terminal voltage is externally supplied

Current sensing level V_{CS} (V) vs. Ambient temperature Ta (°C)
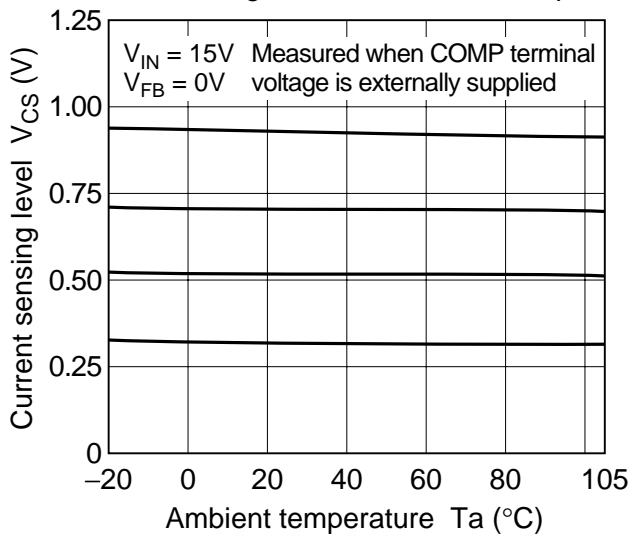
Relationship Between Low Voltage Malfunction Protection and PWM Output

V_{IN} (UVL1)	L	H	H	L
Vref (UVL2)	L	L	H	H
PWM OUTPUT	L	L	Available to output	L
Condition description	Standby state	IC is in the ON state and output is fixed to LO.	Operation state	Standby state

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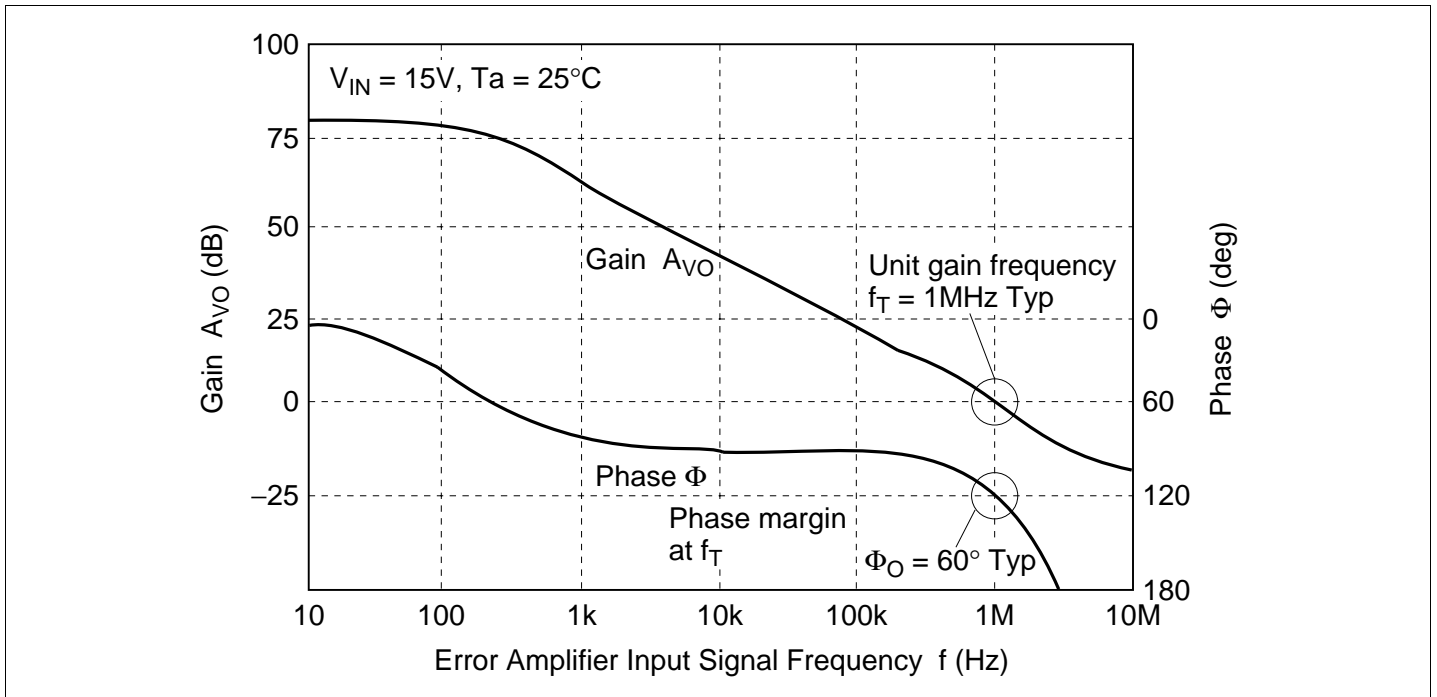
Figure 10   Open Loop Gain Characterisrics of Error Amplifier

● Calculation of operation parameters

1. Maximum ON duty Du max (Refer to the right figure.)

$$\text{Du max} = \cfrac{1}{1 + 1.78 \times \ln\left(1 + \cfrac{190\Omega}{R_T - 440\Omega}\right)}$$

2. Oscillation frequency fosc

$$\text{fosc} = \cfrac{1}{C_T \times R_T \times \left\{0.56 + \ln\left(1 + \cfrac{190\Omega}{R_T - 440\Omega}\right)\right\}}$$

From the above two equations, the following two equations are obtained.

3. Equalization to device R_T from Du max

$$R_T = \cfrac{190\Omega}{e^{0.56\,(1/\text{Du max} - 1)} - 1} + 440\Omega$$

(e = 2.71828.base of natural logarithm)

4. Equation to device C_T from fosc and R_T

$$C_T = 1.78 \times \frac{\text{Du max}}{\text{fosc} \times R_T}$$

5. Operating current I_{IN}

$$I_{IN} = I_Q + \text{Isink}_{CT} \times (1 - \text{Du max}) + C_{iss} \times V_{IN} \times \text{fosc}$$

> providing that $I_Q = 8.4\text{mA}$ Typ (Supply current when oscillation in IC stops.)
> Ciss is the input gate capacitance of the power MOSFET which is connected and V_{IN} is the supply voltage of the IC.

Example 1: Calculation when $R_T = 10\text{k}\Omega$ and $C_T = 3300\text{pF}$
> fosc = 52kHz, Du max = 95%, I_{IN} = 9.7mA

Example 2: Calculation for 50% of Du max and 200 kHz of fosc
> $R_T = 693\Omega$, $C_T = 6360\text{pF}$, I_{IN} = 12.5mA
> However, Ciss = 1000pF, V_{IN} = 18V

> Note that the actual value may differ from the calculated one because of the internal delay in operation and input characteristics of the POWER MOS FET. Check the value when mounting.
> Additionally a small Dumax leads to a large supply current, even if the frequency is not changed, and start up may become difficult. In such a case, the following measure is recommended.

(1) For an AC/DC converter, a small bleeder resistance is required.

(2) The large capacitance between Vref and GND is required.

(3) Use a large Dumax with a triangular wave and raise the current limit of the switching device to around the maximum value (1.0V Typ).

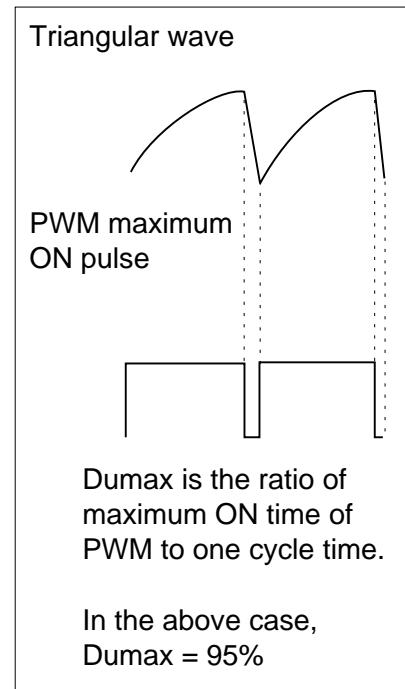The current limit is expressed as $\quad ID_{max} = \dfrac{V_{THCS}}{R_{CS}}$

Triangular wave

PWM maximum ON pulse

Dumax is the ratio of maximum ON time of PWM to one cycle time.

In the above case, Dumax = 95%

Figure 11   Calculation of Operation Parameters

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Application Circuit Example (1)

Notes: 1. ⊥ : PRIMARY GND, ▽ : SECONDARY GND.
2. Check the wiring direction of the transformer coil.
3. Insert a snubber circuit if necessary.
4. OVP function is not included in HA17384SPS/SRP.

Snubber circuit example

(Opetation Theory)
Because this circuit is a flyback type, the voltages in the primary (P), secondary (s) coils of the transformer and backup (B) coil are proportional to each other. Using this, the output voltage of the backup coil (V_{IN} of IC) is controlled at constant 16.4V. (The voltage of the point divided by resistors of 20kΩ and 3.6kΩ is 2.5V).

Figure 12   Primary Voltage Sensing Flyback Converter

Application Circuit Example (2)
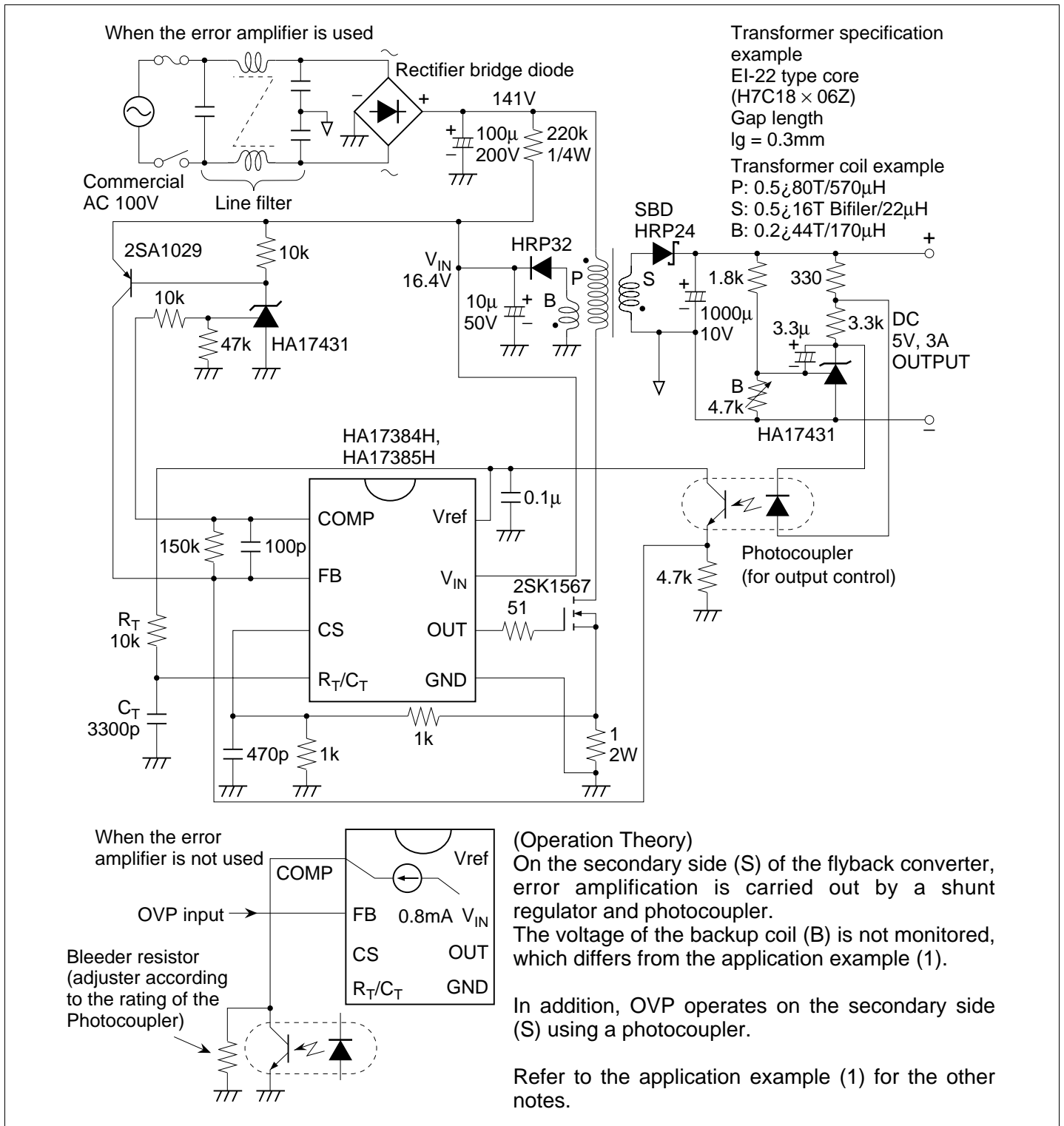
Figure 13   Secondary Voltage Sensing Flyback Converter

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Application Examples for Fuller Exploitation of Power Supply Functions

A number of application examples are briefly described below.

1. Soft start

    A soft start is a start method in which the PWM pulse width is gradually increased when the power supply is activated. This prevents the stress on the transformer and switch element caused by a rapid increase in the PWM pulse width, and also prevents overshoot when the secondary-side output voltage rises. The circuit diagram is shown in figure 14.
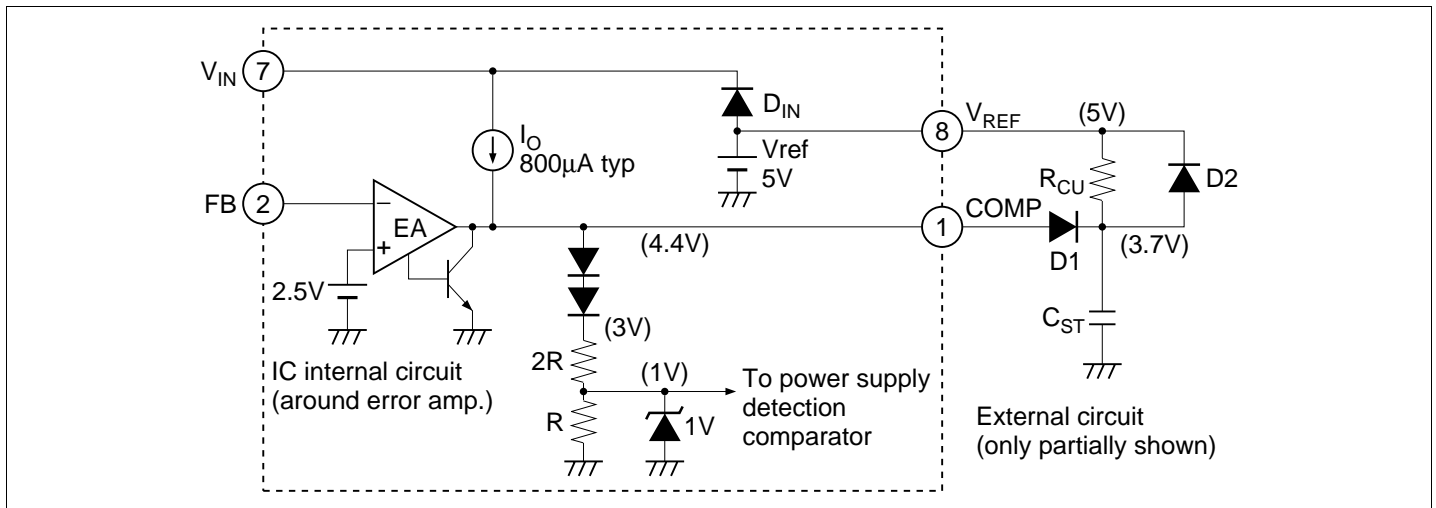
Figure 14   Circuit Diagram for Soft Start

Operation: In this circuit, error amp output source current I_O (800 µA typ.) gradually raises the switch element current detection level, using a voltage slope that charges soft start capacitance C_{ST}. When the voltage at each node is at the value shown in parentheses in the figure, the soft start ends. The soft start time is thus given by the following formula:

$$T_{ST} = (3.7 \text{ V}/800 \text{ µA}) \times C_{ST} \approx 4.62 \, C_{ST} \text{ (ms)}$$
$$(C_{ST} \text{ unit: µF})$$

External parts other than C_{ST} operate as follows:

- Diode D1   : Current detection level shift and current reverse-flow prevention.
- Diode D2   : Together with diode D_{IN} in the IC, C_{ST} charge drawing when power supply falls.
- Resistance R_{CU} : For C_{ST} charge-up at end of soft start. (Use a high resistance of the order of several hundred kΩ.)

Note: During a soft start, since PWM pulses are not output for a while after the IC starts operating, there is a lack of energy during this time, and intermittent mode may be entered. In this case, the capacitance between Vref and GND should be increased to around 4.7 µF to 10 µF.

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2. OVP latch output overvoltage protection (the HA17384H and HA17385H only)

The OVP latch is incorporated in the error amp input pin (FB). If the FB pin is pulled up to 7.0 V typ. just once when the power supply enters any kind of error state, IC operation can be halted and held as it is (latched). To reset the latch, drop the IC's supply voltage to 7.0 V typ. or below momentarily.
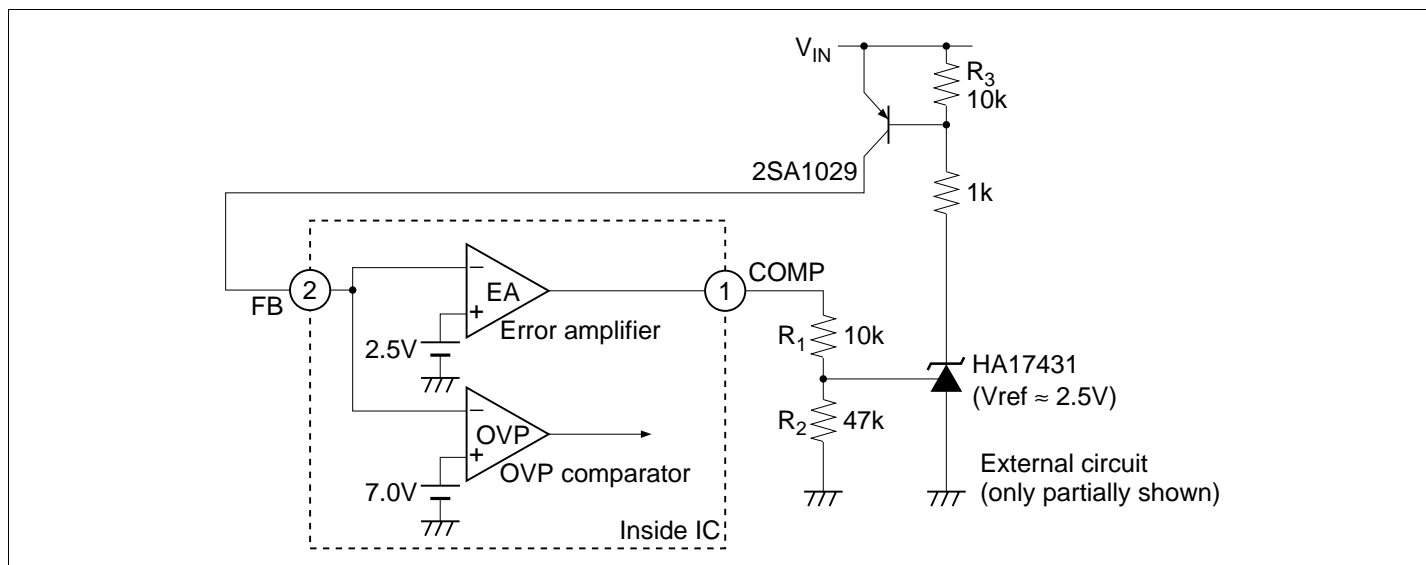
An OVP latch application example is shown in figure 15.

Figure 15   Example of OVP Latch Application Circuit

This circuit protects the system by causing latch operation in the event of an overload or load short. In the steady state, the error amp input/output pins operate at 2.5 V typ., but if the load becomes heavy the FB pin level drops and the COMP pin level rises. As shown in the figure, this is detected by the HA17431 shunt regulator, and the FB pin level is pulled up, operating the OVP latch.

The operation parameters are as follows:

COMP pin voltage detection level: $V_{th} = (R_1 + R_2) / R_2 \times 2.5$ V

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Notice for Use

1. OVP Latch Block

- Case

    When DC power is applied directly as the power supply of the HA17384H, HA17385H, without using the transformer backup coil. Also, when high-frequency noise is superimposed on the V_{IN} pin.

- Problem

    The IC may not be turn on in the case of a circuit in which V_{IN} rises quickly (10 V/100 μs or faster), such as that shown in figure 16. Also, the OVP latch may operate even though the FB pin is normally at V_{OVP} or below after the IC is activated.

- Reason

    Because of the IC circuit configuration, the timer latch block operates first.

- Remedy (counter measure)

    Take remedial action such as configuring a time constant circuit (R_B, C_B) as shown in figure 17, to keep the V_{IN} rise speed below 10 V/100 μs. Also, if there is marked high-frequency noise on the V_{IN} pin, a noise cancellation capacitor (C_N) with the best possible high-frequency characteristics (such as a ceramic capacitor) should be inserted between the V_{IN} pin and GND, and close to the V_{IN} pin.

When configuring an IC power supply with an activation resistance and backup winding, such as an AC/DC converter, the rise of V_{IN} will normally be around 1 V/100 μs, and there is no risk of this problem occurring, but careful attention must be paid to high-frequency noise.

Also, this phenomenon is not occuring to the HA17384S, because OVP function is not built-in.
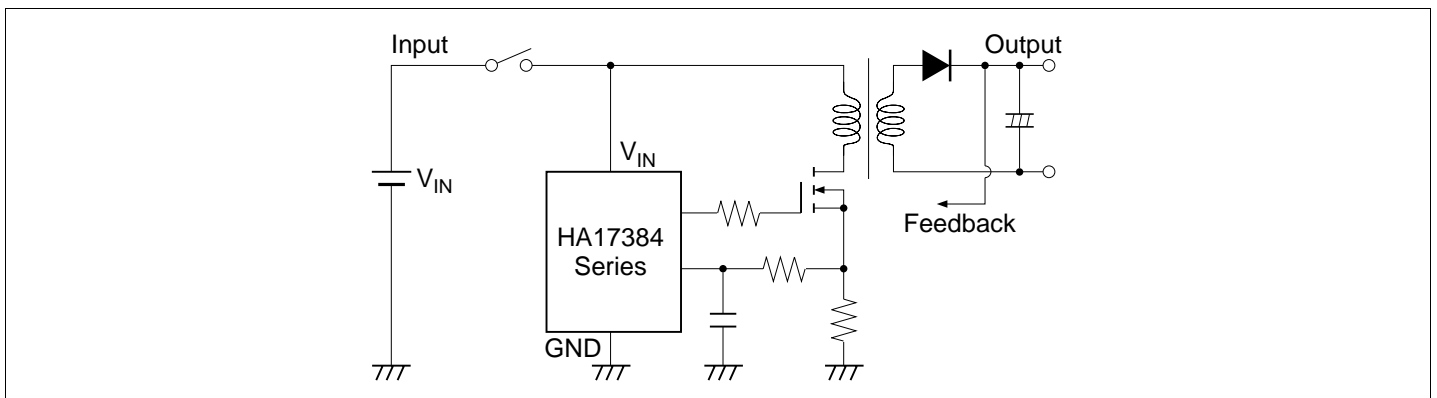
**Figure 16   Example of Circuit with Fast V_{IN} Rise Time**

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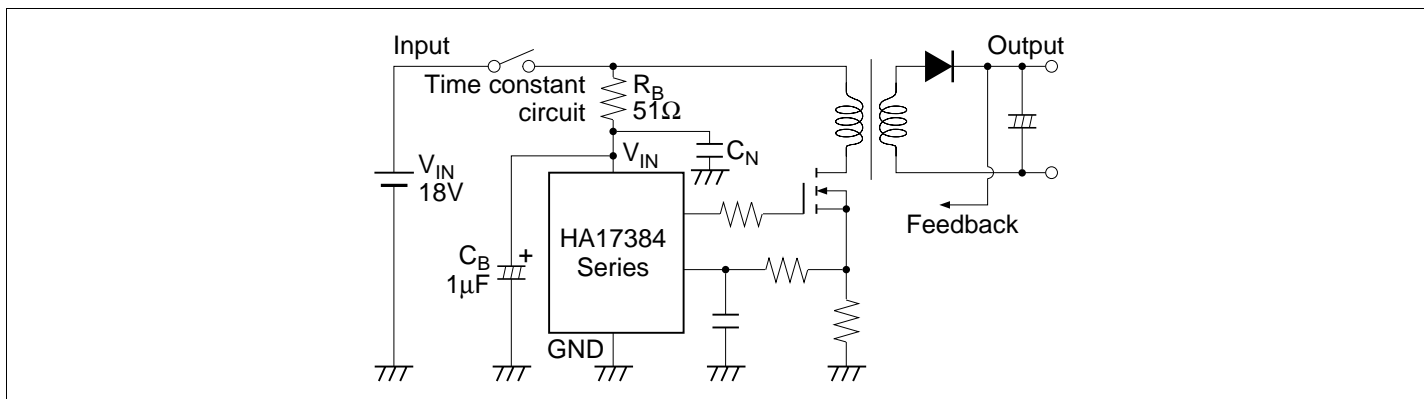
Figure 17   Sample Remedial Circuit

2. Externally Synchronized Operation

- Case

  When, with a power supply using the HA17384S/H or HA17385H, externally synchronized operation is performed by applying an external syncronous signal to the R_T/C_T pin (pin 4).

- Problem

  Synchronized operation may not be possible if the amplitude of the external syncronous signal is too large.

- Reason

  The R_T/C_T pin falls to a potential lower than the ground.

- Remedy (counter measure)

  In this case, clamping is necessary using a diode with as small a V_F value as possible, such as a schottky barrier diode, as shown in figure 18.
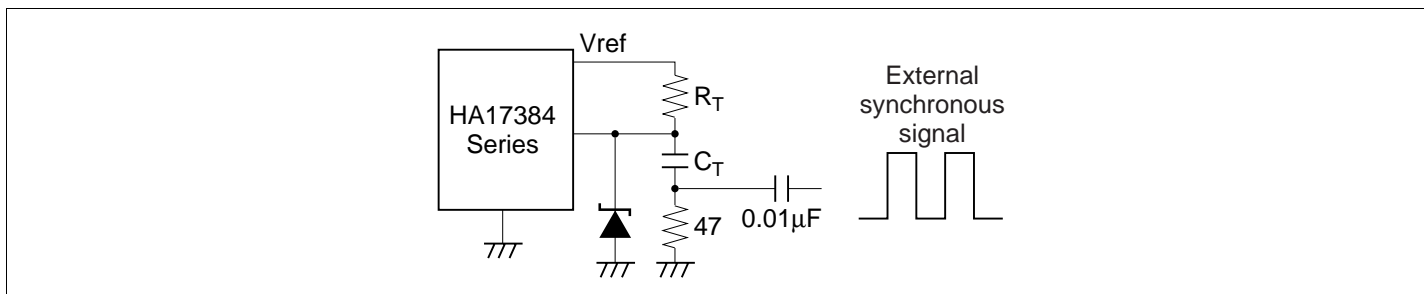
Figure 18   Sample Remedial Circuit

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HA17384SPS/SRP, HA17384HPS/HRP, HA17385HPS/HRP

Package Dimensions

Unit: mm
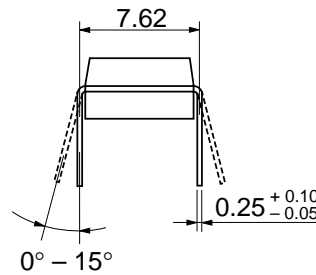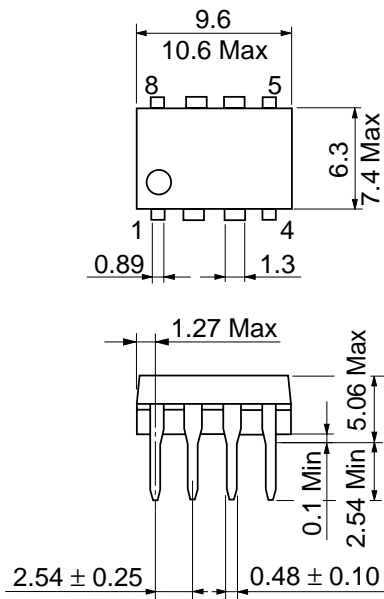
Hitachi Code	DP-8
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	0.54 g

9.6
10.6 Max
6.3
7.4 Max
0.89
1.3
1.27 Max
5.06 Max
0.1 Min
2.54 Min
2.54 ± 0.25
0.48 ± 0.10
7.62
0.25 $^{+0.10}_{-0.05}$
0° − 15°

Unit: mm

4.90
5.3 Max
3.95
0.75 Max
1.75 Max
1.27
0.14 $^{+0.11}_{-0.04}$
*0.42 ± 0.08
0.40 ± 0.06
0.15
0.25 Ⓜ
*0.22 ± 0.03
0.20 ± 0.03
6.10 $^{+0.10}_{-0.30}$
1.08
0° − 8°
0.60 $^{+0.67}_{-0.20}$
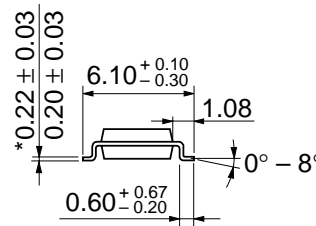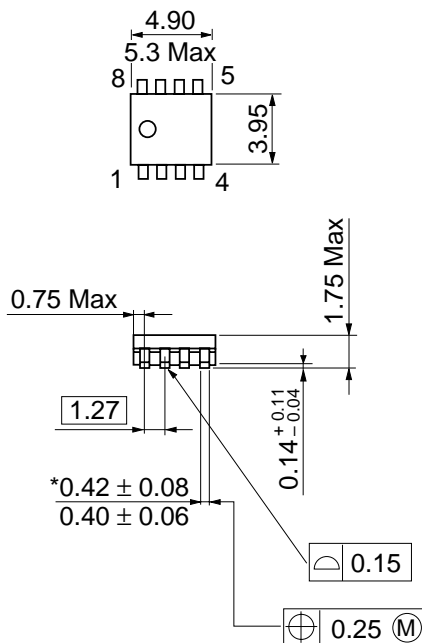
*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-8DC
JEDEC	Conforms
EIAJ	—
Mass (reference value)	0.085 g

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