16-bit Edge triggered D-type Flip Flops with 3-state Outputs

HITACHI

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Description

The HD74ALVCH162374 is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. It can be used as two 8-bit flip flops or one 16-bit flip flop. On the positive transition of the clock (CLK) input, the Q outputs of the flip flop take on the logic levels set up at the data (D) inputs.

The output enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high impedance state. In the high impedance state, the outputs neither load nor drive the bus lines significantly. The high impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components. \overline{OE} does not affect internal operations of the flip flops. Old data can be retained or new data can be entered while the outputs are in the high impedance state.

Active bus hold circuitry is provided to hold unused or floating data inputs at a valid logic level. All outputs, which are designed to sink up to 12 mA, include 26 Ω resistors to reduce overshoot and undershoot.

Features

- $V_{CC} = 2.3 \text{ V} \text{ to } 3.6 \text{ V}$
- Typical V_{OL} ground bounce < 0.8 V (@V_{CC} = 3.3 V, Ta = 25°C)
- Typical V_{OH} undershoot > 2.0 V (@V_{CC} = 3.3 V, Ta = 25°C)
- High output current $\pm 12 \text{ mA}$ (@V_{CC} = 3.0 V)
- Bus hold on data inputs eliminates the need for external pullup / pulldown resistors
- All outputs have equivalent 26 Ω series resistors, so no external resistors are required.



Function Table

| Inputs | | | Output Q |
|--------|------------|---|------------------------------|
| ŌE | CLK | D | |
| L | \uparrow | Н | Н |
| L | Ŷ | L | L |
| L | H or L | Х | Q ₀ ^{*1} |
| Н | Х | Х | Z |

H : High level

L : Low level

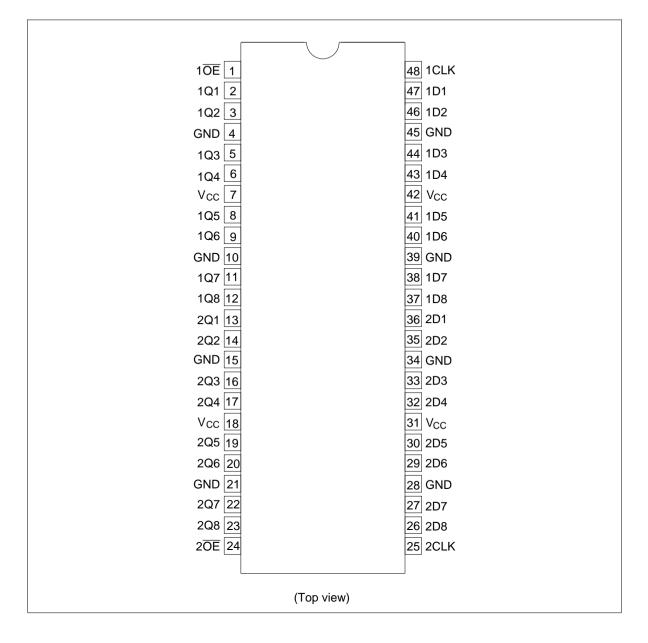
X : Immaterial

Z : High impedance

 \uparrow : Low to high transition

Note: 1. Output level before the indicated steady state input conditions were established.

Pin Arrangement



Absolute Maximum Ratings

| Item | Symbol | Ratings | Unit | Conditions | |
|---|-------------------------------|------------------------------|------|---|--|
| Supply voltage | V _{cc} | -0.5 to 4.6 | V | | |
| Input voltage ^{*1} | V | -0.5 to 4.6 | V | | |
| Output voltage *1, 2 | Vo | –0.5 to V _{cc} +0.5 | V | | |
| Input clamp current | I _{IK} | -50 | mA | V ₁ < 0 | |
| Output clamp current | Ι _{οκ} | ±50 | mA | $V_{\rm o}$ < 0 or $V_{\rm o}$ > $V_{\rm cc}$ | |
| Continuous output current | I _o | ±50 | mA | $V_o = 0$ to V_{cc} | |
| V _{cc} , GND current / pin | $I_{\rm CC}$ or $I_{\rm GND}$ | ±100 | mA | | |
| Maximum power dissipation at Ta = 55° C (in still air) ^{'3} | P _T | 0.85 | W | TSSOP | |
| Storage temperature | Tstg | -65 to 150 | °C | | |

Notes: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

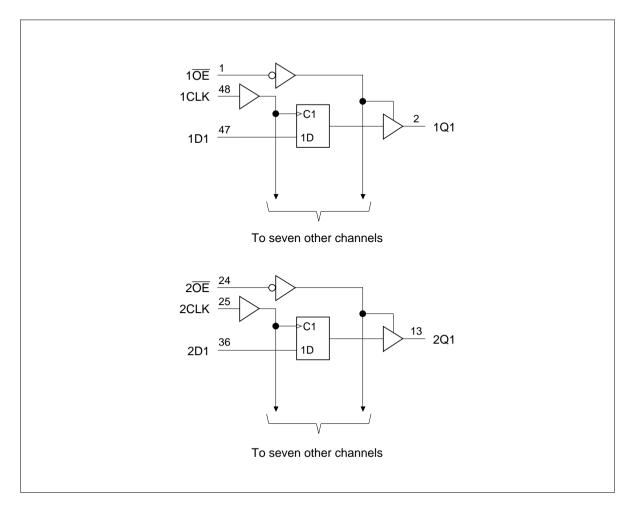
- 1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
- 2. This value is limited to 4.6 V maximum.
- 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

| Item | Symbol | Min | Мах | Unit | Conditions |
|------------------------------------|-----------------------|-----|-----------------|--------|-------------------------|
| Supply voltage | V _{cc} | 2.3 | 3.6 | V | |
| Input voltage | V | 0 | V _{cc} | V | |
| Output voltage | Vo | 0 | V _{cc} | V | |
| High level output current | I _{OH} | — | -6 | mA | $V_{cc} = 2.3 V$ |
| | | — | -8 | | $V_{cc} = 2.7 V$ |
| | | _ | -12 | | V _{cc} = 3.0 V |
| Low level output current | I _{ol} | — | 6 | mA | $V_{cc} = 2.3 V$ |
| | | _ | 8 | | $V_{cc} = 2.7 V$ |
| | | _ | 12 | | V _{cc} = 3.0 V |
| Input transition rise or fall rate | $\Delta t / \Delta v$ | 0 | 10 | ns / V | |
| Operating temperature | Та | -40 | 85 | °C | |

Recommended Operating Conditions

Note: Unused control inputs must be held high or low to prevent them from floating.

Logic Diagram



| Item | Symbol | V _{cc} (V) | Min | Max | Unit | Test Conditions |
|--------------------------|-----------------|---------------------|----------------------|------|------|--|
| Input voltage | V _{IH} | 2.3 to 2.7 | 1.7 | _ | V | |
| | | 2.7 to 3.6 | 2.0 | _ | = | |
| | V _{IL} | 2.3 to 2.7 | | 0.7 | - | |
| | | 2.7 to 3.6 | _ | 0.8 | - | |
| Output voltage | V _{OH} | Min to Max | V _{cc} -0.2 | _ | V | I _{OH} = -100 μA |
| | | 2.3 | 1.9 | _ | - | $I_{OH} = -4 \text{ mA}, V_{IH} = 1.7 \text{ V}$ |
| | | 2.3 | 1.7 | _ | = | $I_{OH} = -6 \text{ mA}, V_{IH} = 1.7 \text{ V}$ |
| | | 3.0 | 2.4 | _ | = | $I_{_{OH}} = -6 \text{ mA}, V_{_{IH}} = 2.0 \text{ V}$ |
| | | 2.7 | 2.0 | _ | = | $I_{OH} = -8 \text{ mA}, V_{IH} = 2.0 \text{ V}$ |
| | | 3.0 | 2.0 | _ | - | $I_{OH} = -12 \text{ mA}, V_{IH} = 2.0 \text{ V}$ |
| | V _{OL} | Min to Max | _ | 0.2 | - | I _{oL} = 100 μA |
| | | 2.3 | _ | 0.4 | - | $I_{oL} = 4 \text{ mA}, V_{IL} = 0.7 \text{ V}$ |
| | | 2.3 | _ | 0.55 | - | $I_{oL} = 6 \text{ mA}, V_{IL} = 0.7 \text{ V}$ |
| | | 3.0 | _ | 0.55 | = | $I_{ol} = 6 \text{ mA}, V_{ll} = 0.8 \text{ V}$ |
| | | 2.7 | _ | 0.6 | = | $I_{oL} = 8 \text{ mA}, V_{IL} = 0.8 \text{ V}$ |
| | | 3.0 | _ | 0.8 | - | $I_{oL} = 12 \text{ mA}, V_{IL} = 0.8 \text{ V}$ |
| Input current | I _{IN} | 3.6 | | ±5 | μΑ | $V_{IN} = V_{CC}$ or GND |
| | I IN (hold) | 2.3 | 45 | — | = | V _{IN} = 0.7 V |
| | | 2.3 | -45 | _ | - | V _{IN} = 1.7 V |
| | | 3.0 | 75 | _ | = | V _{IN} = 0.8 V |
| | | 3.0 | -75 | — | = | V _{IN} = 2.0 V |
| | | 3.6 | | ±500 | - | $V_{IN} = 0$ to 3.6 V ^{*1} |
| Off state output current | I _{oz} | 3.6 | | ±10 | μΑ | $V_{OUT} = V_{CC}$ or GND |
| Quiescent supply current | I _{cc} | 3.6 | _ | 40 | μΑ | $V_{IN} = V_{CC}$ or GND |
| | ΔI_{cc} | 3.0 to 3.6 | _ | 750 | μΑ | V_{IN} = one input at (V _{cc} -0.6) V, other inputs at V _{cc} or GND |

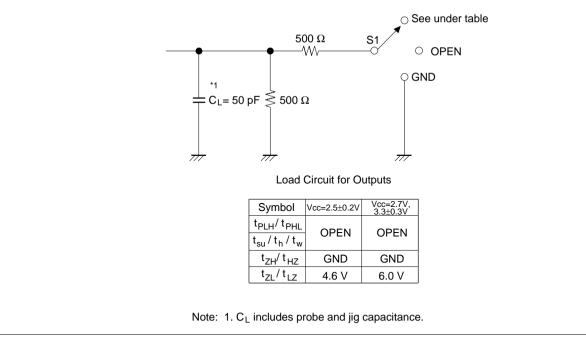
Electrical Characteristics (Ta = -40 to 85° C)

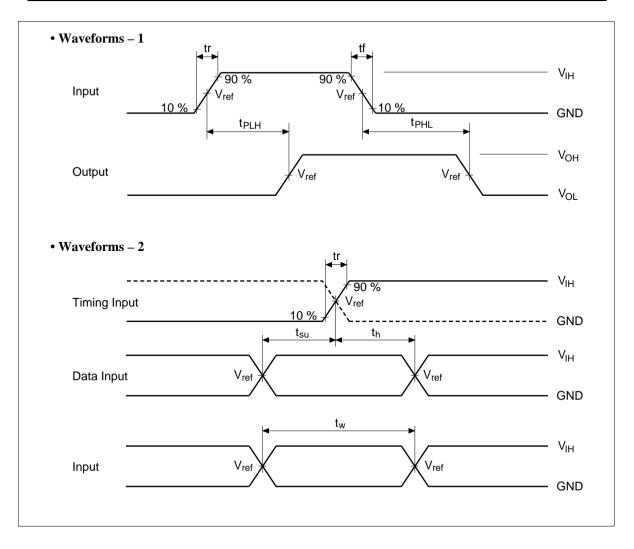
Note: 1. This is the bus hold maximum dynamic current required to switch the input from one state to another.

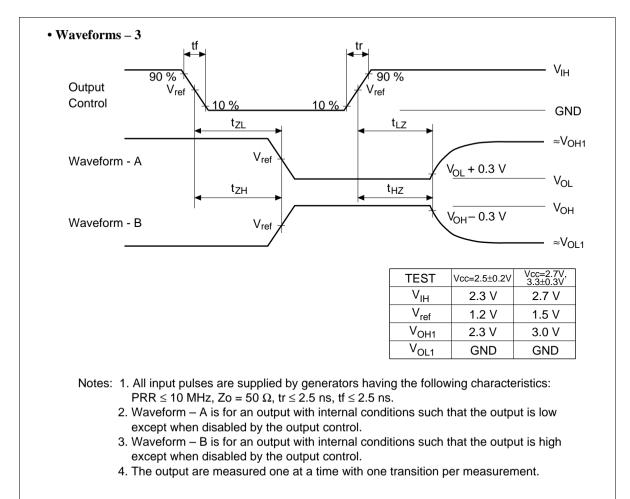
| Item | Symbol | V _{cc} (V) | Min | Тур | Max | Unit | FROM (Input) | TO (Output) |
|-------------------------|--------------------|---------------------|-----|-----|-----|------|-----------------|----------------|
| Maximum clock frequency | f _{max} | 2.5±0.2 | 150 | | | MHz | | |
| | | 2.7 | 150 | _ | — | | | |
| | | 3.3±0.3 | 150 | | _ | | | |
| Propagation delay time | \mathbf{t}_{PLH} | 2.5±0.2 | 1.0 | _ | 5.4 | ns | CLK | Q |
| | t _{PHL} | 2.7 | _ | _ | 5.4 | | | |
| | | 3.3±0.3 | 1.0 | — | 4.6 | | | |
| Output enable time | t _{zH} | 2.5±0.2 | 1.0 | _ | 6.5 | ns | ŌĒ | Q |
| | t _{zL} | 2.7 | _ | _ | 6.4 | | | |
| | | 3.3±0.3 | 1.0 | _ | 5.2 | | | |
| Output disable time | t _{HZ} | 2.5±0.2 | 1.0 | _ | 5.6 | ns | ŌĒ | Q |
| | t _{LZ} | 2.7 | _ | _ | 5.0 | | | |
| | | 3.3±0.3 | 1.2 | _ | 4.5 | | | |
| Setup time | t _{su} | 2.5±0.2 | 2.1 | _ | _ | ns | | |
| | | 2.7 | 2.2 | — | — | | | |
| | | 3.3±0.3 | 1.9 | _ | _ | | | |
| Hold time | t _h | 2.5±0.2 | 0.6 | _ | _ | ns | | |
| | | 2.7 | 0.5 | _ | _ | | | |
| | | 3.3±0.3 | 0.5 | | _ | | | |
| Pulse width | t _w | 2.5±0.2 | 3.3 | _ | _ | ns | | |
| | | 2.7 | 3.3 | | | _ | | |
| | | 3.3±0.3 | 3.3 | _ | _ | | | |
| Input capacitance | CIN | 3.3 | _ | 3.0 | _ | pF | Control in | puts |
| | | 3.3 | _ | 6.0 | _ | | Data inpu | ts |
| Output capacitance | Co | 3.3 | _ | 7.0 | _ | pF | | |

Switching Characteristics (Ta = -40 to 85° C)



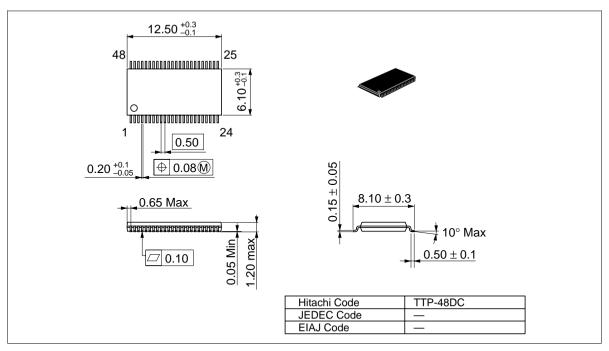






Package Dimensions

Unit : mm



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