

# HD14557B

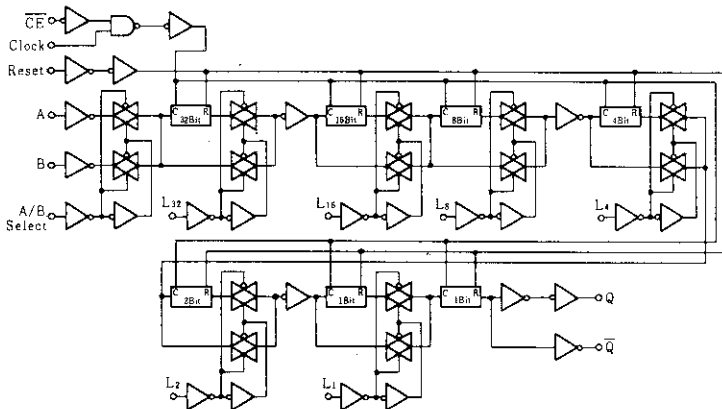
## 1-to-64-bit Variable Length Shift Register

The HD14557B is a static clocked serial shift register whose length may be programmed to be any number of bits between 1 and 64. The number of bits selected is equal to the sum of the subscripts of the enabled Length Control inputs (L1, L2, L4, L8, L16 and L32) plus one. Serial data may be selected from the A or B data inputs with the A/B select input. This feature is useful for recirculation purposes. A Clock Enable (CE) input is provided to allow gating of the clock or negative edge clocking capability.

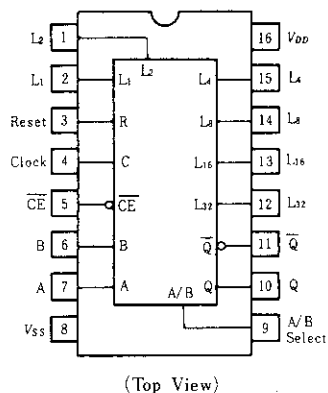
### FEATURES

- Quiescent Current = 10nA/pkg typ. @5V
- 1-64 Bit Programmable Length
- Q and  $\bar{Q}$  Serial Buffered Outputs
- Asynchronous Master Reset
- All Inputs Buffered
- No Limit On Clock Rise and Fall Times
- 8MHz Operation @10V
- Supply Voltage Range = 3 to 18V
- Capable of Driving One Low-power Schottky TTL Load Over the Rated Temperature Range

### LOGIC DIAGRAM



### PIN ARRANGEMENT



### TRUTH TABLE

Inputs				Outputs
R	A/B	C	$\overline{CE}$	Q
0	0		0	B
0	1		0	A
0	0	1		B
0	1	1		A
1	x	x	x	0

Note: Q is the output of the first selected shift register stage.  
x = Don't Care

■ LENGTH SELECT TRUTH TABLE

L <sub>32</sub>	L <sub>16</sub>	L <sub>8</sub>	L <sub>4</sub>	L <sub>2</sub>	L <sub>1</sub>	Register Length
0	0	0	0	0	0	1-bit
0	0	0	0	0	1	2-bit
0	0	0	0	1	0	3-bit
0	0	0	0	1	1	4-bit
0	0	0	1	0	0	5-bit
0	0	0	1	0	1	6-bit
⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	0	0	0	0	0	33-bit
1	0	0	0	0	1	34-bit
⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	0	0	61-bit
1	1	1	1	0	1	62-bit
1	1	1	1	1	0	63-bit
1	1	1	1	1	1	64-bit

■ ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V <sub>DD</sub> (V)	Test Conditions	-40°C		25°C			85°C		Unit
				min	max	min	typ	max	min	max	
Output Voltage	V <sub>OL</sub>	5.0	V <sub>in</sub> = V <sub>DD</sub> or 0	—	0.05	—	0	0.05	—	0.05	V
		10		—	0.05	—	0	0.05	—	0.05	
		15		—	0.05	—	0	0.05	—	0.05	
	V <sub>OH</sub>	5.0	V <sub>in</sub> = 0 or V <sub>DD</sub>	4.95	—	4.95	5.0	—	4.95	—	V
		10		9.95	—	9.95	10	—	9.95	—	
		15		14.95	—	14.95	15	—	14.95	—	
Input Voltage	V <sub>IL</sub>	5.0	V <sub>out</sub> = 4.5 or 0.5V	—	1.5	—	2.25	1.5	—	1.5	V
		10	V <sub>out</sub> = 9.0 or 1.0V	—	3.0	—	4.50	3.0	—	3.0	
		15	V <sub>out</sub> = 13.5 or 1.5V	—	4.0	—	6.75	4.0	—	4.0	
	V <sub>IH</sub>	5.0	V <sub>out</sub> = 0.5 or 4.5V	3.5	—	3.5	2.75	—	3.5	—	V
		10	V <sub>out</sub> = 1.0 or 9.0V	7.0	—	7.0	5.50	—	7.0	—	
		15	V <sub>out</sub> = 1.5 or 13.5V	11.0	—	11.0	8.25	—	11.0	—	
Output Drive Current	I <sub>OH</sub>	5.0	V <sub>OH</sub> = 2.5V	-1.0	—	-0.8	-1.7	—	-0.6	—	mA
		5.0	V <sub>OH</sub> = 4.6V	-0.2	—	-0.16	-0.36	—	-0.12	—	
		10	V <sub>OH</sub> = 9.5V	-0.5	—	-0.4	-0.9	—	-0.3	—	
		15	V <sub>OH</sub> = 13.5V	-1.4	—	-1.2	-3.5	—	-1.0	—	
	I <sub>OL</sub>	5.0	V <sub>OL</sub> = 0.4V	0.52	—	0.44	0.88	—	0.36	—	mA
		10	V <sub>OL</sub> = 0.5V	1.3	—	1.1	2.25	—	0.9	—	
15		V <sub>OL</sub> = 1.5V	3.6	—	3.0	8.8	—	2.4	—		
Input Current	I <sub>in</sub>	15		—	±0.3	—	±0.0001	±0.3	—	±1.0	μA
Input Capacitance	C <sub>in</sub>		V <sub>in</sub> = 0	—	—	—	5.0	7.5	—	—	pF
Quiescent Current	I <sub>DD</sub>	5.0	Zero Signal, per Package	—	50	—	0.010	50	—	375	μA
		10		—	100	—	0.020	100	—	750	
		15		—	200	—	0.030	200	—	1500	
Total Supply Current*	I <sub>T</sub>	5.0	Dynamic + I <sub>DD</sub> , per Gate, C <sub>L</sub> = 50pF, f = 1 kHz	—	—	—	1.75	—	—	—	μA
		10		—	—	—	3.5	—	—	—	
		15		—	—	—	5.25	—	—	—	

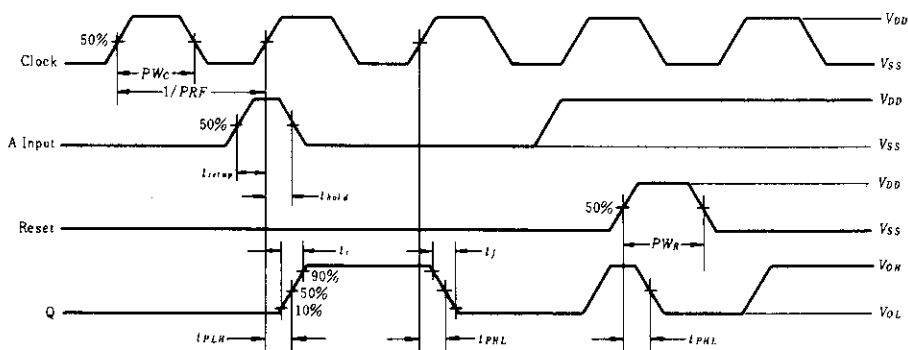
\* To calculate total supply current at frequency other than 1kHz.

@V<sub>DD</sub> = 5.0V I<sub>T</sub> = (1.75 μA/kHz)f + I<sub>DD</sub>, @V<sub>DD</sub> = 10V I<sub>T</sub> = (3.5 μA/kHz)f + I<sub>DD</sub>, @V<sub>DD</sub> = 15V I<sub>T</sub> = (5.25 μA/kHz)f + I<sub>DD</sub>

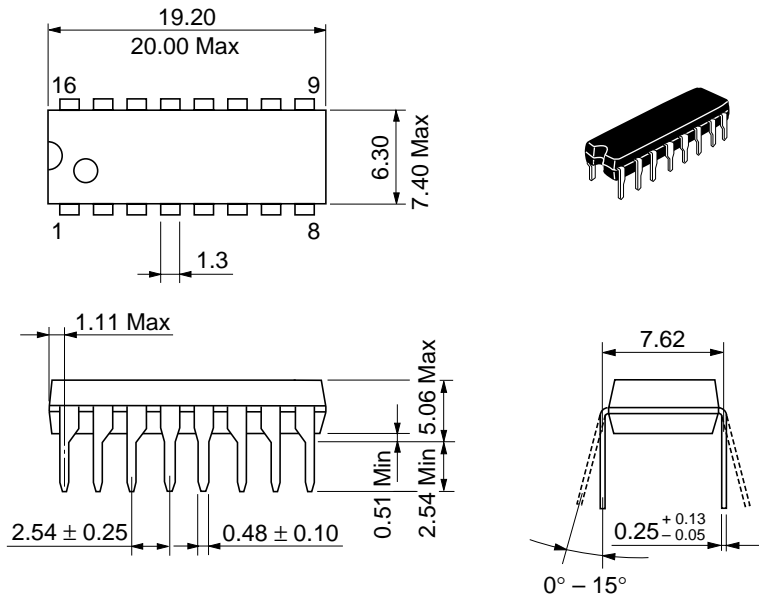
■ SWITCHING CHARACTERISTICS ( $C_L=50\text{pF}$ ,  $T_a=25^\circ\text{C}$ )

Characteristic		Symbol	$V_{DD}(\text{V})$	min	typ	max	Unit
Output Rise Time		$t_r$	5.0	—	180	400	ns
			10	—	90	200	
			15	—	65	100	
Output Fall Time		$t_f$	5.0	—	100	200	ns
			10	—	50	100	
			15	—	37	80	
Propagation Delay Time	C, $\overline{\text{CE}}$ to Q, $\overline{\text{Q}}$	$t_{PLH}$ , $t_{PHL}$	5.0	—	500	1250	ns
			10	—	200	500	
	15	—	150	375			
	R to Q, $\overline{\text{Q}}$	5.0	—	475	1190		
		10	—	190	475		
			15	—	140	350	
Clock Pulse Width		$PW_C$	5.0	660	220	—	ns
			10	200	68	—	
			15	150	50	—	
Reset Pulse Width		$PW_R$	5.0	900	300	—	ns
			10	270	90	—	
			15	180	60	—	
Clock Frequency		$PRF$	5.0	—	2.5	0.83	MHz
			10	—	8.0	2.7	
			15	—	10.5	3.3	
Clock Pulse Rise and Fall Time		$t_r, t_f$	5.0	No Limit			
			10				
			15				
Setup Time		$t_{setup}$	5.0	1350	450	—	ns
			10	540	180	—	
			15	400	135	—	
Hold Time		$t_{hold}$	5.0	-150	-450	—	ns
			10	-60	-180	—	
			15	-45	-135	—	

● TIMING DIAGRAM



Note) 1-bit length;  $\overline{\text{CE}}=0$ , A/B=1, L<sub>1</sub>=L<sub>2</sub>=L<sub>4</sub>=L<sub>5</sub>=L<sub>16</sub>=L<sub>32</sub>=0



Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g

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