Octal Bus Transceivers/Registers (with inverted 3-state outputs) Octal Bus Transceivers/Registers (with 3-state outputs)

HITACHI

Description

This device consists of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Enable GAB and $\overline{\text{GBA}}$ are provided to cotrol the transceiver functions. Select AB and Select BA control pins are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high selects stored data. The following examples demonstrate the four fundamental bus-management functions that can be performed with the HD74HC651 and HD74HC652.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to high transition at the appropriate clock pins (Clock AB or Clock BA) regardless of the select or enable control pins. When Select AB and Select BA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling Enable GAB and \overline{GBA} . In this configuration each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

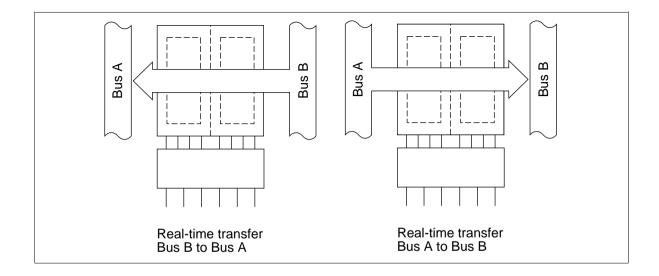
Features

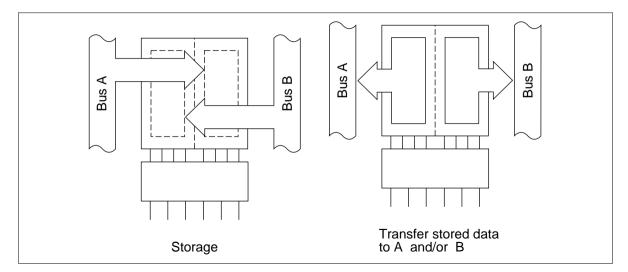
- High Speed Operation: t_{pd} (Bus to Bus) = 16 ns typ ($C_L = 50 \text{ pF}$)
- High Output Current: Fanout of 15 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 2 \text{ to } 6 \text{ V}$
- Low Input Current: 1 µA max
- Low Quiescent Supply Current: I_{CC} (static) = 4 μ A max (Ta = 25°C)



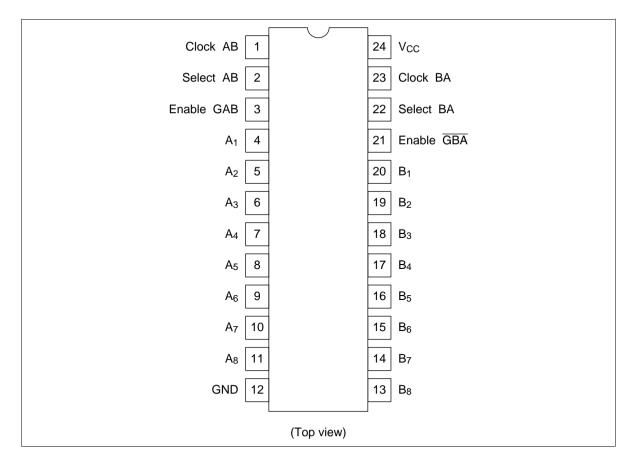
Function Table

	Real-Time Transfer Bus B to Bus A	Real-Time Transfer Bus A to Bus B	Storage	Transfer Stored Data to A and/or B
Clock AB	Х	Х		L or H
Select AB	Х	L	Х	Н
Enable GAB	L	Н	L	Н
Clock BA	Х	Х		L or H
Select BA	L	Х	Х	Н
Enable GBA	L	Н	Н	L





Pin Arrangement

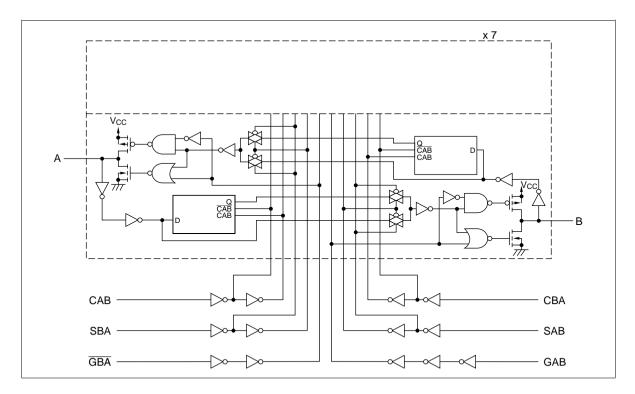


Absolute Maximum Ratings

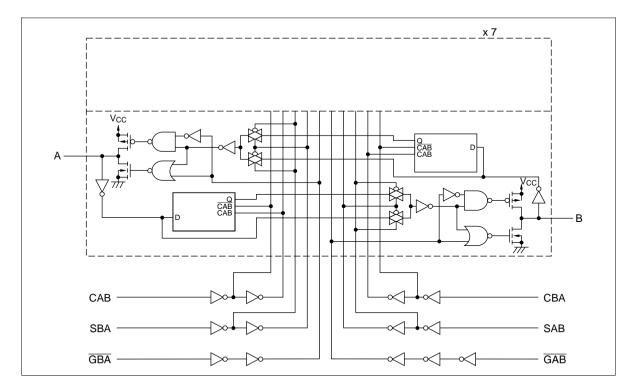
Item	Symbol	Rating	Unit
Supply voltage range	V _{cc}	-0.5 to +7.0	V
Input voltage	V _{IN}	–0.5 to V_{cc} + 0.5	V
Output voltage	V _{OUT}	–0.5 to V _{cc} + 0.5	V
Output current	I _{OUT}	±35	mA
DC current drain per V_{cc} , GND	I _{cc} , I _{gnd}	±75	mA
DC input diode current	l _{ik}	±20	mA
DC output diode current	Ι _{οκ}	±20	mA
Power Dissipation per package	Ρ _τ	500	mW
Storage temperature	Tstg	-65 to +150	٥C

Logic Diagram

HD74HC651



HD74HC652



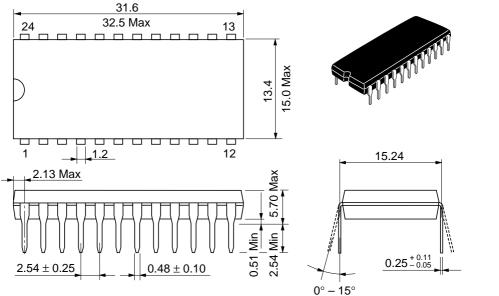
DC Characteristics

			Ta =	: 25°C	;	Ta = - +85°C	–40 to C			
Item	Symbol	V _{cc} (V)	Min	Тур	Мах	Min	Мах	Unit	Test Condition	าร
Input voltage	V _{IH}	2.0	1.5	_	_	1.5	_	V		
		4.5	3.15	_	_	3.15	_	_		
		6.0	4.2	_	_	4.2	_			
	V _{IL}	2.0	—	—	0.5	—	0.5	V		
		4.5	_	_	1.35	—	1.35	_		
		6.0	_	_	1.8	—	1.8	_		
Output voltage	V _{OH}	2.0	1.9	2.0	—	1.9	—	V	$Vin = V_{IH} \text{ or } V_{IL}$	I _{OH} = -20 μA
		4.5	4.4	4.5	_	4.4	_			
		6.0	5.9	6.0	—	5.9	—	_		
		4.5	4.18	—	—	4.13	—			I _{он} = —6 mA
		6.0	5.68	_	—	5.63	—	_		I _{OH} = -7.8 mA
	V _{OL}	2.0	_	0.0	0.1	—	0.1	V	$Vin = V_{IH} \text{ or } V_{IL}$	I _{oL} = 20 μA
		4.5	—	0.0	0.1	—	0.1	_		
		6.0		0.0	0.1	—	0.1	_		
		4.5			0.26	—	0.33	_		I _{oL} = 6 mA
		6.0	—	—	0.26	—	0.33			I _{oL} = 7.8 mA
Off-state output current	I _{oz}	6.0	_	_	±0.5	_	±5.0	μA	$Vin = V_{IH} \text{ or } V_{IL},$ Vout = V _{CC} or C	
Input current	lin	6.0		_	±0.1	_	±1.0	μA	$Vin = V_{CC} \text{ or } GN$	ND
Quiescent supply current	I _{cc}	6.0	—	—	4.0	—	40	μA	Vin = V _{cc} or GN	ND, lout = $0 \mu A$

AC Characteristics ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

			Ta =	: 25°C	2	Ta = - +85°0	–40 to C		
Item	Symbol	V _{cc} (V)	Min	Тур	Мах	Min	Max	Unit	Test Conditions
Propagation delay	t _{PLH}	2.0	_		170		215	ns	Clock to Bus
time	t _{PHL}	4.5	_	19	34	_	43	-	
		6.0		_	29	_	37	-	
		2.0	_	_	135	_	170	ns	Bus to Bus
		4.5	—	16	27	_	34	_	
		6.0	_	_	23		29	-	
		2.0	_	_	190	_	240	ns	Select to Bus
		4.5	_	18	38	_	48	_	
		6.0	_	_	32	_	41	-	
Output enable	t _{zL}	2.0		—	150	_	190	ns	
time	t _{zH}	4.5		14	30	_	38	_	
		6.0	—	_	26	_	33	_	
Output disable	t _{LZ}	2.0	_	—	150	—	190	ns	
time	\mathbf{t}_{HZ}	4.5		18	30	_	38	_	
		6.0	—	_	26	_	33	_	
Pulse width	t _w	2.0	80	—		100	_	ns	
		4.5	16	7		20	_	_	
		6.0	14	_		17	_	_	
Setup time	t _{su}	2.0	100	_		125	_	ns	
		4.5	20	4	_	25		_	
		6.0	17	_		21	_	_	
Hold time	t _h	2.0	5	_	_	5		ns	
		4.5	5	-1	_	5	_	_	
		6.0	5	_	_	5	_	-	
Output rise/fall	t _{TLH}	2.0	_	_	60	_	75	ns	
time	t_{THL}	4.5		4	12	—	15	_	
		6.0	_	_	10		13	-	
Input capacitance	Cin	_		5	10	_	10	pF	

Unit: mm



Hi	itachi Code	DP-24
JE	EDEC	Conforms
EI	AJ	Conforms
W	eight (reference value)	3.1 g

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Semiconductor & Integrated Circuits. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109 NorthAmerica URL http:semiconductor.hitachi.com/ http://www.hitachi-eu.com/hel/ecg Europe http://www.has.hitachi.com.sg/grp3/sicd/index.htm http://www.hitachi.com.tw/E/Product/SICD_Frame.htm Asia (Singapore) Asia (Taiwan) Asia (HongKong) http://www.hitachi.com.hk/eng/bo/grp3/index.htm http://www.hitachi.co.jp/Sicd/indx.htm Japan For further information write to: Hitachi Semiconductor Hitachi Europe GmbH Hitachi Asia Pte. Ltd. (America) Inc. Electronic components Group 16 Collyer Quay #20-00 179 East Tasman Drive, Dornacher Stra§e 3 Hitachi Tower San Jose,CA 95134 D-85622 Feldkirchen, Munich Singapore 049318 Tel: <1> (408) 433-1990 Fax: <1>(408) 433-0223 Germany Tel: 535-2100 Tel: <49> (89) 9 9180-0 Fax: 535-1533 Fax: <49> (89) 9 29 30 00

 Fax: <49> (89) 9 29 30 00
 Hita

 Hitachi Europe Ltd.
 Hita

 Electronic Components Group.
 Taip

 Whitebrook Park
 3F,

 Lower Cookham Road
 Tun

 Maidenhead
 Tel:

 Berkshire SL6 8YA, United Kingdom
 Fax

 Tel: <44> (1628) 585000

 Fax: <44> (1628) 778322

Hitachi Asia Ltd. Taipei Branch Office 3F, Hung Kuo Building. No.167, Tun-Hwa North Road, Taipei (105) Tel: <886> (2) 2718-3666 Fax: <886> (2) 2718-8180

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Hitachi Asia (Hong Kong) Ltd. Group III (Electronic Components) 7/F., North Tower, World Finance Centre, Harbour City, Canton Road, Tsim Sha Tsui, Kowloon, Hong Kong Tel: <852> (2) 735 9218 Fax: <852> (2) 730 0281 Telex: 40815 HITEC HX

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