HD74HC670

4-by-4 Register File (with 3-state outputs)

HITACHI

Description

The HD74HC670, 16-bit register file is organized as 4 words of 4 bits each and separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data.

This permits simultaneous writing into one location and reading from another word location. Four data inputs are available which are used to supply the 4-bit word to be stored. Location of the word is determined by the write-address inputs A and B in conjunction with a write-enable signal. Data applied at the inputs should be in its true form. That is, if a high-level signal is desired from the output, a high-level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at the D input is transferred to the latch output. When the write-enable input, (G_W) is high, the data inputs are inhibited and their levels can cuase no change in the information stored in the internal latches. When the read-enable input, (G_R) is high, the data outputs are inhibited and go into the high-impedance state. The individual address lines permit direct acquisition of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word. when the read address is made in conjunction with the read-enable signal, the word appears at the four outputs.

Features

- High Speed Operation: t_{pd} (Read Select to Q) = 21 ns typ (C_L = 50 pF)
- High Output Current: Fanout of 15 LSTTL Loads
- Wide Operating Voltage: V_{CC} = 2 to 6 V
- Low Input Current: 1 µA max
- Low Quiescent Supply Current: I_{CC} (static) = 4 µA max (Ta = 25°C)

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Function Table

Write Inputs			Word			
W_B	W_A	G_W	0	1	2	3
L	L	L	Q = D	Q_0	Q_0	Q_0
L	H	L	Q_0	Q = D	Q_0	Q_0
H	L	L	Q_0	Q_0	Q = D	Q_0
H	H	L	Q_0	Q_0	Q_0	Q = D
X	X	H	Q_0	Q_0	Q_0	Q_0

Read Inputs			Outputs			
R_B	R_A	G_R	Q_1	Q_2	Q_3	Q_4
L	L	L	$W_0 B_1$	$W_0 B_2$	$W_0 B_3$	$W_0 B_4$
L	H	L	$W_1 B_1$	$W_1 B_2$	$W_1 B_3$	$W_1 B_4$
H	L	L	$W_2 B_1$	$W_2 B_2$	$W_2 B_3$	$W_2 B_4$
H	H	L	$W_3 B_1$	$W_3 B_2$	$W_3 B_3$	$W_3 B_4$
X	X	H	Z	Z	Z	Z

H : high level

L : low level

X : irrelevant

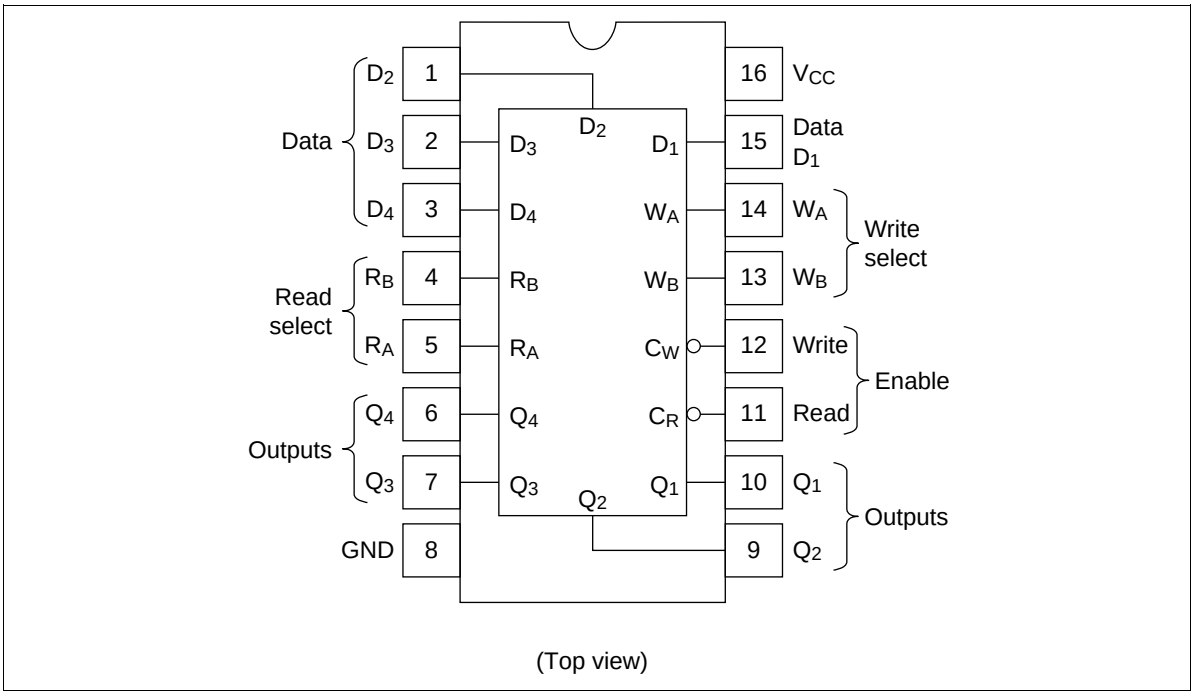
Z : high impedance (off)

(Q = D) : The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.

Q_0 : The level of Q before the indicated input conditions were established.

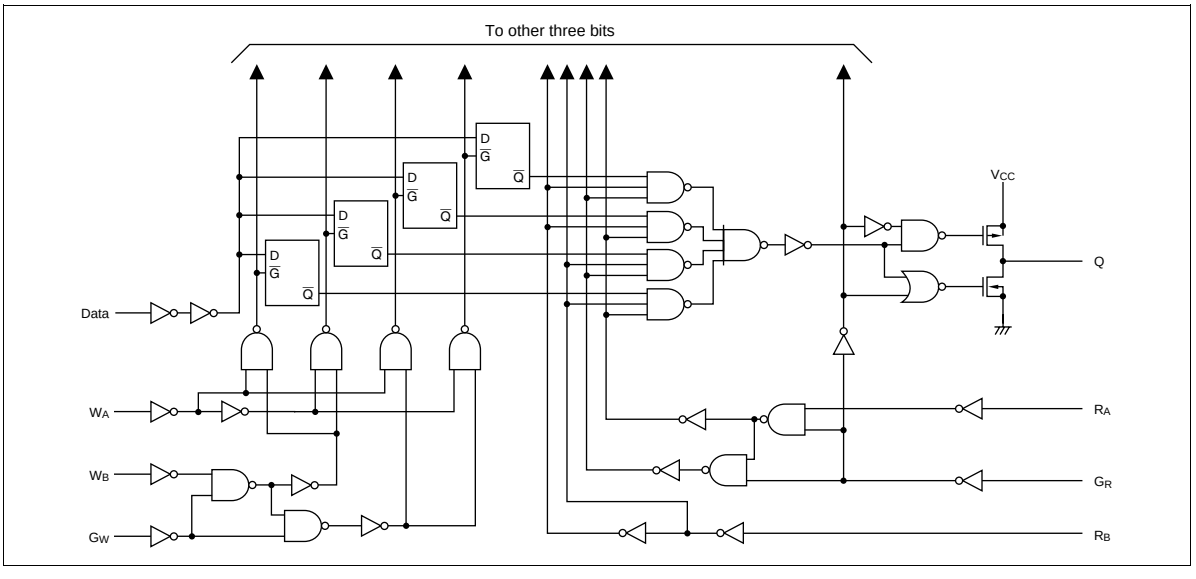
$W_0 B_1$: The first bit of word 0, etc.

Pin Arrangement



(Top view)

Logic Diagram



DC Characteristics

Item	Symbol	V_{CC} (V)	Ta = 25°C Min	Typ	Max	Ta = –40 to +85°C Min	Max	Unit	Test Conditions	
Input voltage	V_{IH}	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	V_{IL}	2.0	—	—	0.5	—	0.5	V		
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	V_{OH}	2.0	1.9	2.0	—	1.9	—	V	Vin = V_{IH} or V_{IL}	I_{OH} = –20 µA
		4.5	4.4	4.5	—	4.4	—			
		6.0	5.9	6.0	—	5.9	—			
		4.5	4.18	—	—	4.13	—			I_{OH} = –6 mA
		6.0	5.68	—	—	5.63	—			I_{OH} = –7.8 mA
	V_{OL}	2.0	—	0.0	0.1	—	0.1	V	Vin = V_{IH} or V_{IL}	I_{OL} = 20 µA
		4.5	—	0.0	0.1	—	0.1			
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	—	0.26	—	0.33			I_{OL} = 6 mA
		6.0	—	—	0.26	—	0.33			I_{OL} = 7.8 mA
Off-state output current	I_{OZ}	6.0	—	—	±0.5	—	±5.0	µA	Vin = V_{IN} or V_{IL}, Vout = V_{CC} or GND	
Input current	Iin	6.0	—	—	±0.1	—	±1.0	µA	Vin = V_{CC} or GND	
Quiescent supply current	I_{CC}	6.0	—	—	4.0	—	40	µA	Vin = V_{CC} or GND, Iout = 0 µA	

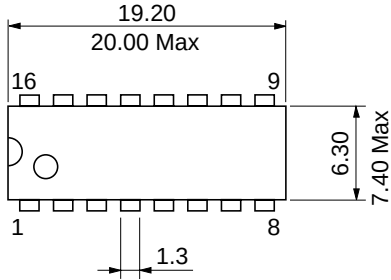
AC Characteristics (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

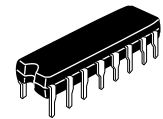
			Ta = 25°C			Ta = –40 to +85°C			
Item	**Symbol**	**V_{cc} (V)**	**Min**	**Typ**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Propagation delay time	t_{PLH}	2.0	—	—	160	—	200	ns	Read select to Q
	t_{PHL}	4.5	—	21	32	—	40		
		6.0	—	—	27	—	34		
	t_{PLH}	2.0	—	—	200	—	250	ns	Write enable to Q
	t_{PHL}	4.5	—	24	40	—	50		
		6.0	—	—	34	—	43		
	t_{PLH}	2.0	—	—	150	—	190	ns	Data to Q
	t_{PHL}	4.5	—	18	30	—	38		
		6.0	—	—	26	—	33		
Output enable time	t_{ZH}	2.0	—	—	150	—	190	ns	
	t_{ZL}	4.5	—	18	30	—	38		
		6.0	—	—	26	—	33		
Output disable time	t_{HZ}	2.0	—	—	150	—	190	ns	
	t_{LZ}	4.5	—	17	30	—	38		
		6.0	—	—	26	—	33		
Pulse width	t_w	2.0	80	—	—	100	—	ns	
		4.5	16	—	—	20	—		
		6.0	14	—	—	17	—		
Setup time	t_{su}	2.0	60	—	—	75	—	ns	Data to Write enable
		4.5	12	4	—	15	—		
		6.0	10	—	—	13	—		
	t_{su}	2.0	60	—	—	75	—	ns	Write select to Write enable
		4.5	12	—	—	15	—		
		6.0	10	—	—	13	—		
Hold time	t_h	2.0	50	—	—	63	—	ns	Write enable to Data
		4.5	10	6	—	13	—		
		6.0	9	—	—	11	—		
		2.0	50	—	—	63	—	ns	Write enable to Write select
		4.5	10	—	—	13	—		
		6.0	9	—	—	11	—		

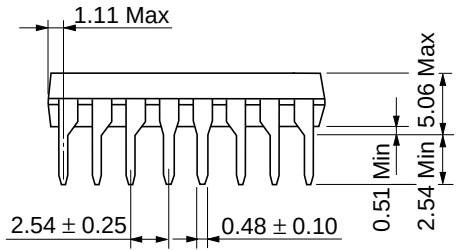
AC Characteristics (C_L = 50 pF, Input t_r = t_f = 6 ns) (cont)

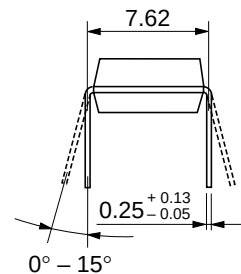
			Ta = 25°C			Ta = –40 to +85°C			
Item	**Symbol**	**V_{CC} (V)**	**Min**	**Typ**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Latch time for new	t_{latch}	2.5	100	—	—	125	—	ns	
data		4.5	20	—	—	25	—		
		6.0	17	—	—	21	—		
Output rise/fall	t_{TLH}	2.0	—	—	75	—	95	ns	
time	t_{THL}	4.5	—	5	15	—	19		
		6.0	—	—	13	—	16		
Input capacitance	Cin	—	—	5	10	—	10	pF	

Unit: mm



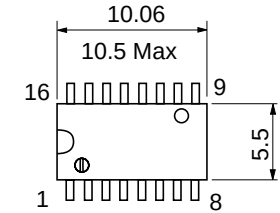


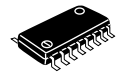


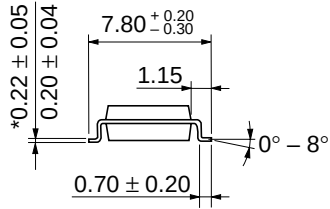


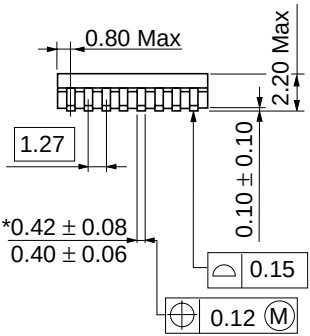
Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g

Unit: mm





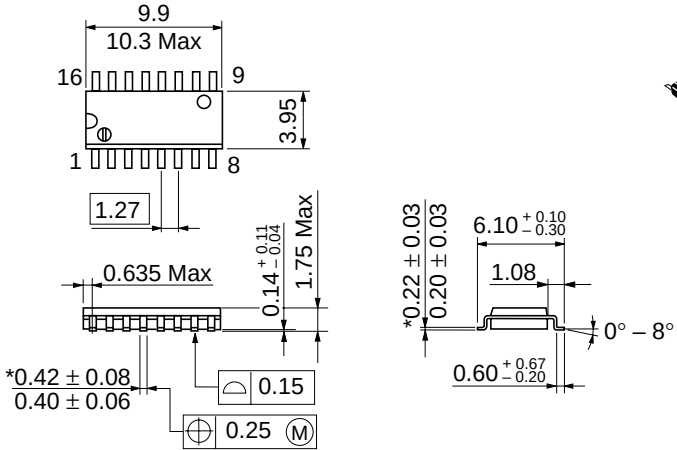


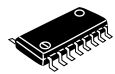


*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g

Unit: mm





Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

*Dimension including the plating thickness
Base material dimension

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