HD74AC138/HD74ACT138

1-of-8 Decoder/Demultiplexer

HITACHI

Description

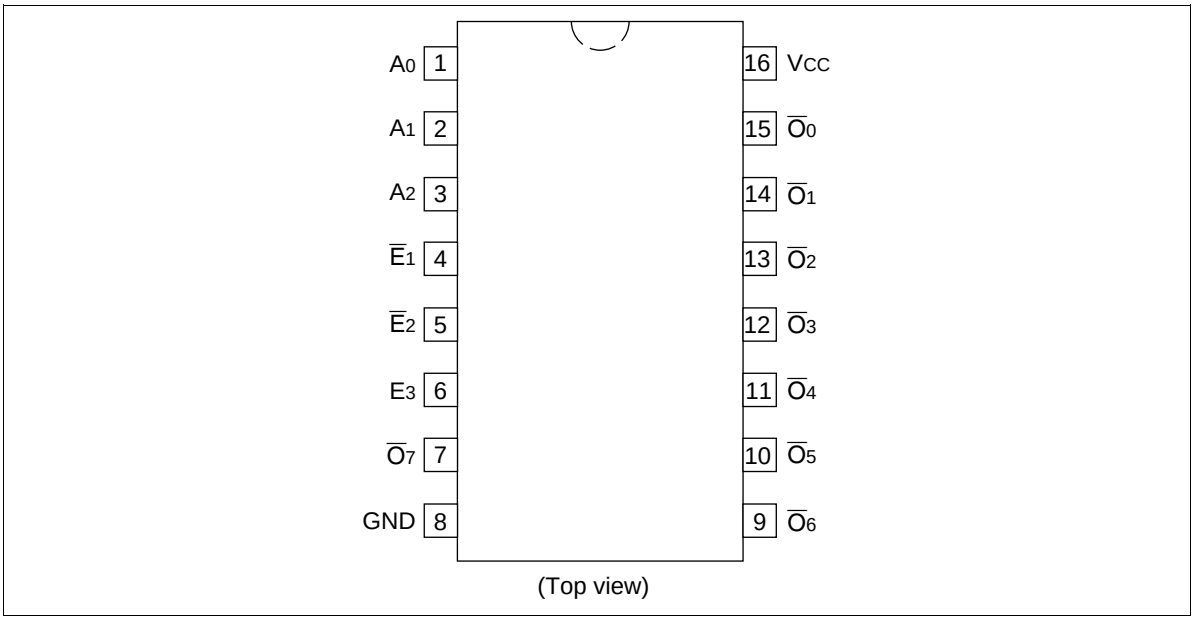
The HD74AC138/HD74ACT138 is a high-speed 1-of-8 decoder/demultiplexer. This device is ideally suited for high-speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three HD74AC138/HD74ACT138 devices or a 1-of-32 decoder using four HD74AC138/HD74ACT138 devices and one inverter.

Features

- Demultiplexing Capability
- Multiple Input Enable for Easy Expansion
- Active LOW Mutually Exclusive Outputs
- Outputs Source/Sink 24 mA
- HD74ACT138 has TTL-Compatible Inputs

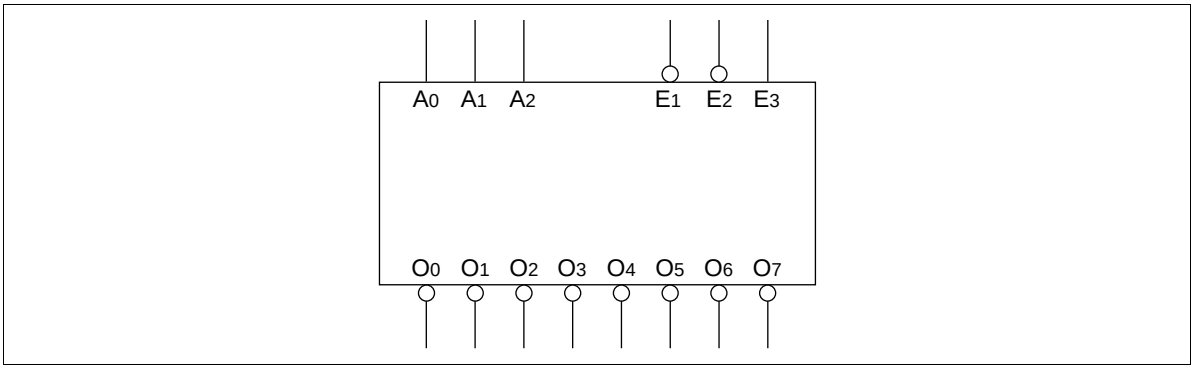
Hitachi semiconductor

Pin Arrangement



(Top view)

Logic Symbol



Pin Names

A_0 to A_2	Address Inputs
$\overline{E}_1$ to $\overline{E}_2$	Enable Inputs
E_3	Enable Input
$\overline{O}_0$ to $\overline{O}_7$	Outputs

Functional Description

The HD74AC138/HD74ACT138 high-speed 1-of-8 decoder/demultiplexer accepts three binary weighted inputs (A_0, A_1, A_2) and, when enabled, provides eight mutually exclusive active-LOW outputs ($\overline{O}_0$ to $\overline{O}_7$). The HD74AC138/HD74ACT138 features three Enable inputs, two active-Low ($\overline{E}_1$, $\overline{E}_2$) and one active-High (E_3). All outputs will be High unless $\overline{E}_1$ and $\overline{E}_2$ are Low and E_3 is High. This multiple enabled function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four HD74AC138/HD74ACT138 devices and one inverter (See Figure a). The HD74AC138/HD74ACT138 can be used as an 8-output demultiplexer by using one of the active Low Enable inputs as the data input and the other Enable inputs as strobes. The Enables inputs which are not used must be permanently tied to their appropriate active-High or active-Low state.

Truth Table

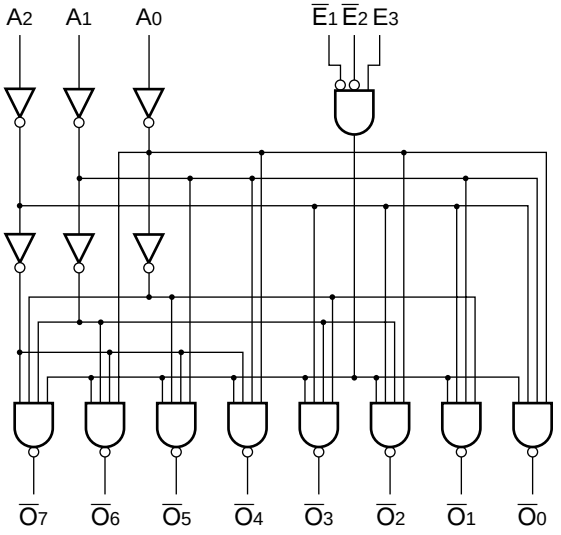
Inputs						Outputs							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H : High Voltage Level

L : Low Voltage Level

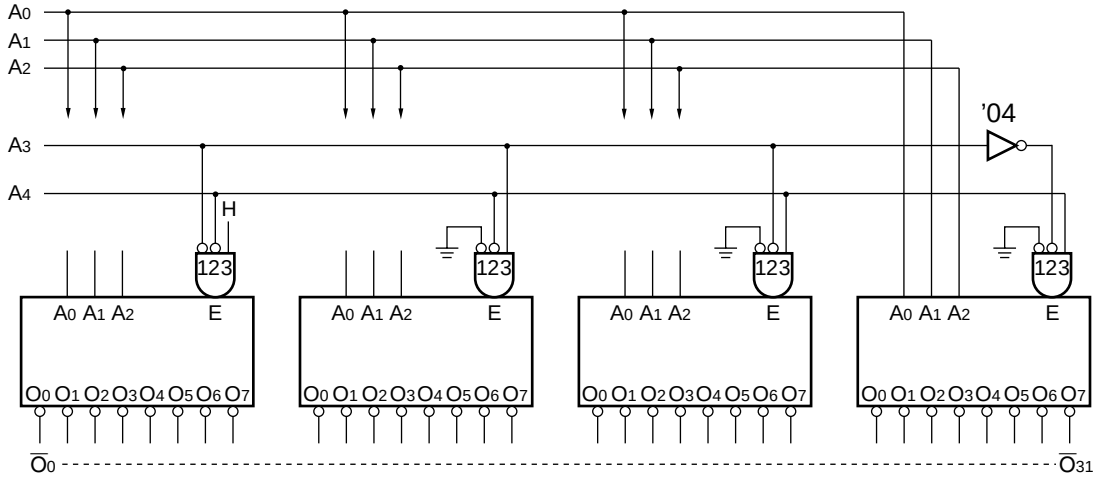
X : Immaterial

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure a: Expansion of 1-of-32 Decoding



DC Characteristics (unless otherwise specified)

Item	Symbol	Max	Unit	Condition
Maximum quiescent supply current	I_{CC}	80	µA	V_{IN} = V_{CC} or ground, V_{CC} = 5.5 V, Ta = Worst case
Maximum quiescent supply current	I_{CC}	8.0	µA	V_{IN} = V_{CC} or ground, V_{CC} = 5.5 V, Ta = 25°C
Maximum I_{CC}/input (HD74ACT138)	I_{CCT}	1.5	mA	V_{IN} = V_{CC} – 2.1 V, V_{CC} = 5.5 V Ta = Worst case

AC Characteristics: HD74AC138

			Ta = +25°C C_L = 50 pF			Ta = –40°C to +85°C C_L = 50 pF		
Item	**Symbol**	**V_{CC} (V)*[1]**	**Min**	**Typ**	**Max**	**Min**	**Max**	**Unit**
Propagation delay	t_{PLH}	3.3	1.0	8.5	13.0	1.0	15.0	ns
A_n to $\overline{O}_n$		5.0	1.0	6.5	9.5	1.0	10.5	
Propagation delay	t_{PHL}	3.3	1.0	8.0	12.5	1.0	14.0	ns
A_n to $\overline{O}_n$		5.0	1.0	6.0	9.0	1.0	10.5	
Propagation delay	t_{PLH}	3.3	1.0	11.0	15.0	1.0	16.0	ns
$\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$		5.0	1.0	8.0	11.0	1.0	12.0	
Propagation delay	t_{PHL}	3.3	1.0	9.5	13.5	1.0	15.0	ns
$\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$		5.0	1.0	7.0	9.5	1.0	10.5	
Propagation delay	t_{PLH}	3.3	1.0	11.0	15.5	1.0	16.5	ns
E_3 to $\overline{O}_n$		5.0	1.0	8.0	11.0	1.0	12.5	
Propagation delay	t_{PHL}	3.3	1.0	8.5	13.0	1.0	14.0	ns
E_3 to $\overline{O}_n$		5.0	1.0	6.0	8.0	1.0	9.5	

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Characteristics: HD74ACT138

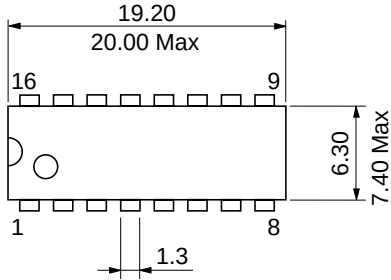
			Ta = +25°C C_L = 50 pF			Ta = –40°C to +85°C C_L = 50 pF		
Item	**Symbol**	**V_{cc} (V)*[1]**	**Min**	**Typ**	**Max**	**Min**	**Max**	**Unit**
Propagation delay An to $\overline{O}_n$	t_{PLH}	5.0	1.0	7.0	10.5	1.0	11.5	ns
Propagation delay An to $\overline{O}_n$	t_{PHL}	5.0	1.0	6.5	10.5	1.0	11.5	ns
Propagation delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$	t_{PLH}	5.0	1.0	8.0	11.5	1.0	12.5	ns
Propagation delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$	t_{PHL}	5.0	1.0	7.5	11.5	1.0	12.5	ns
Propagation delay E_3 to $\overline{O}_n$	t_{PLH}	5.0	1.0	8.0	12.0	1.0	13.0	ns
Propagation delay E_3 to $\overline{O}_n$	t_{PHL}	5.0	1.0	6.5	10.5	1.0	11.5	ns

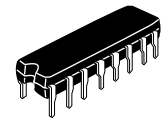
Note: 1. Voltage Range 5.0 is 5.0 V ± 0.5 V

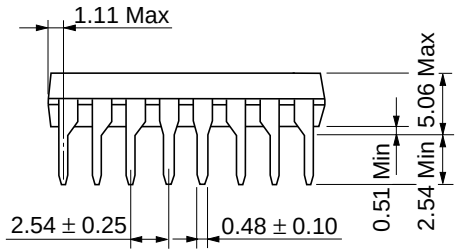
Capacitance

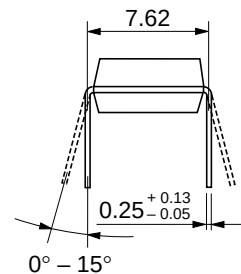
Item	**Symbol**	**Typ**	**Unit**	**Condition**
Input capacitance	C_{IN}	4.5	pF	V_{CC} = 5.5 V
Power dissipation capacitance	C_{PD}	60.0	pF	V_{CC} = 5.0 V

Unit: mm



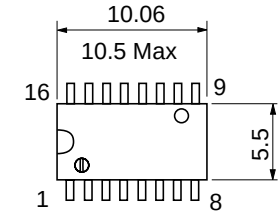


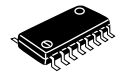


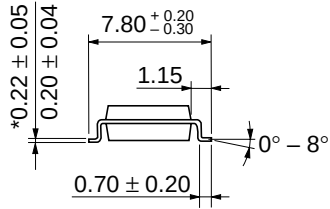


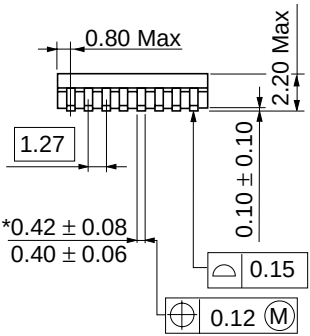
Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g

Unit: mm





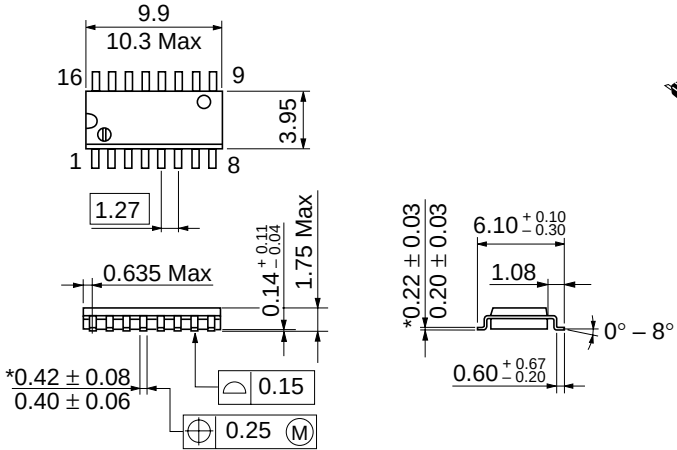




*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g

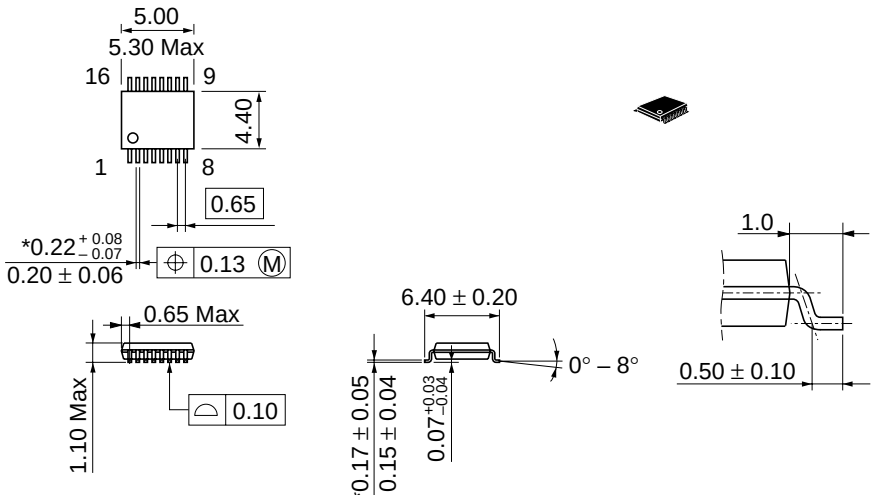
Unit: mm



Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

*Dimension including the plating thickness
Base material dimension

Unit: mm



Hitachi Code	TTP-16DA
JEDEC	—
EIAJ	—
Weight (reference value)	0.05 g

*Dimension including the plating thickness
Base material dimension

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