
HD74AC174

Hex D-Type Flip-Flop with Master Reset

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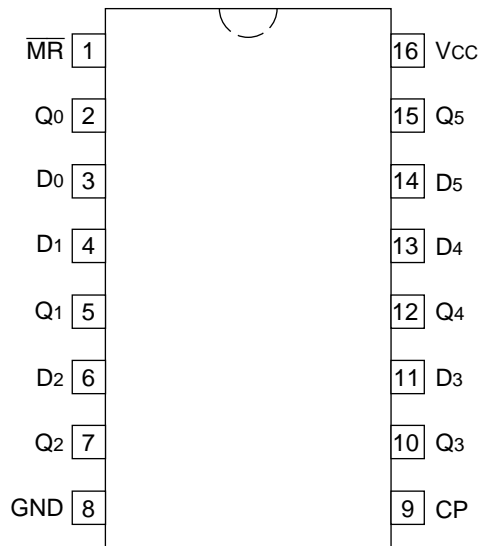
Description

The HD74AC174 is a high-speed hex D flip-flop. The device is used primarily as a 6-bit edge-triggered storage register. The information on the D inputs is transferred to storage during the Low-to-High clock transition. The device has a Master Reset to simultaneously clear all flip-flops.

Feature

- Outputs Source/Sink 24 mA

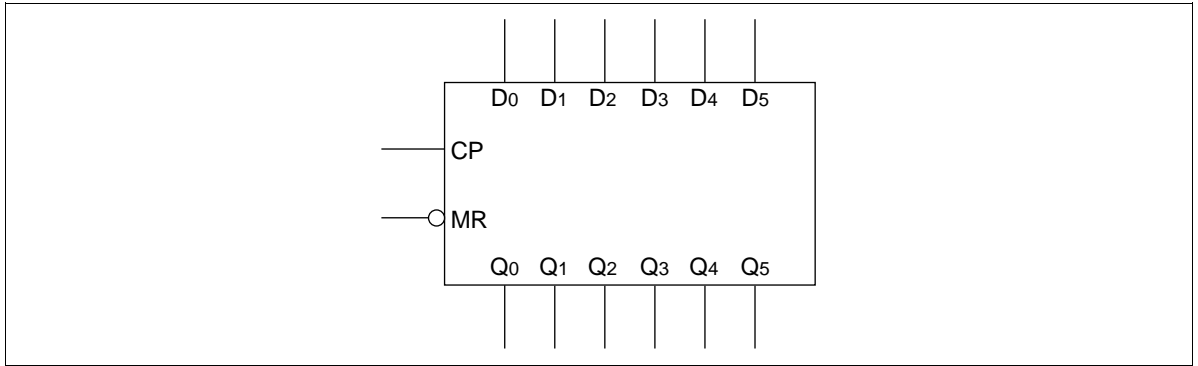
Pin Arrangement



(Top view)

HD74AC174

Logic Symbol





Pin Names

- D₀ to D₅ Data Inputs
- CP Clock Pulse Input
- $\overline{\text{MR}}$ Master Reset Input
- Q₀ to Q₅ Outputs

Functional Description

The HD74AC174 consists of six edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Master Reset ($\overline{\text{MR}}$) are common to all flip-flops. Each D input's state is transferred to the corresponding flip-flop's output following the Low-to-High Clock (CP) transition. A Low input to the Master Reset ($\overline{\text{MR}}$) will force all outputs Low independent of Clock or Data inputs. The HD74AC174 is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

Truth Table

Inputs			Output
$\overline{\text{MR}}$	CP	D	Q
L	X	X	L
H		H	H
H		L	L
H	L	X	Q

H : High Voltage Level

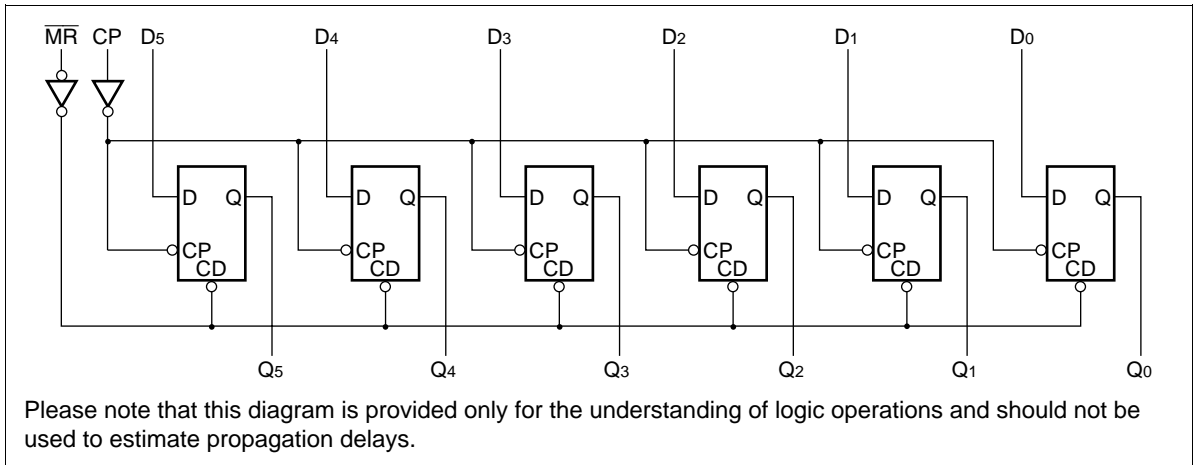
L : Low Voltage Level

X : Immaterial

 : Low-to-High Transition of Clock

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Logic Diagram



DC Characteristics (unless otherwise specified)

Item	Symbol	Max	Unit	Condition
Maximum quiescent supply current	I_{CC}	80	μA	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5 V$, $T_a = \text{Worst case}$
Maximum quiescent supply current	I_{CC}	8.0	μA	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5 V$, $T_a = 25^\circ C$

AC Characteristics: HD74AC174

Item	Symbol	$V_{CC} (V)^{*1}$	$T_a = +25^\circ C$ $C_L = 50 pF$			$T_a = -40^\circ C \text{ to } +85^\circ C$ $C_L = 50 pF$		Unit
			Min	Typ	Max	Min	Max	
Maximum clock frequency	f_{max}	3.3	90	100	—	70	—	MHz
		5.0	100	125	—	100	—	
Propagation delay CP to Q_n	t_{PLH}	3.3	1.0	9.0	11.5	1.0	12.5	ns
		5.0	1.0	6.0	8.5	1.0	9.5	
Propagation delay CP to Q_n	t_{PHL}	3.3	1.0	8.5	11.0	1.0	12.0	ns
		5.0	1.0	6.0	8.0	1.0	9.0	
Propagation delay \overline{MR} to Q_n	t_{PHL}	3.3	1.0	9.0	11.5	1.0	12.5	ns
		5.0	1.0	7.0	9.0	1.0	10.5	

Note: 1. Voltage Range 3.3 is $3.3 V \pm 0.3 V$
Voltage Range 5.0 is $5.0 V \pm 0.5 V$

HD74AC174

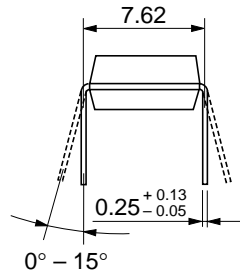
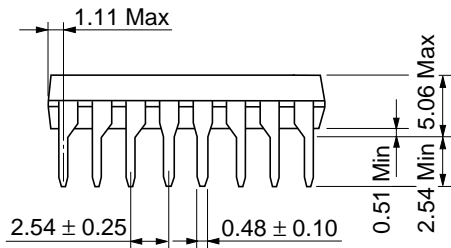
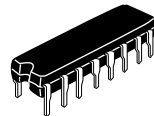
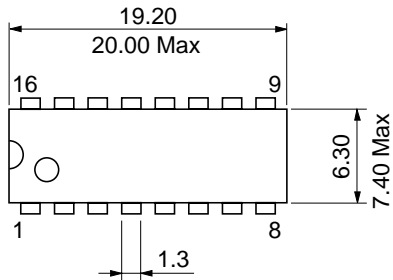
AC Operating Requirements: HD74AC174

Item	Symbol	V_{CC} (V)*1	$T_a = +25^\circ\text{C}$ $C_L = 50 \text{ pF}$		$T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$ $C_L = 50 \text{ pF}$	
			Typ	Guaranteed Minimum	Guaranteed Minimum	Unit
Setup time, HIGH or LOW	t_{su}	3.3	2.5	6.5	7.0	ns
D_n to CP		5.0	2.0	5.0	5.5	
Hold time, HIGH or LOW	t_h	3.3	1.0	3.0	3.0	ns
D_n to CP		5.0	0.5	3.0	3.0	
\overline{MR} pulse width, LOW	t_w	3.3	1.0	5.5	7.0	ns
		5.0	1.0	5.0	5.0	
CP pulse width	t_w	3.3	1.0	5.5	7.0	ns
		5.0	1.0	5.0	5.0	
Recovery time	t_{rec}	3.3	0	2.5	2.5	ns
\overline{MR} to CP		5.0	0	2.0	2.0	

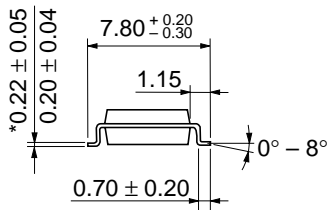
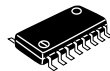
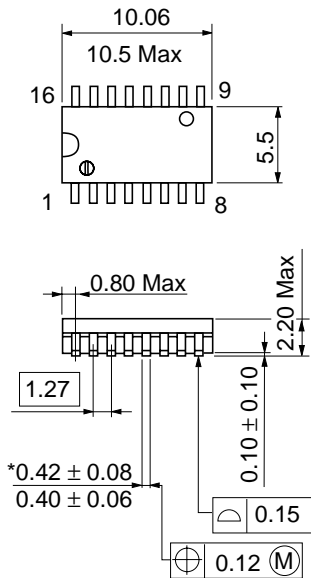
Note: 1. Voltage Range 3.3 is $3.3 \text{ V} \pm 0.3 \text{ V}$
Voltage Range 5.0 is $5.0 \text{ V} \pm 0.5 \text{ V}$

Capacitance

Item	Symbol	Typ	Unit	Condition
Input capacitance	C_{IN}	4.5	pF	$V_{CC} = 5.5 \text{ V}$
Power dissipation capacitance	C_{PD}	85.0	pF	$V_{CC} = 5.0 \text{ V}$

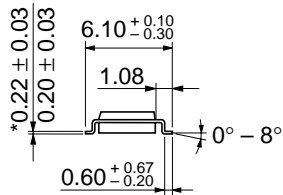
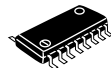
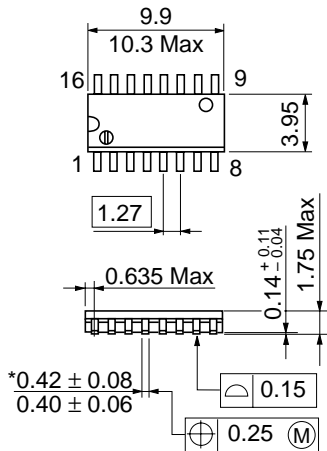


Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g



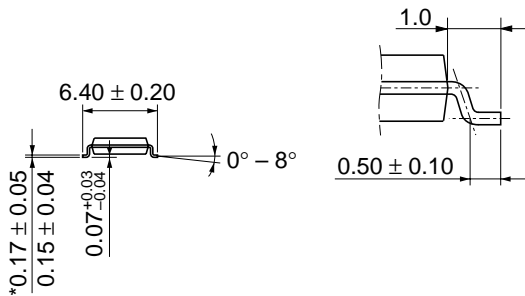
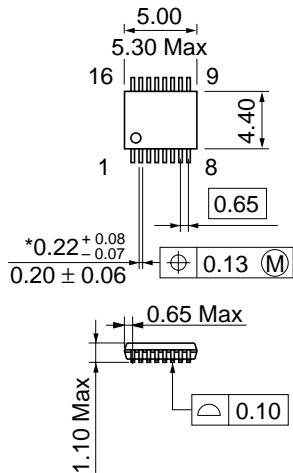
*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g



*Dimension including the plating thickness
 Base material dimension

Hitachi Code	TTP-16DA
JEDEC	—
EIAJ	—
Weight (reference value)	0.05 g

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