
BB101M

Build in Biasing Circuit MOS FET IC
UHF RF Amplifier

HITACHI

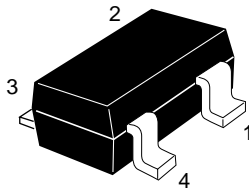
ADE-208-504
1st. Edition

Features

- Build in Biasing Circuit; To reduce using parts cost & PC board space.
- Low noise characteristics; (NF = 2.0 dB typ. at f = 900 MHz)
- Withstanding to ESD; Build in ESD absorbing diode. Withstand up to 200 V at C = 200 pF, Rs = 0 conditions.

Outline

MPAK-4



1. Source
2. Gate1
3. Gate2
4. Drain

Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DS}	6	V
Gate 1 to source voltage	V_{G1S}	+6 -0	V
Gate 2 to source voltage	V_{G2S}	± 6	V
Drain current	I_D	25	mA
Channel power dissipation	Pch	150	mW
Channel temperature	Tch	150	$^\circ\text{C}$
Storage temperature	Tstg	-55 to +150	$^\circ\text{C}$

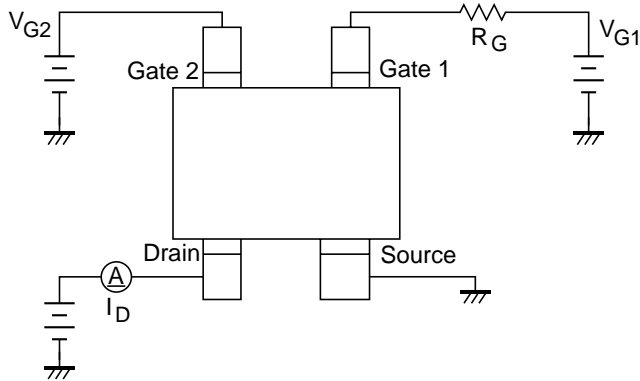
Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	6	—	—	V	$I_D = 200 \mu A$ $V_{G1S} = V_{G2S} = 0$
Gate 1 to source breakdown voltage	$V_{(BR)G1SS}$	+6	—	—	V	$I_{G1} = +10 \mu A$ $V_{G2S} = V_{DS} = 0$
Gate 2 to source breakdown voltage	$V_{(BR)G2SS}$	± 6	—	—	V	$I_{G2} = \pm 10 \mu A$ $V_{G1S} = V_{DS} = 0$
Gate 1 to source cutoff current	I_{G1SS}	—	—	+100	nA	$V_{G1S} = +5 V$ $V_{G2S} = V_{DS} = 0$
Gate 2 to source cutoff current	I_{G2SS}	—	—	± 100	nA	$V_{G2S} = \pm 5 V$ $V_{G1S} = V_{DS} = 0$
Gate 1 to source cutoff voltage	$V_{G1S(off)}$	0.2	—	0.8	V	$V_{DS} = 5 V, V_{G2S} = 4 V$ $I_D = 100 \mu A$
Gate 2 to source cutoff voltage	$V_{G2S(off)}$	0.4	—	1.0	V	$V_{DS} = 5 V, V_{G1S} = 5 V$ $I_D = 100 \mu A$
Drain current	$I_{D(op)}$	10	15	20	mA	$V_{DS} = 5 V, V_{G1} = 5 V$ $V_{G2S} = 4 V, R_G = 220 k\Omega$
Forward transfer admittance	$ y_{fs} $	16	22	—	mS	$V_{DS} = 5 V, V_{G1} = 5 V,$ $V_{G2S} = 4 V,$ $R_G = 220 k\Omega, f = 1 kHz$
Input capacitance	Ciss	1.2	1.7	2.2	pF	$V_{DS} = 5 V, V_{G1} = 5 V$
Output capacitance	Coss	0.7	1.1	1.5	pF	$V_{G2S} = 4 V, R_G = 220 k\Omega$
Reverse transfer capacitance	Crss	—	0.012	0.03	pF	$f = 1 MHz$
Power gain	PG	16	20	—	dB	$V_{DS} = 5 V, V_{G1} = 5 V$ $V_{G2S} = 4 V$
Noise figure	NF	—	2.0	3.0	dB	$R_G = 220 k\Omega, f = 900 MHz$

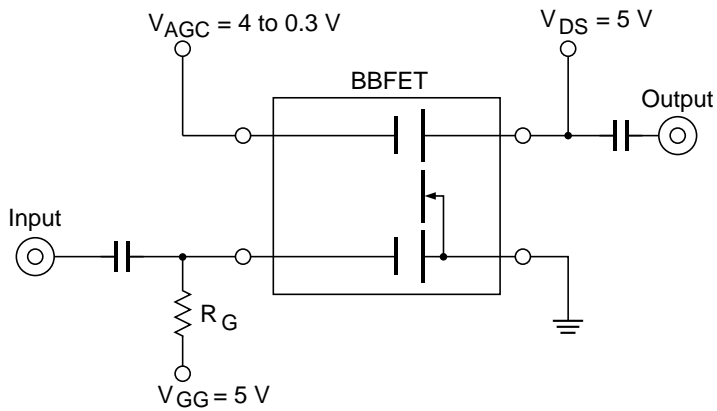
Note: Marking is "AU-".

Main Characteristics

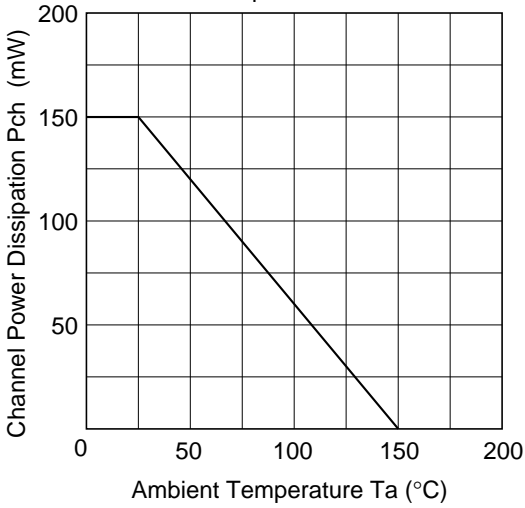
Test Circuit for Operating Items ($I_{D(op)}$, $|y_{fs}|$, C_{iss} , C_{oss} , C_{rss} , NF, PG)



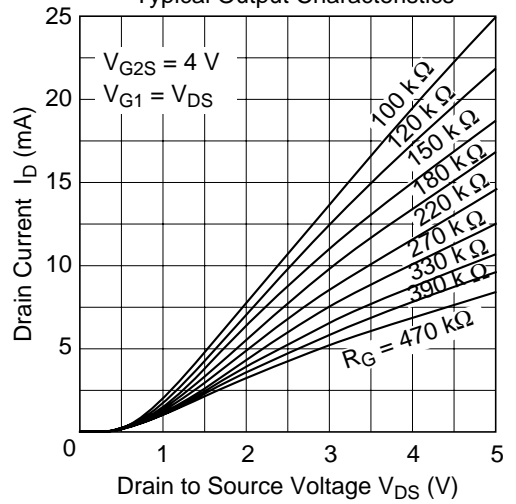
Application Circuit



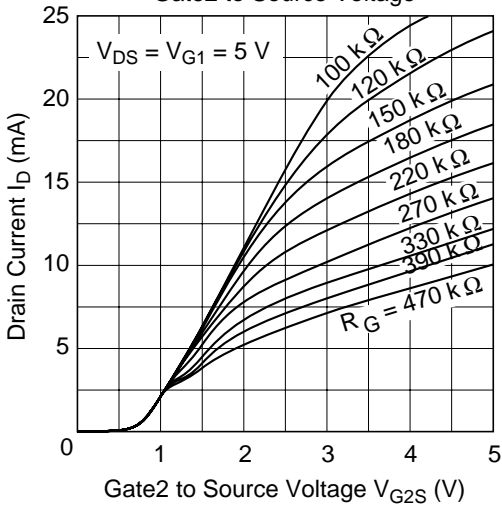
Maximum Channel Power Dissipation Curve



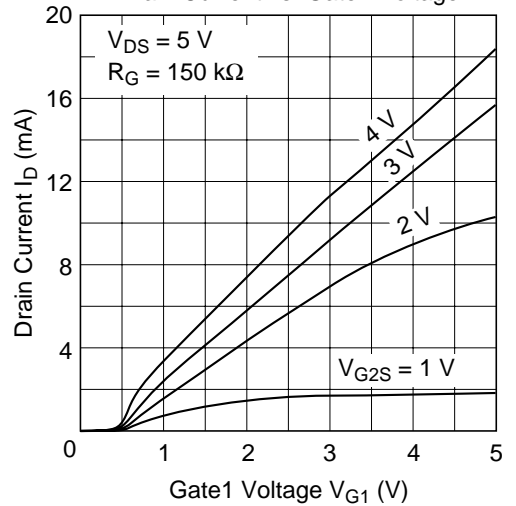
Typical Output Characteristics

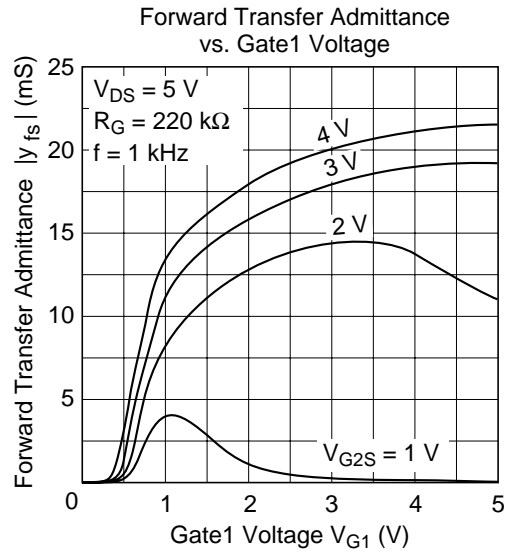
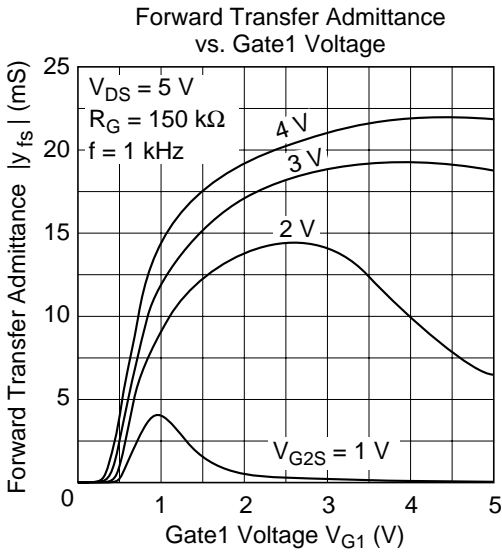
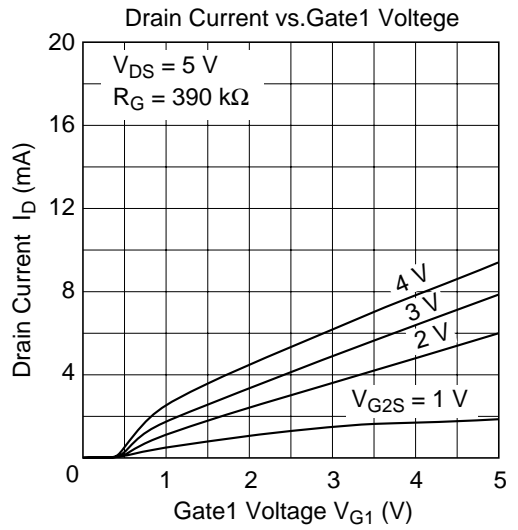
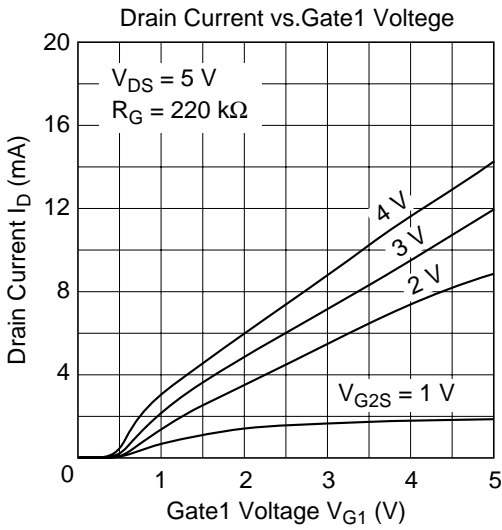


Drain Current vs. Gate2 to Source Voltage

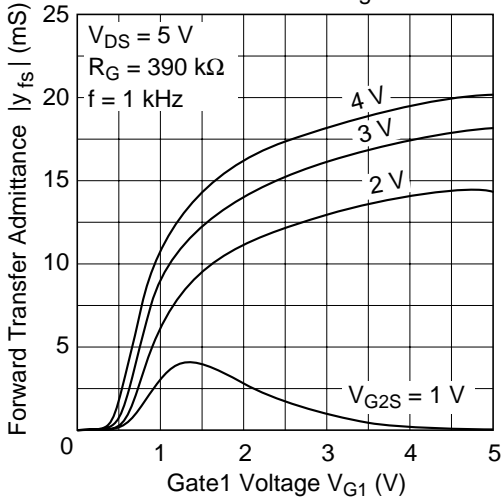


Drain Current vs. Gate1 Voltage

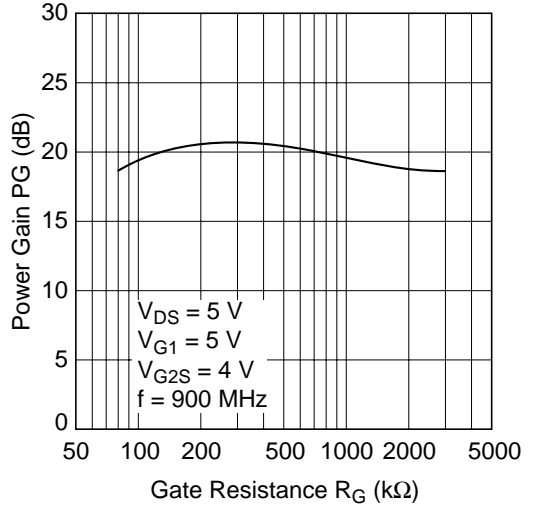




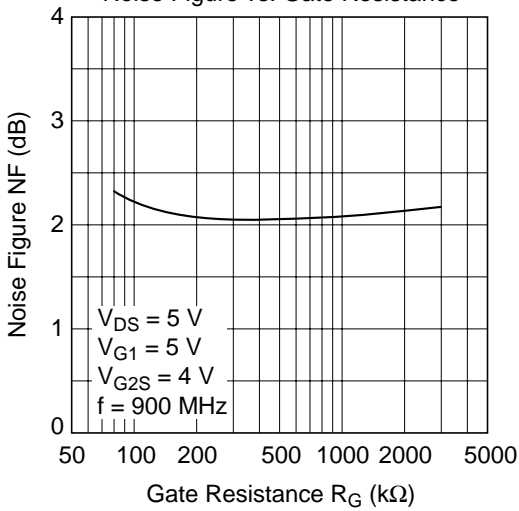
Forward Transfer Admittance vs. Gate1 Voltage



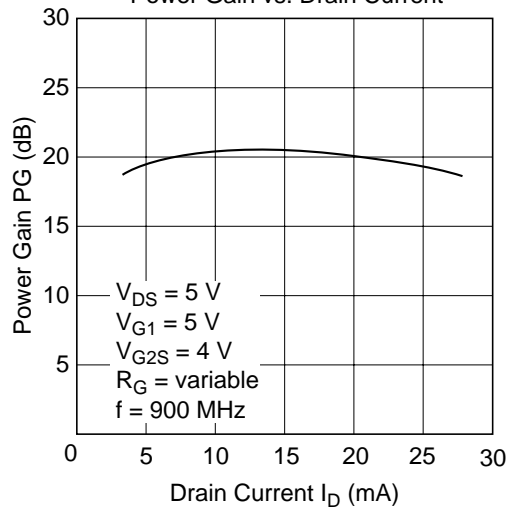
Power Gain vs. Gate Resistance

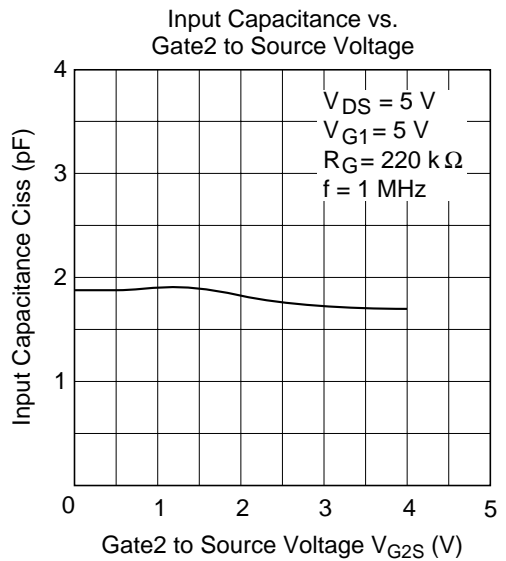
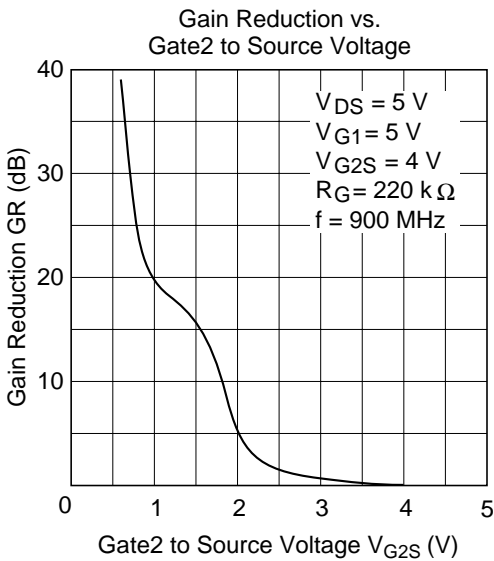
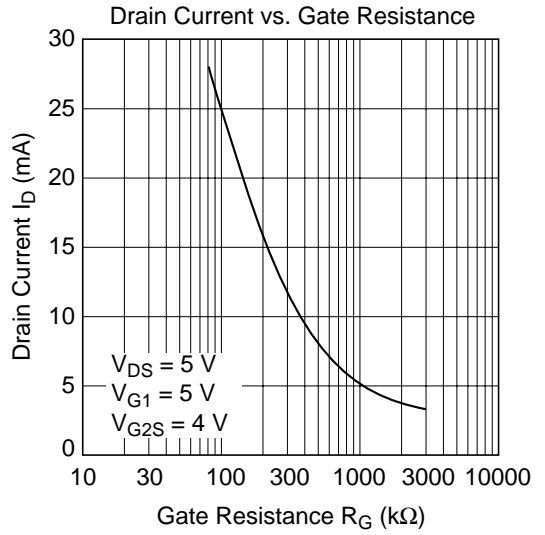
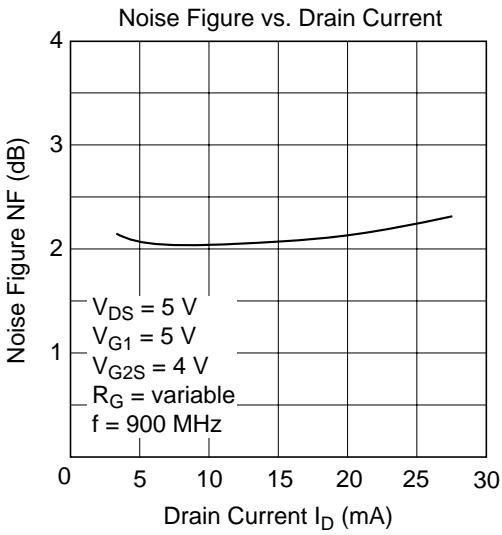


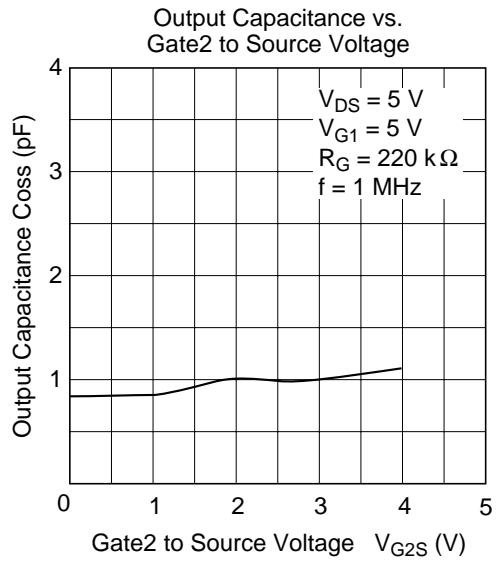
Noise Figure vs. Gate Resistance



Power Gain vs. Drain Current

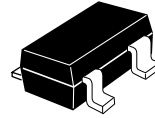
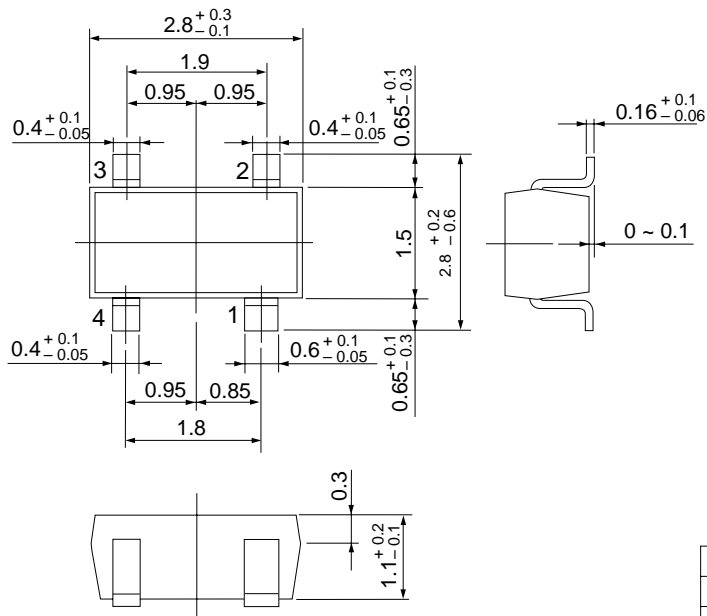






Package Dimentions

Unit: mm



Hitachi Code	MPAK-4
EIAJ	SC-61AA
JEDEC	—

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