2SJ452

Silicon P-Channel MOS FET

HITACHI

ADE-208-383
1st. Edition

Application

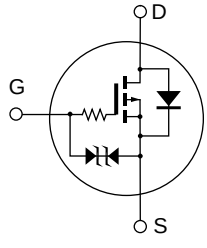
Low frequency power switching

Features

- Low on-resistance.
- Low drive power
- 2.5 V gate drive device.
- Small package (MPAK).

Outline

MPAK



1. Source
2. Gate
3. Drain

Hitachi semiconductor

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–50	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–0.2	A
Drain peak current	$I_{D(pulse)}$*[1]	–0.4	A
Channel dissipation	Pch	150	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

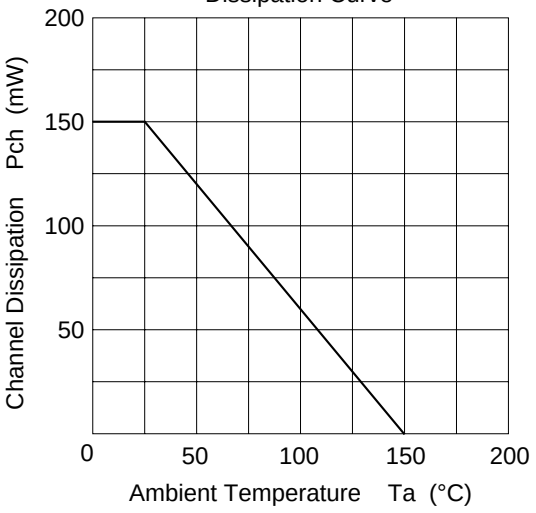
Note: 1. PW ≤ 10 µs, duty cycle ≤ 1%
Marking is "ZM–".

Electrical Characteristics (Ta = 25°C)

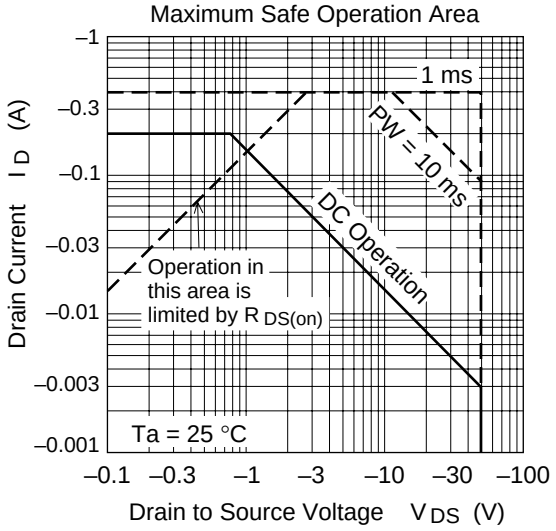
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–50	—	—	V	I_D = –100 µA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–1.0	µA	V_{DS} = –40 V, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±2.0	µA	V_{GS} = ±16 V, V_{DS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–0.5	—	–1.5	V	I_D = –10 µA, V_{DS} = –5 V
Static drain to source on state resistance	$R_{DS(on)}$1	—	5.0	7.0	Ω	I_D = –100 mA V_{GS} = –4 V*[1]
Static drain to source on state resistance	$R_{DS(on)}$2	—	7.5	12.0	Ω	I_D = –40 mA V_{GS} = –2.5 V*[1]
Foward transfer admittance	$\|y_{fs}\|$	0.1	0.19	—	S	I_D = –100 mA*[1] V_{DS} = –10 V
Input capacitance	Ciss	—	1.1	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	15.7	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	0.12	—	pF	f = 1 MHz
Turn-on delay time	$t_{d(on)}$	—	0.45	—	µs	V_{GS} = –10 V, I_D = –0.1 A
Rise time	t_r	—	1.3	—	µs	R_L = 300 Ω
Turn-off delay tiem	$t_{d(off)}$	—	8.4	—	µs	
Fall time	t_f	—	5.6	—	µs	

Note: 1. Pulse Test

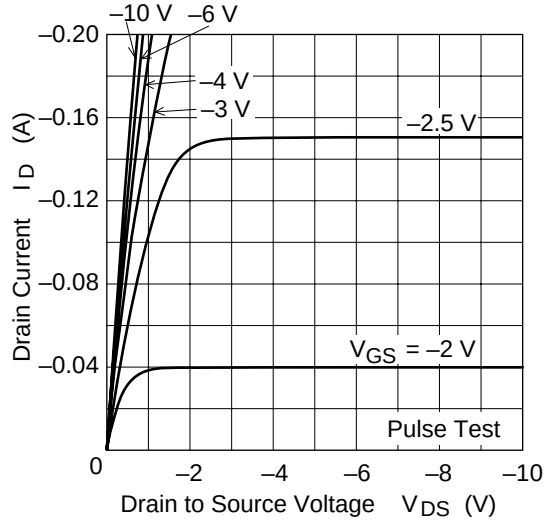
Maximum Channel Dissipation Curve



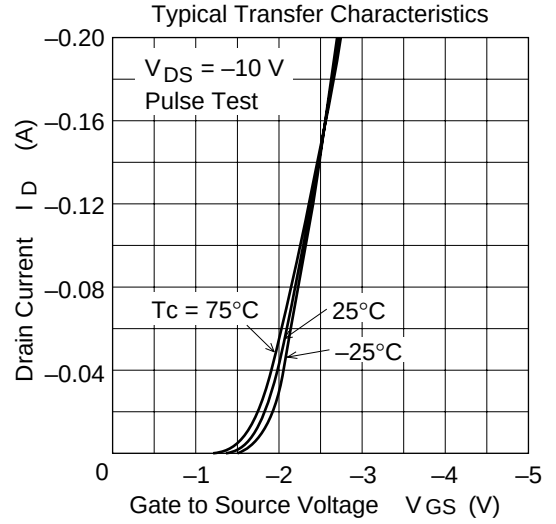
Maximum Safe Operation Area



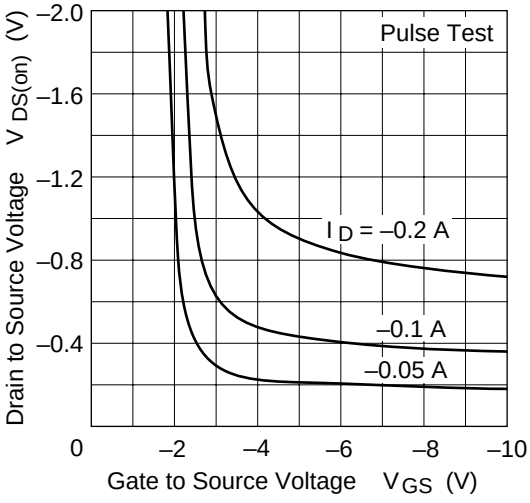
Typical Output Characteristics



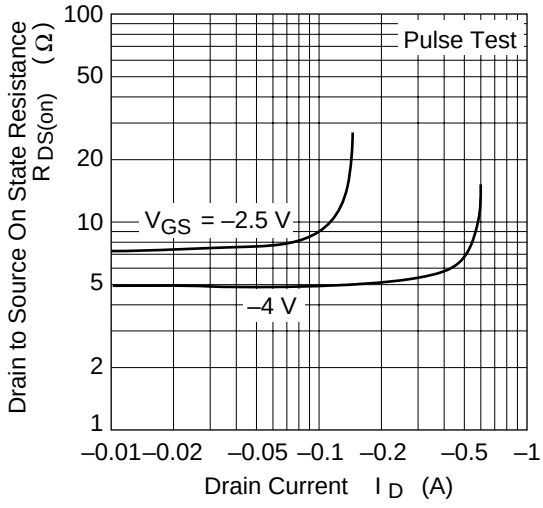
Typical Transfer Characteristics



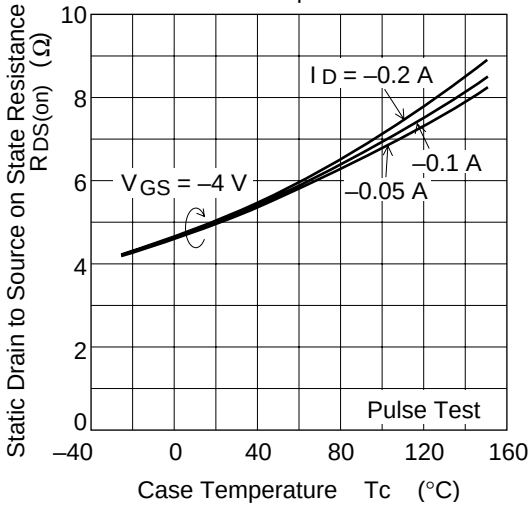
Drain to Source Saturation Voltage vs. Gate to Source Voltage



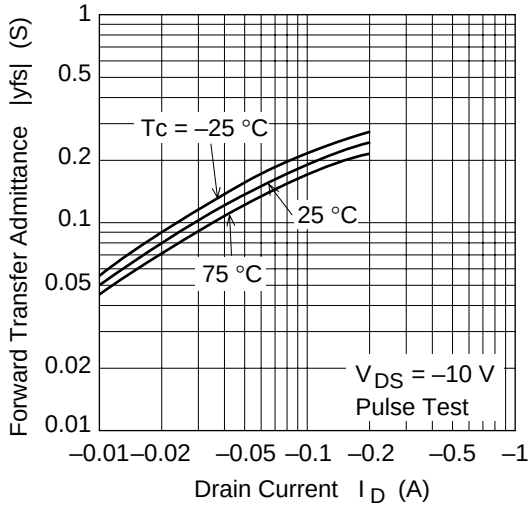
Static Drain to Source on State Resistance vs. Drain Current



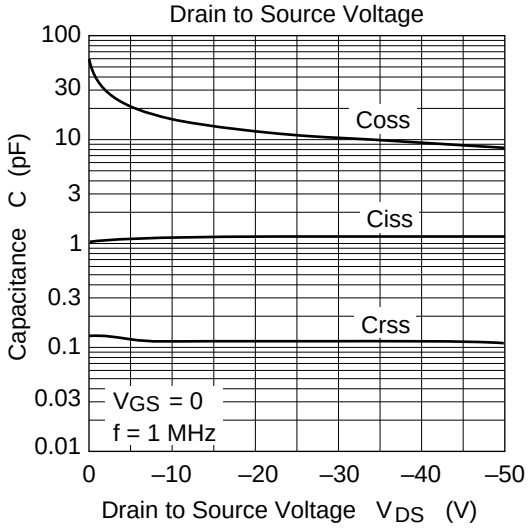
Static Drain to Source on State Resistance vs. Temperature



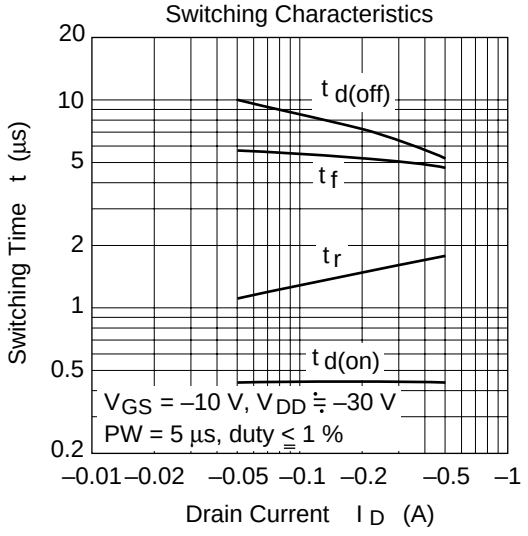
Forward Transfer Admittance vs. Drain Current



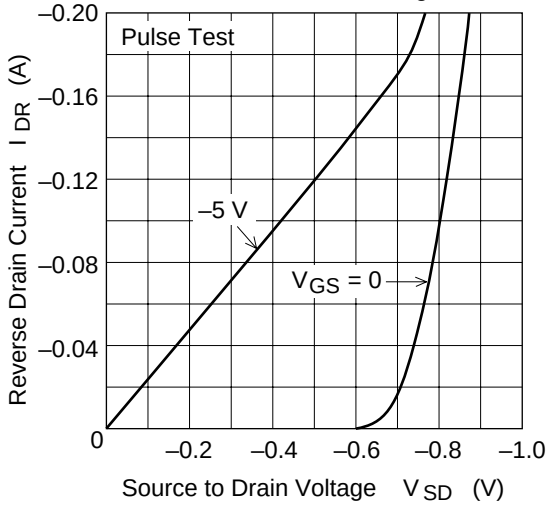
Typical Capacitance vs.
Drain to Source Voltage



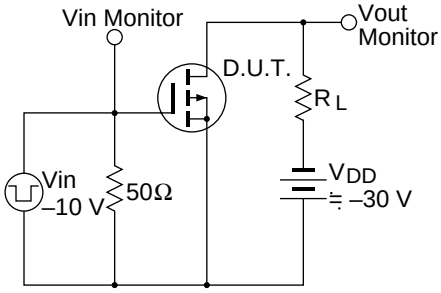
Switching Characteristics

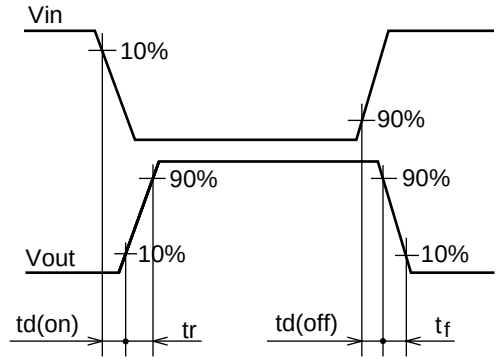


Reverse Drain Current vs.
Source to Drain Voltage

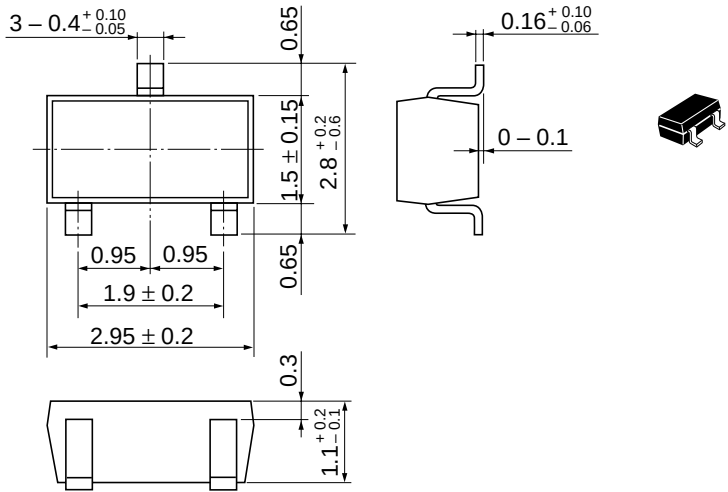


Avalanche Test Circuit and Waveform





Unit: mm



Hitachi Code	MPAK
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.011 g

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HITACHI

Hitachi, Ltd.
Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

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For further information write to:

Hitachi Semiconductor
(America) Inc.
179 East Tasman Drive,
San Jose,CA 95134
Tel: <1> (408) 433-1990
Fax: <1>(408) 433-0223

Hitachi Europe GmbH
Electronic components Group
Dornacher Straße 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia Ltd.
Taipei Branch Office
3F, Hung Kuo Building. No.167,
Tun-Hwa North Road, Taipei (105)
Tel: <886> (2) 2718-3666
Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower, World Finance Centre,
Harbour City, Canton Road, Tsim Sha Tsui,
Kowloon, Hong Kong
Tel: <852> (2) 735 9218
Fax: <852> (2) 730 0281
Telex: 40815 HITEC HX