

2SJ529(L), 2SJ529(S)

Silicon P Channel MOS FET
High Speed Power Switching

HITACHI

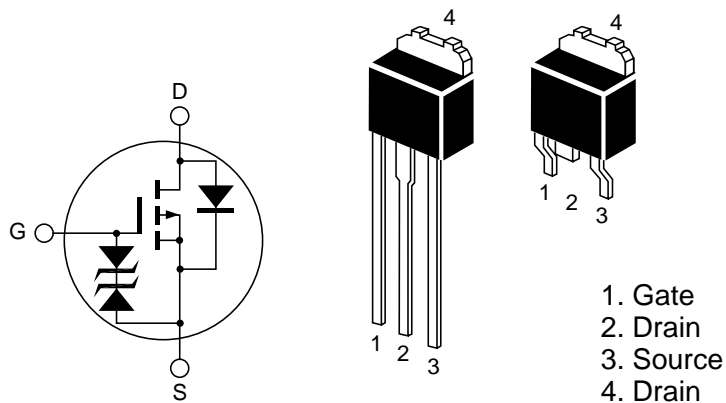
ADE-208-654A (Z)
2nd. Edition
Jun 1998

Features

- Low on-resistance
 $R_{DS(on)} = 0.12 \Omega$ typ.
- 4 V gate drive devices
- High speed switching

Outline

DPAK-2



Absolute Maximum Ratings ($T_a = 25^{\circ}\text{C}$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	-60	V
Gate to source voltage	V_{GSS}	± 20	V
Drain current	I_{D}	-10	A
Drain peak current	$I_{\text{D(pulse)}}$ ^{Note1}	-40	A
Body-drain diode reverse drain current	I_{DR}	-10	A
Avalanche current	I_{AP} ^{Note3}	-10	A
Avalanche energy	E_{AR} ^{Note3}	8.5	mJ
Channel dissipation	P_{ch} ^{Note2}	20	W
Channel temperature	T_{ch}	150	$^{\circ}\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^{\circ}\text{C}$

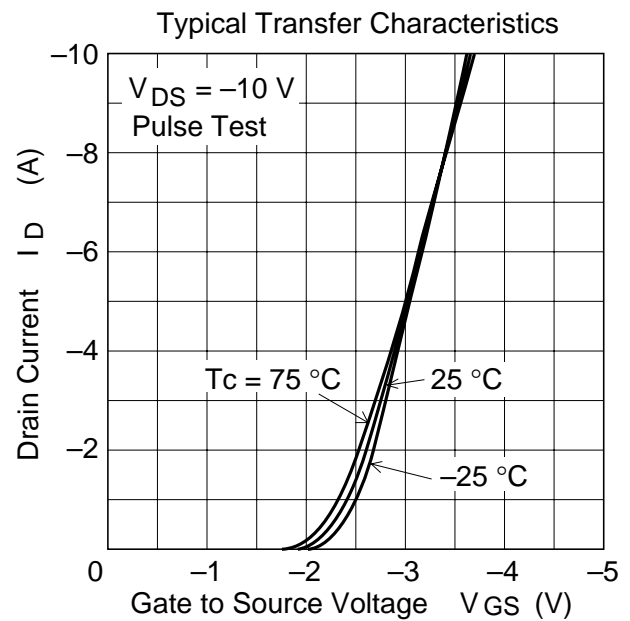
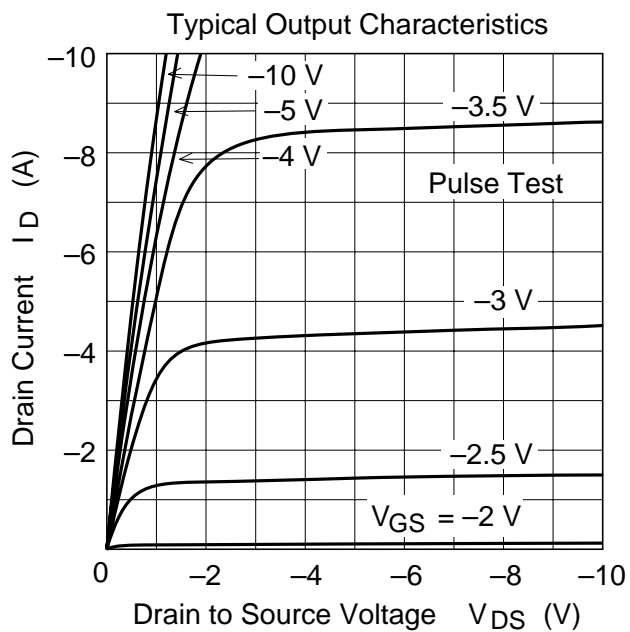
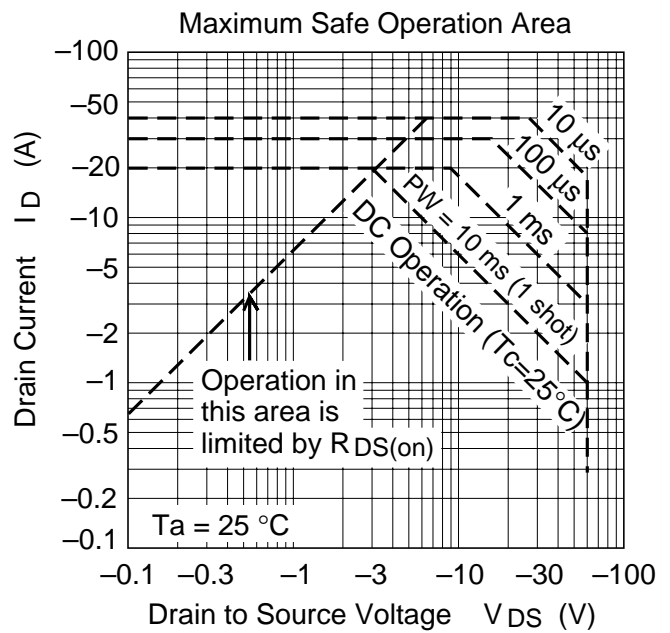
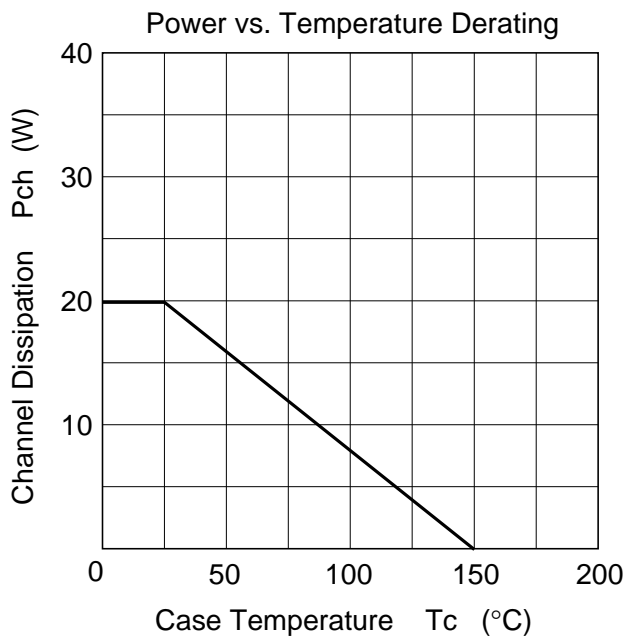
Note: 1. $PW \leq 10\mu\text{s}$, duty cycle $\leq 1\%$
 2. Value at $T_c = 25^{\circ}\text{C}$
 3. Value at $T_{\text{ch}} = 25^{\circ}\text{C}$, $R_g \geq 50\ \Omega$

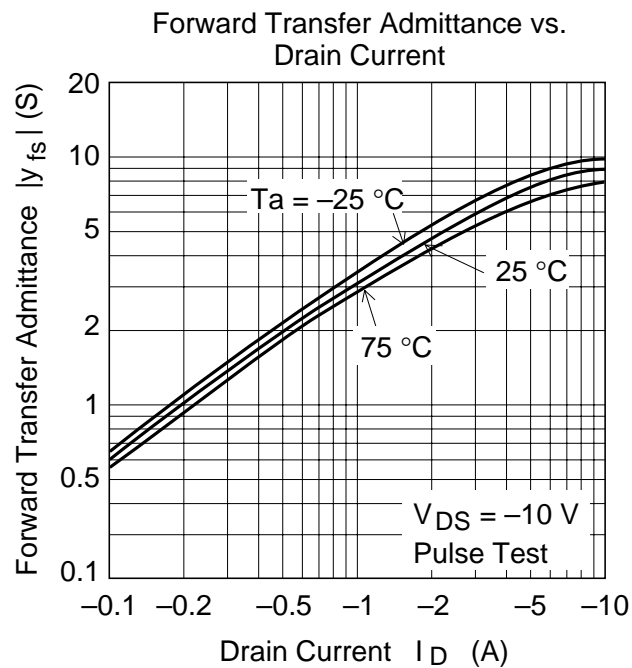
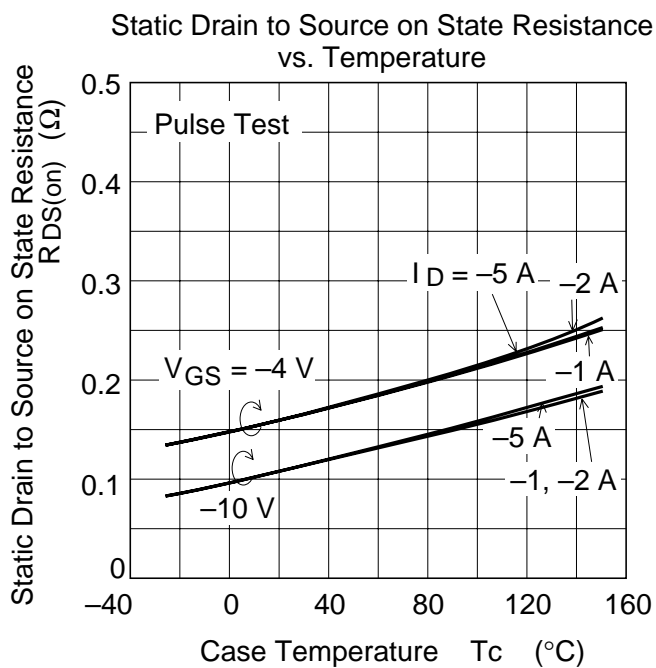
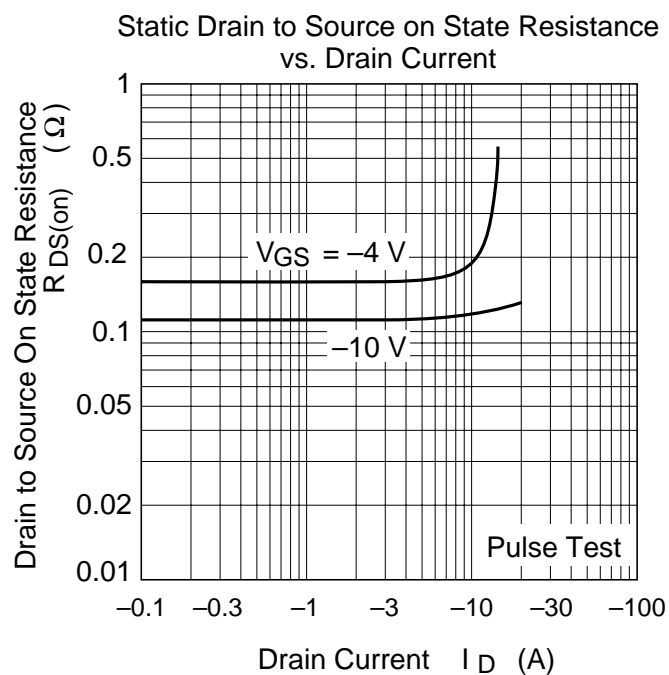
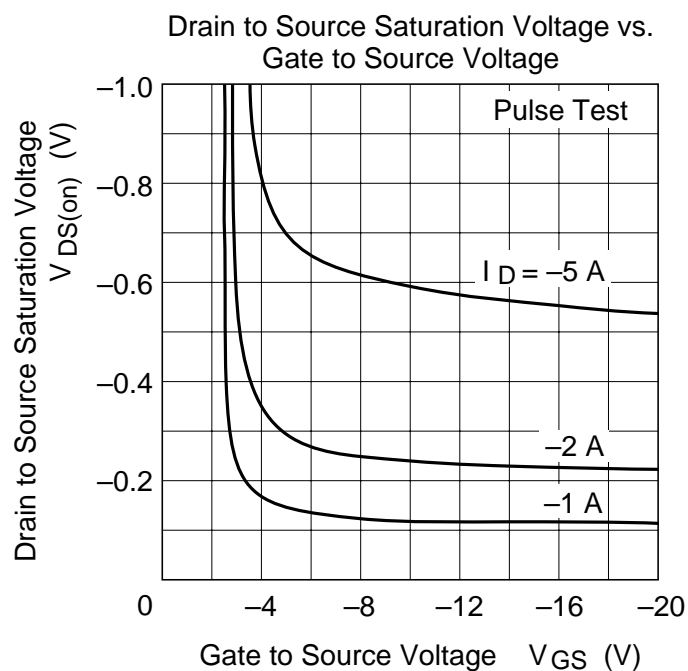
Electrical Characteristics ($T_a = 25^{\circ}\text{C}$)

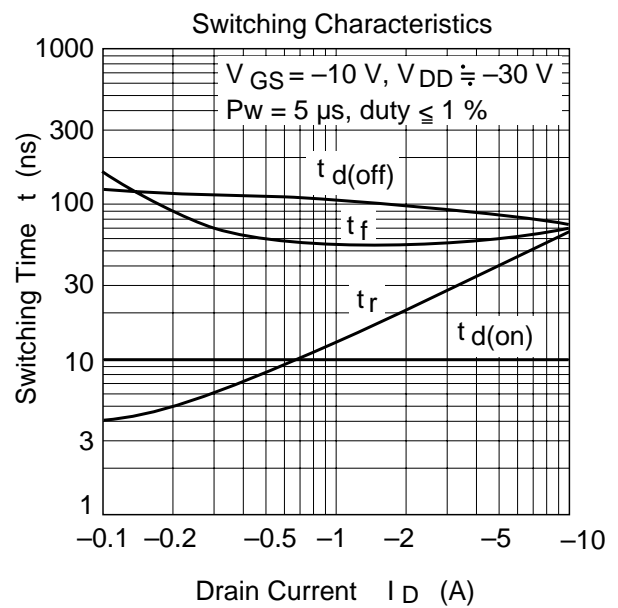
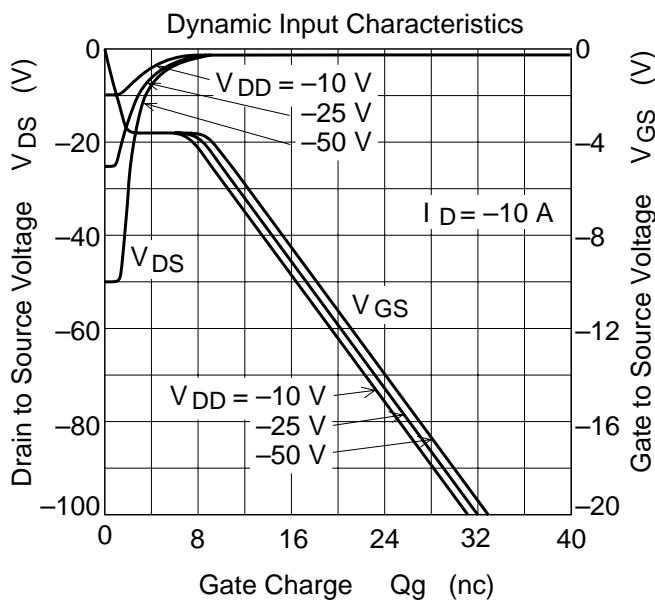
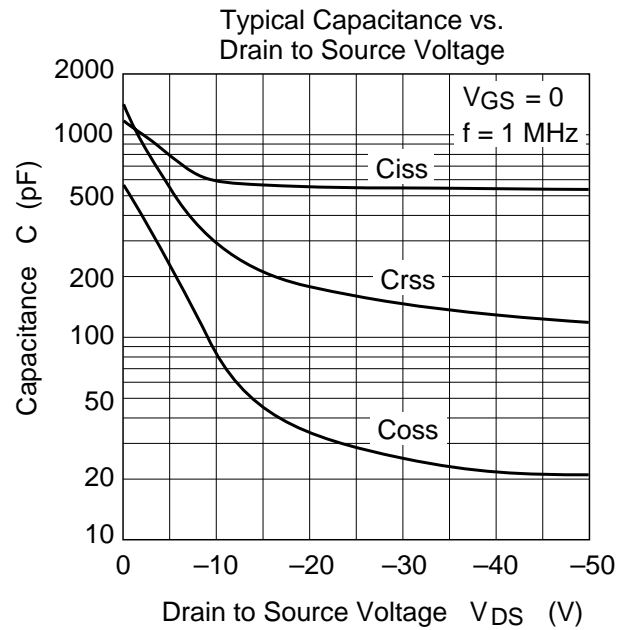
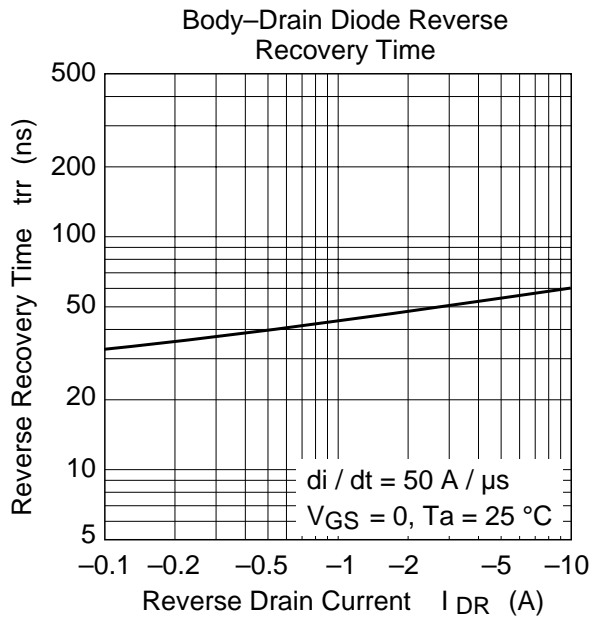
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(\text{BR})\text{DSS}}$	-60	—	—	V	$I_{\text{D}} = -10\text{mA}$, $V_{\text{GS}} = 0$
Gate to source breakdown voltage	$V_{(\text{BR})\text{GSS}}$	± 20	—	—	V	$I_{\text{G}} = \pm 100\mu\text{A}$, $V_{\text{DS}} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	-10	μA	$V_{\text{DS}} = -60\text{V}$, $V_{\text{GS}} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{\text{GS}} = \pm 16\text{V}$, $V_{\text{DS}} = 0$
Gate to source cutoff voltage	$V_{\text{GS(off)}}$	-1.0	—	-2.0	V	$I_{\text{D}} = -1\text{mA}$, $V_{\text{DS}} = -10\text{V}$
Static drain to source on state resistance	$R_{\text{DS(on)}}$	—	0.12	0.16	Ω	$I_{\text{D}} = -5\text{A}$, $V_{\text{GS}} = -10\text{V}$ ^{Note4}
	$R_{\text{DS(on)}}$	—	0.17	0.24	Ω	$I_{\text{D}} = -5\text{A}$, $V_{\text{GS}} = -4\text{V}$ ^{Note4}
Forward transfer admittance	$ y_{\text{fs}} $	4.5	7.5	—	S	$I_{\text{D}} = -5\text{A}$, $V_{\text{DS}} = -10\text{V}$ ^{Note4}
Input capacitance	C_{iss}	—	580	—	pF	$V_{\text{DS}} = -10\text{V}$
Output capacitance	C_{oss}	—	300	—	pF	$V_{\text{GS}} = 0$
Reverse transfer capacitance	C_{rss}	—	85	—	pF	$f = 1\text{MHz}$
Turn-on delay time	$t_{\text{d(on)}}$	—	10	—	ns	$V_{\text{GS}} = -10\text{V}$, $I_{\text{D}} = -5\text{A}$
Rise time	t_{r}	—	40	—	ns	$R_{\text{L}} = 6\Omega$
Turn-off delay time	$t_{\text{d(off)}}$	—	85	—	ns	
Fall time	t_{f}	—	60	—	ns	
Body-drain diode forward voltage	V_{DF}	—	-1.2	—	V	$I_{\text{F}} = -10\text{A}$, $V_{\text{GS}} = 0$
Body-drain diode reverse recovery time	t_{rr}	—	60	—	ns	$I_{\text{F}} = -10\text{A}$, $V_{\text{GS}} = 0$ $di_{\text{F}}/dt = 50\text{A}/\mu\text{s}$

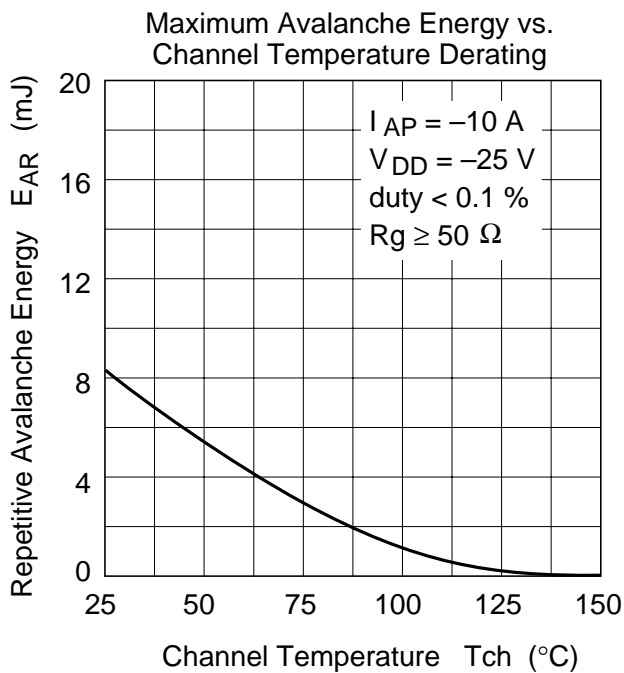
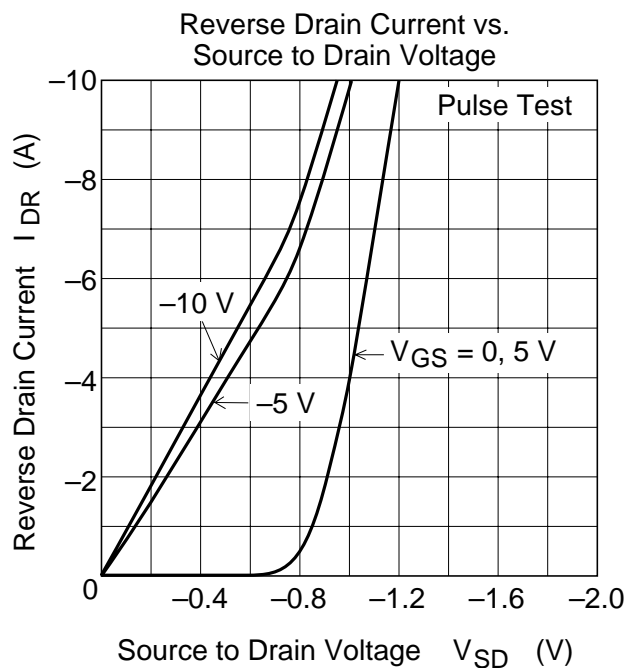
Note: 4. Pulse test

Main Characteristics

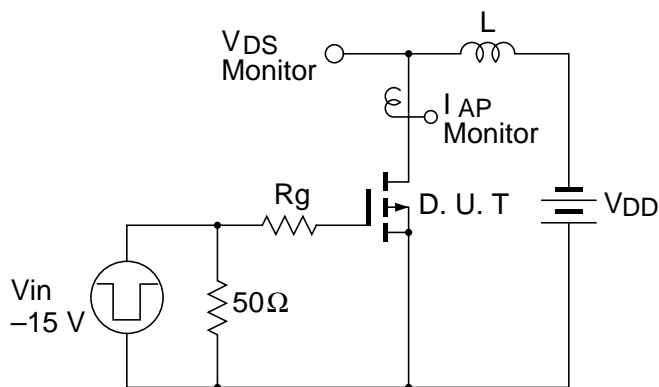




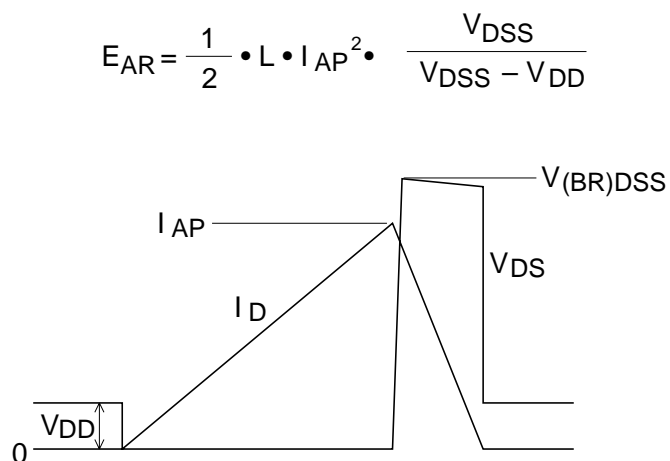


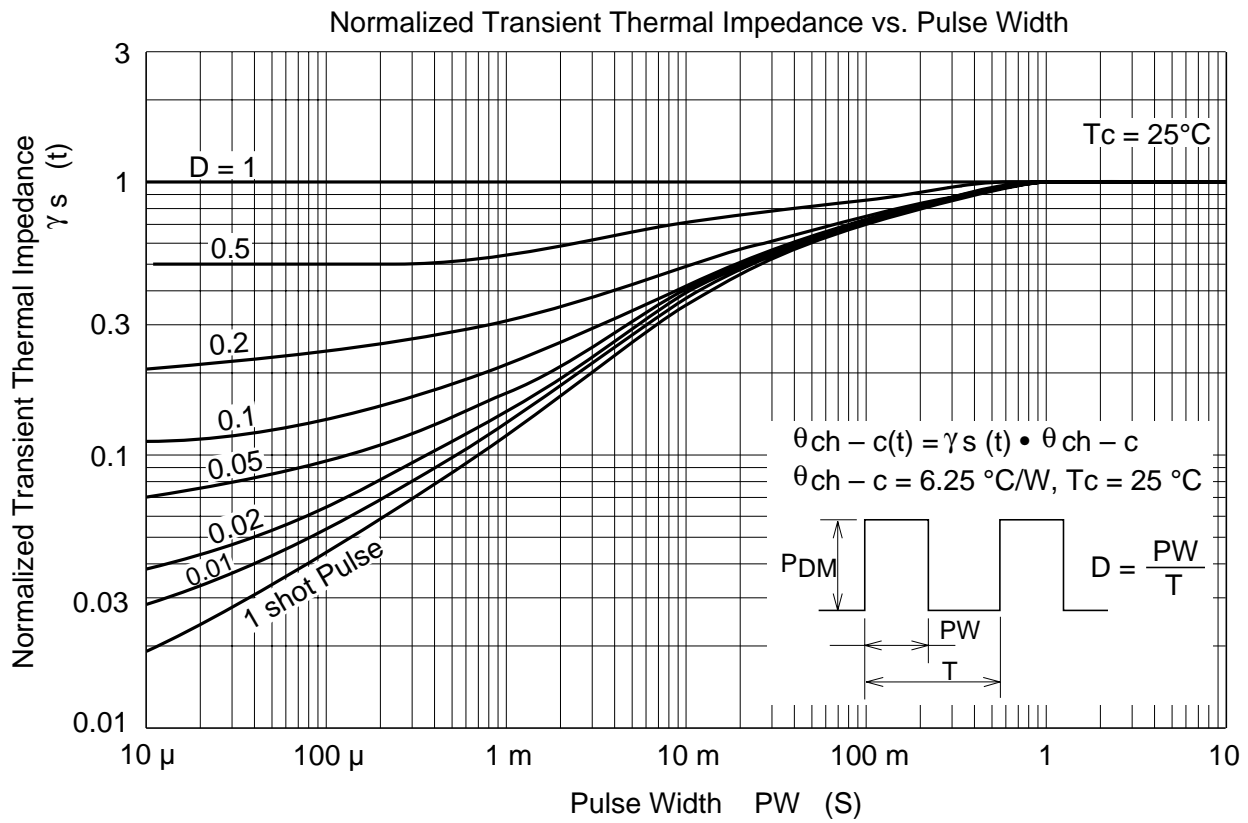


Avalanche Test Circuit

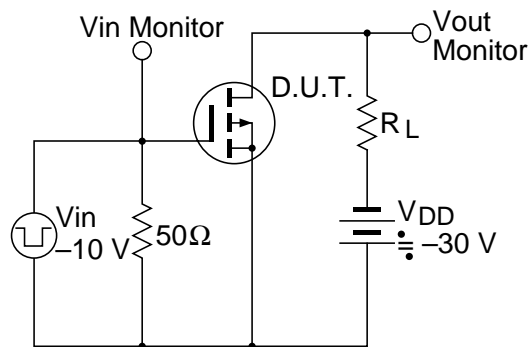


Avalanche Waveform

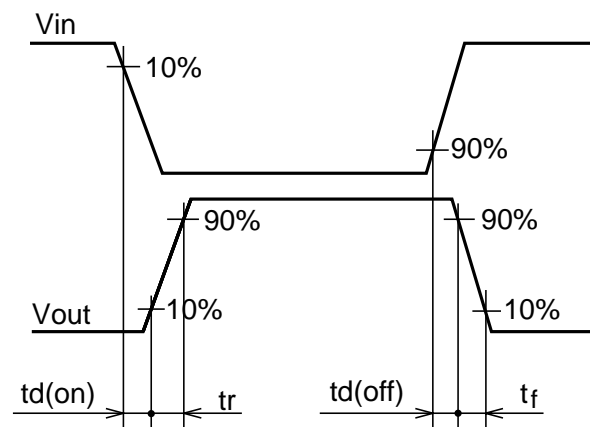




Switching Time Test Circuit

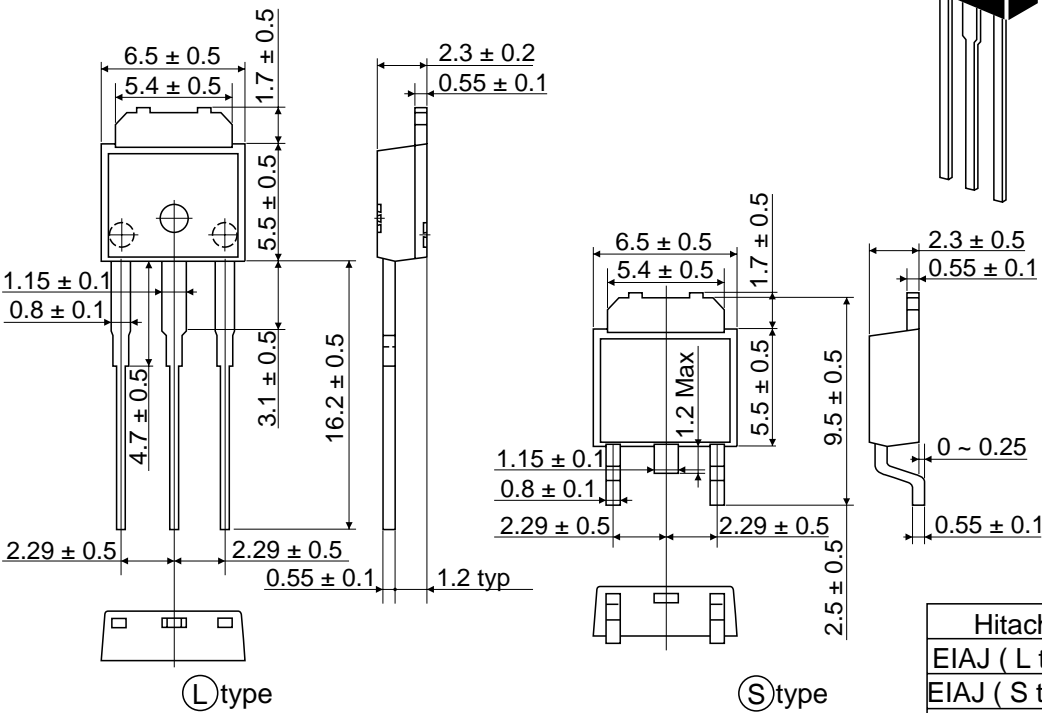


Waveform



Package Dimensions

Unit: mm



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HITACHI

Hitachi, Ltd.

Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

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For further information write to:

Hitachi Semiconductor
(America) Inc.
179 East Tasman Drive,
San Jose, CA 95134
Tel: <1> (408) 433-1990
Fax: <1> (408) 433-0223

Hitachi Europe GmbH
Electronic Components Group
Dornacher StraÙe 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00
Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia Ltd.
Taipei Branch Office
3F, Hung Kuo Building. No.167,
Tun-Hwa North Road, Taipei (105)
Tel: <886> (2) 2718-3666
Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower, World Finance Centre,
Harbour City, Canton Road, Tsim Sha Tsui,
Kowloon, Hong Kong
Tel: <852> (2) 735 9218
Fax: <852> (2) 730 0281
Telex: 40815 HITEC HX

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