

# 2SJ505(L), 2SJ505(S)

Silicon P Channel MOS FET  
High Speed Power Switching

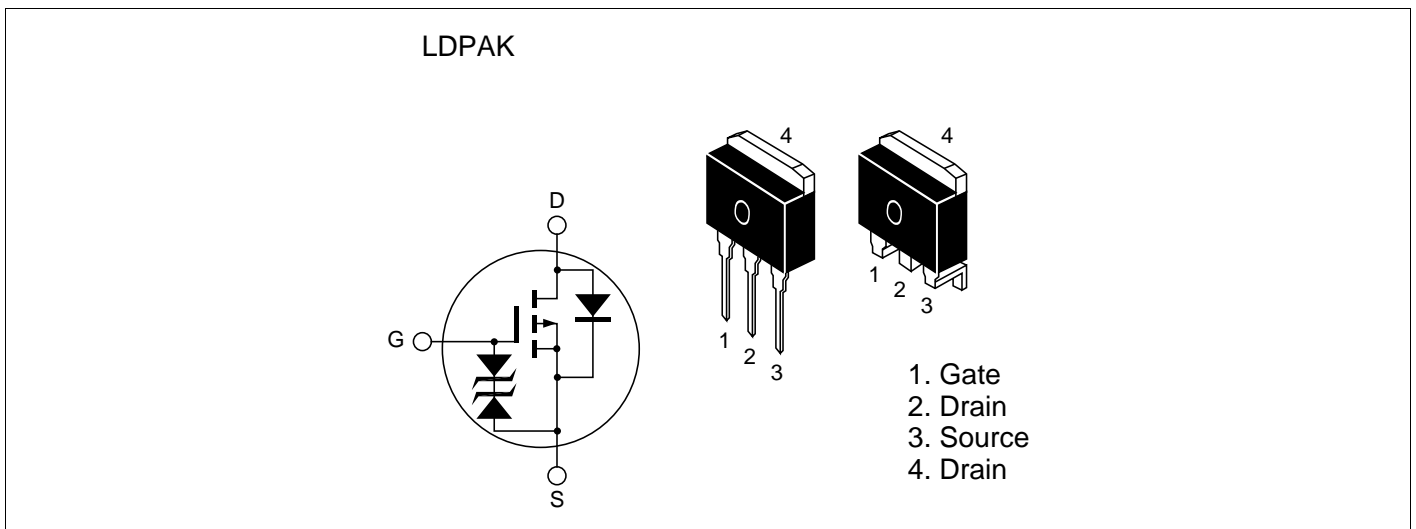
# HITACHI

ADE-208-547  
Target specification 1st. Edition

## Features

- Low on-resistance  
 $R_{DS(on)} = 0.017\Omega$  typ.
- Low drive current.
- 4V gate drive devices.
- High speed switching.

## Outline



## 2SJ505(L), 2SJ505(S)

### Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{DSS}$	-60	V
Gate to source voltage	$V_{GSS}$	±20	V
Drain current	$I_D$	-50	A
Drain peak current	$I_{D(pulse)}^{*1}$	-200	A
Body to drain diode reverse drain current	$I_{DR}$	-50	A
Avalanche current	$I_{AP}^{*3}$	-50	A
Avalanche energy	$E_{AR}^{*3}$	214	mJ
Channel dissipation	$Pch^{*2}$	75	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

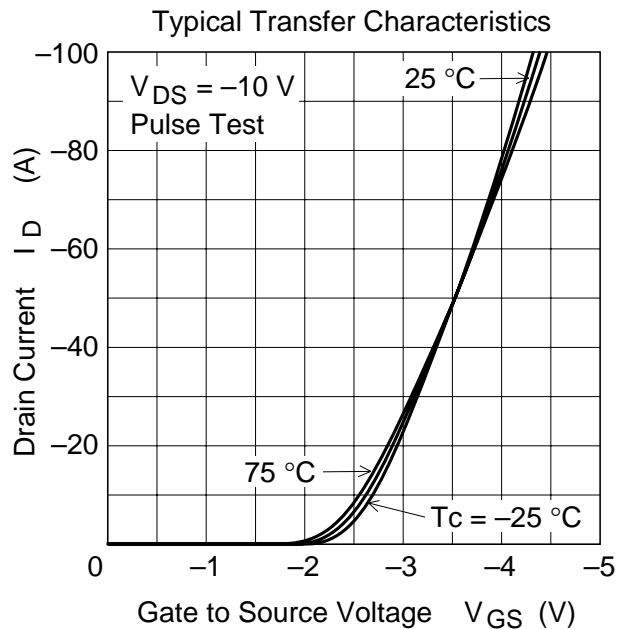
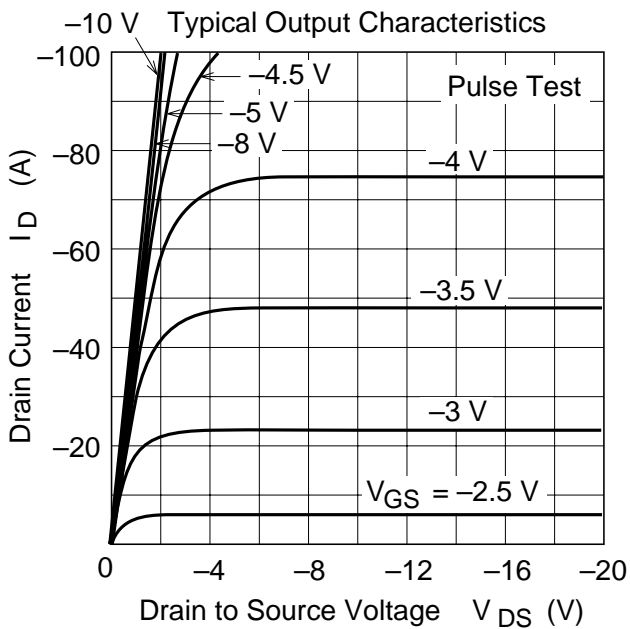
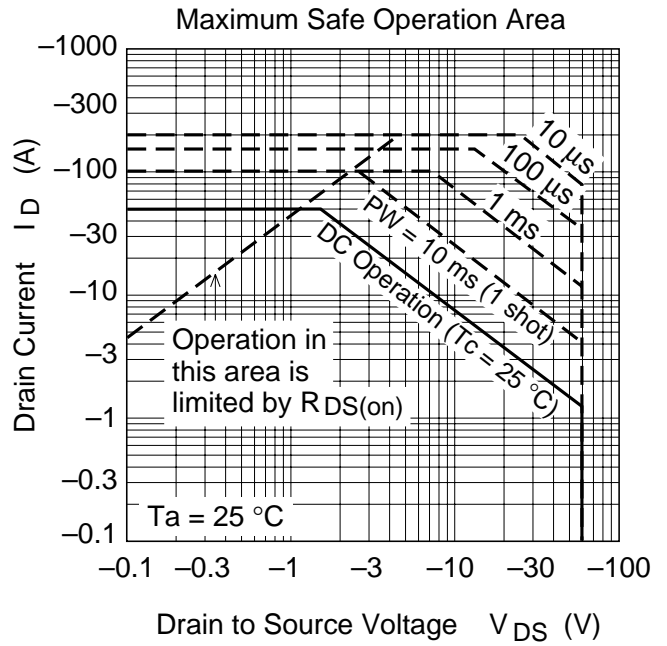
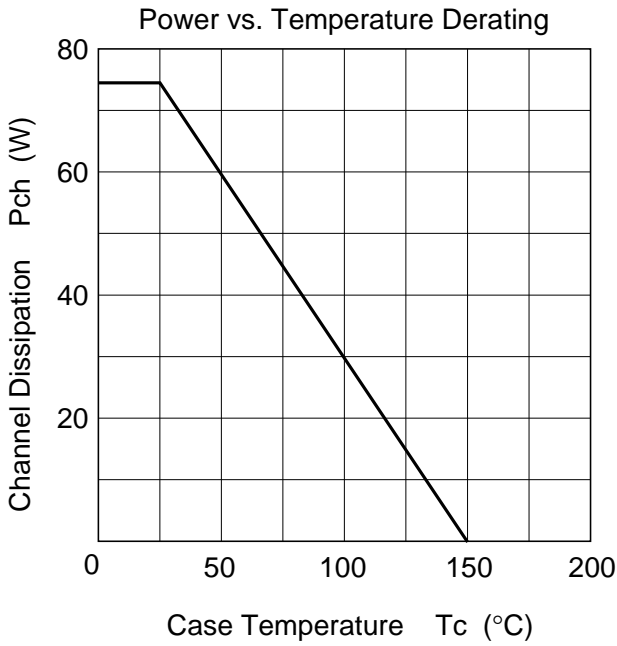
- Notes: 1.  $PW \leq 10\mu s$ , duty cycle  $\leq 1\%$   
2. Value at  $T_c = 25^\circ C$   
3. Value at  $T_a = 25^\circ C$ ,  $R_g \geq 50 \Omega$ ,  $L=100\mu H$

**Electrical Characteristics (Ta = 25°C)**

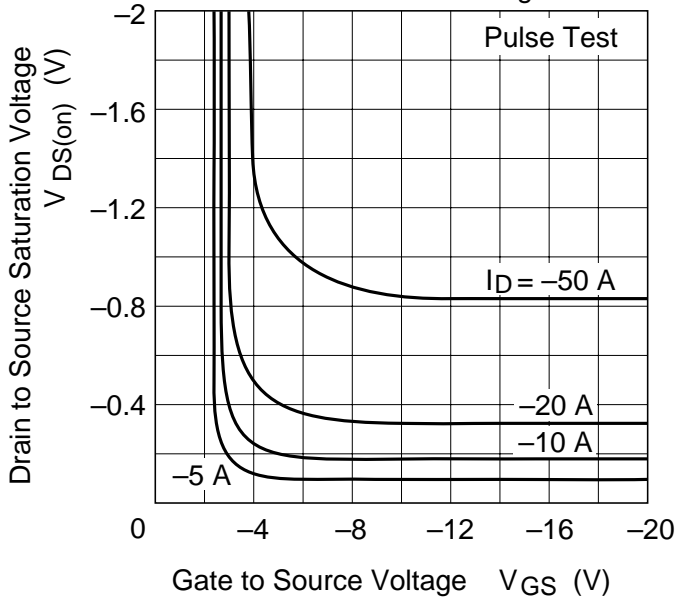
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-60	—	—	V	$I_D = -10\text{mA}, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	$\pm 20$	—	—	V	$I_G = \pm 100\mu\text{A}, V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	-10	$\mu\text{A}$	$V_{DS} = -60\text{V}, V_{GS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	$\pm 10$	$\mu\text{A}$	$V_{GS} = \pm 16\text{V}, V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-1.0	—	-2.0	V	$I_D = -1\text{mA}, V_{DS} = -10\text{V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.017	0.022	$\Omega$	$I_D = -25\text{A}, V_{GS} = -10\text{V}^{*1}$
	$R_{DS(on)}$	—	0.024	0.036	$\Omega$	$I_D = -25\text{A}, V_{GS} = -4\text{V}^{*1}$
Forward transfer admittance	$ y_{fs} $	27	39	—	S	$I_D = 25\text{A}, V_{DS} = 10\text{V}^{*1}$
Input capacitance	$C_{iss}$	—	4100	—	pF	$V_{DS} = -10\text{V}$
Output capacitance	$C_{oss}$	—	2100	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	$C_{rss}$	—	450	—	pF	$f = 1\text{MHz}$
Turn-on delay time	$t_{d(on)}$	—	32	—	ns	$V_{GS} = -10\text{V}, I_D = -10\text{A}$
Rise time	$t_r$	—	225	—	ns	$R_L = 3\Omega$
Turn-off delay time	$t_{d(off)}$	—	530	—	ns	
Fall time	$t_f$	—	330	—	ns	
Body to drain diode forward voltage	$V_{DF}$	—	-1.1	—	V	$I_F = -50\text{A}, V_{GS} = 0$
Body to drain diode reverse recovery time	$t_{rr}$	—	110	—	ns	$I_F = -50\text{A}, V_{GS} = 0$ $di_F/dt = 50\text{A}/\mu\text{s}$

Note: 1. Pulse test

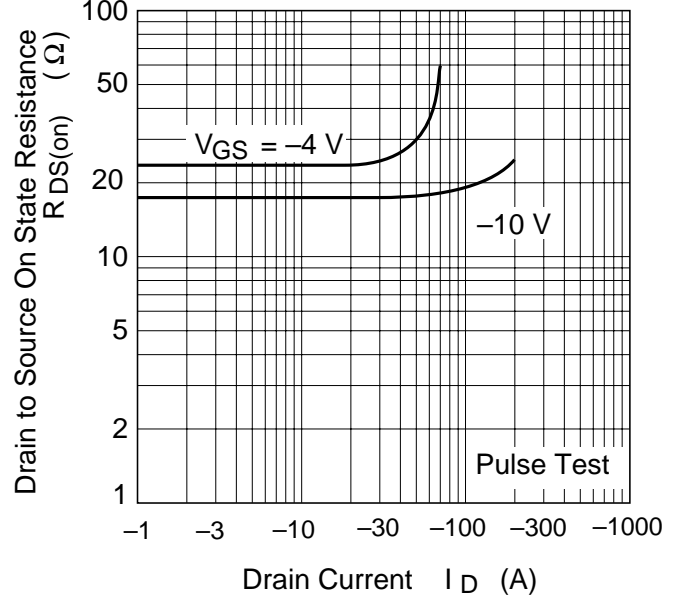
## Main Characteristics



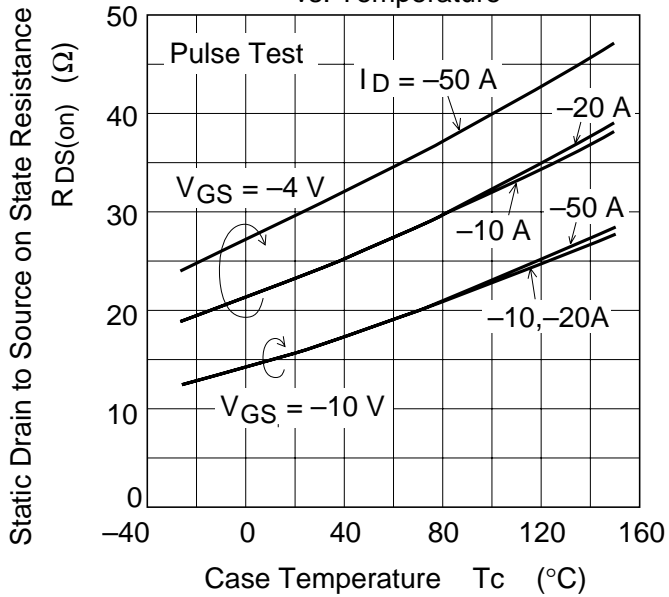
Drain to Source Saturation Voltage vs. Gate to Source Voltage



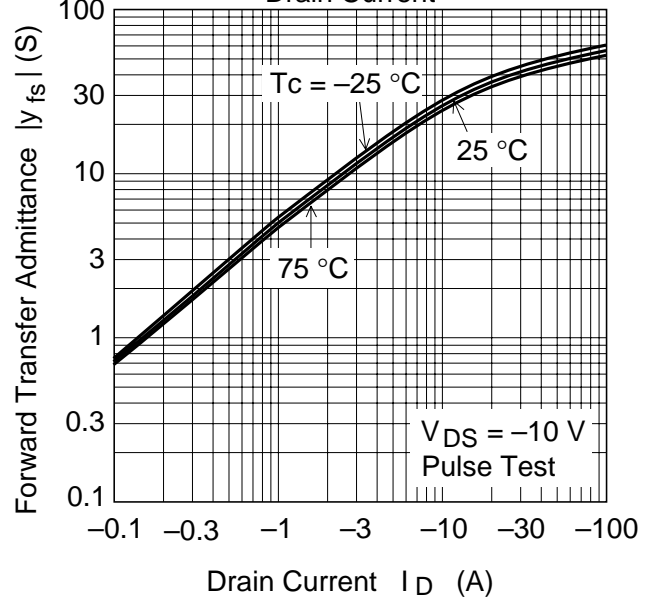
Static Drain to Source on State Resistance vs. Drain Current



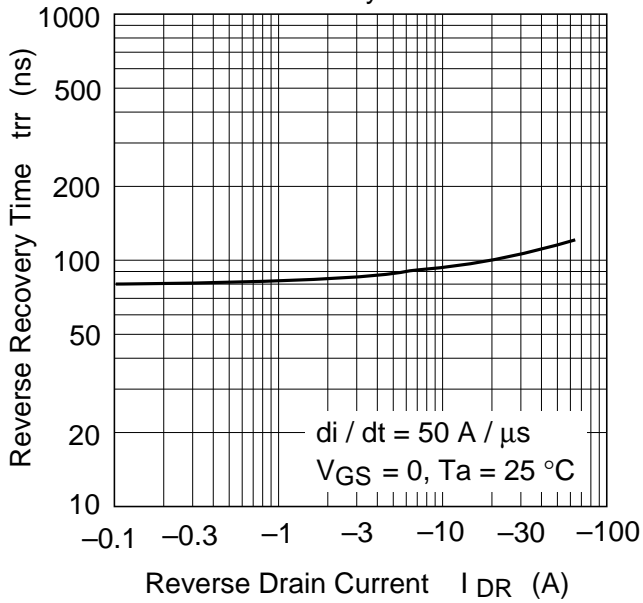
Static Drain to Source on State Resistance vs. Temperature



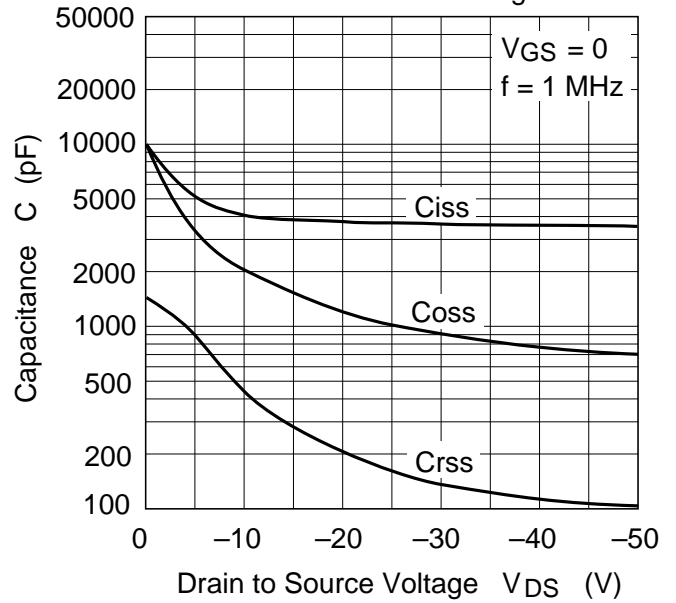
Forward Transfer Admittance vs. Drain Current



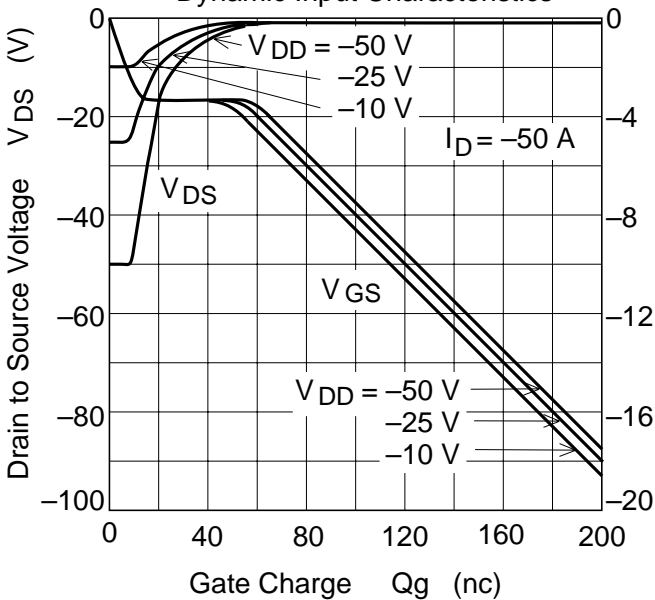
Body to Drain Diode Reverse Recovery Time



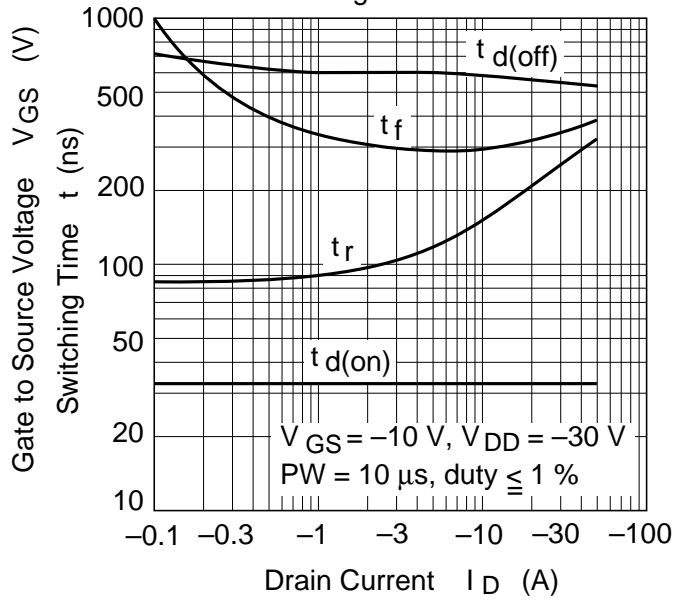
Typical Capacitance vs. Drain to Source Voltage

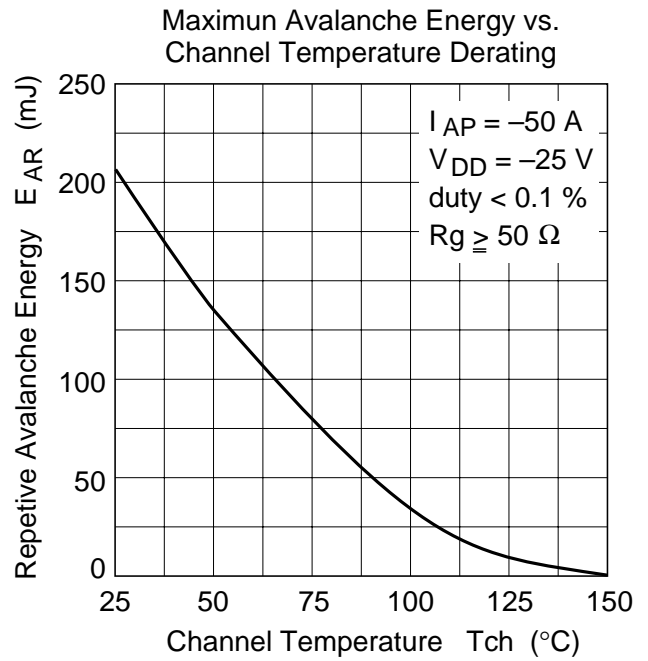
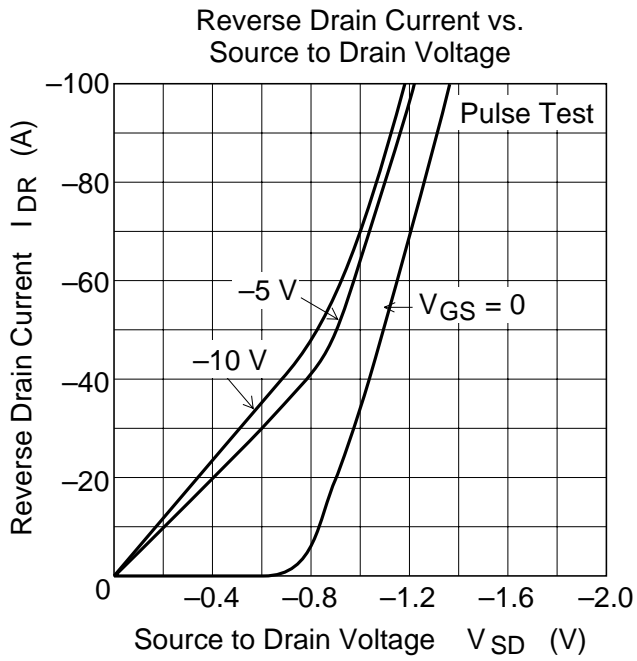


Dynamic Input Characteristics

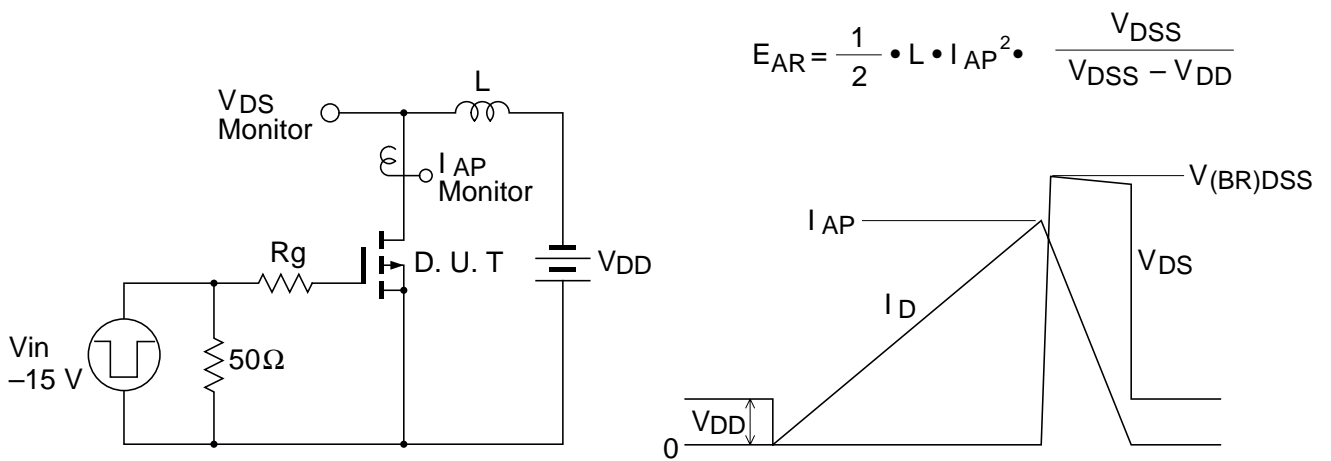


Switching Characteristics

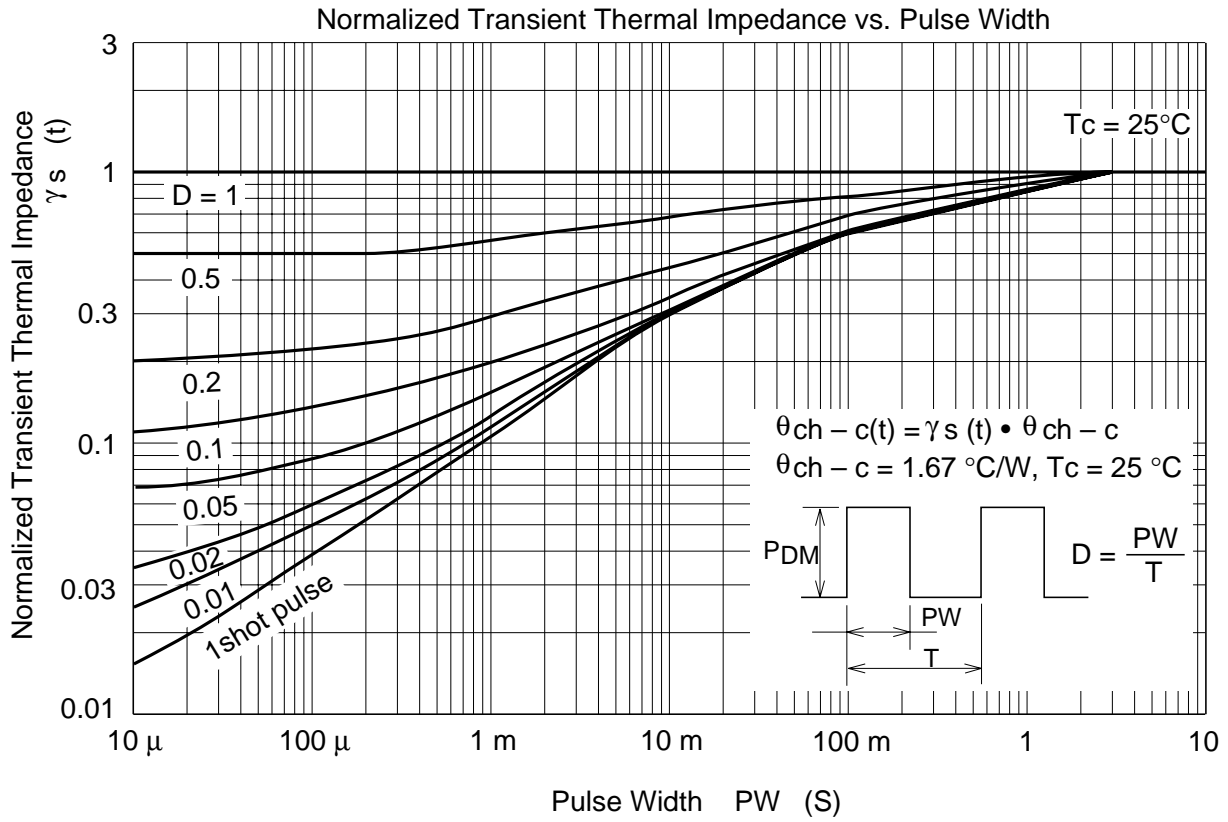




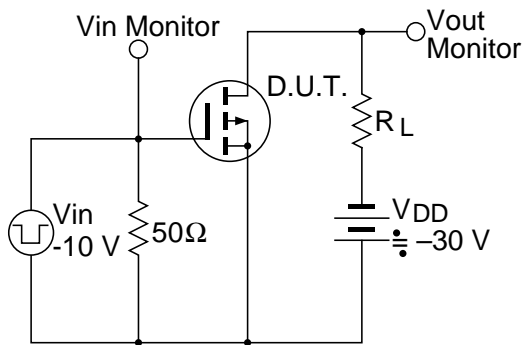
Avalanche Test Circuit and Waveform



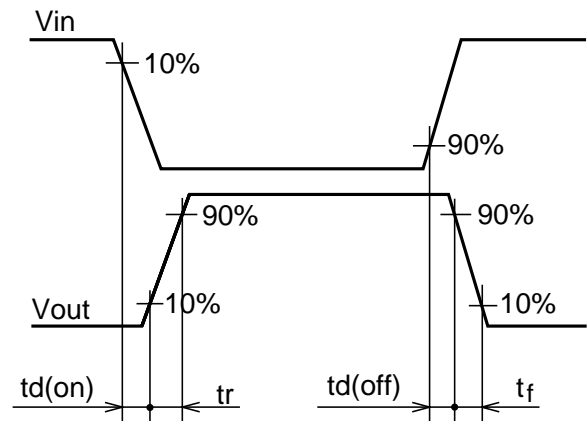
$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



Switching Time Test Circuit



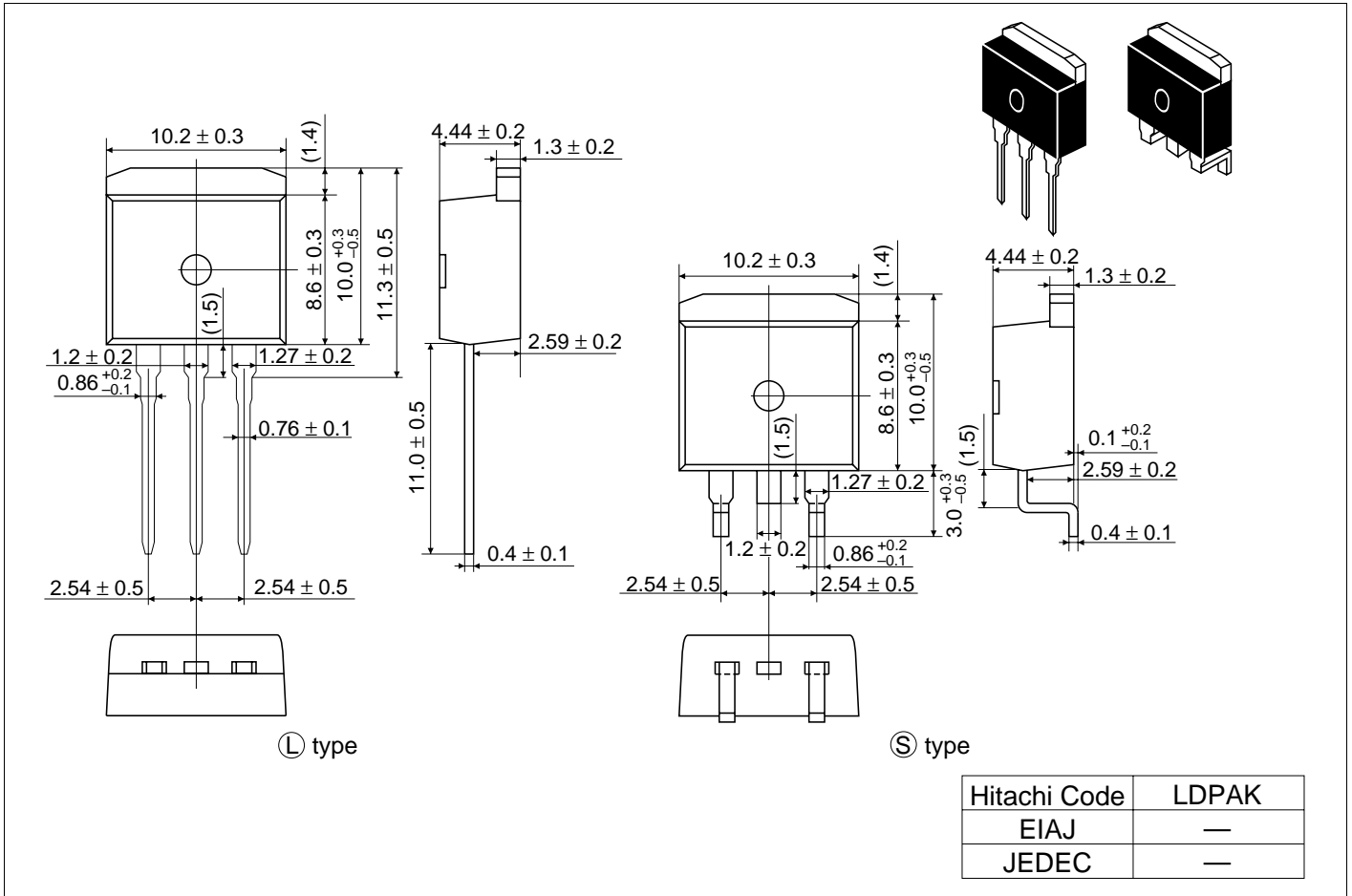
Waveforms





Package Dimensions

Unit: mm



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