
2SK1835

Silicon N-Channel MOS FET

HITACHI

Application

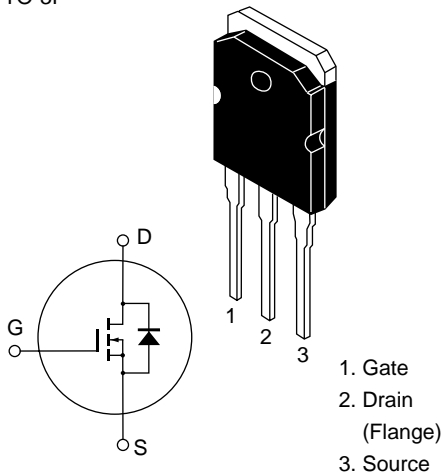
High speed power switching

Features

- High breakdown voltage ($V_{DSS} = 1500V$)
- High speed switching
- Low drive current
- No secondary breakdown
- Suitable for switching regulator

Outline and Equivalent Circuit

TO-3P



Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	1500	V
Gate to source voltage	V_{GSS}	± 20	V
Drain current	I_D	4	A
Drain peak current	$I_{D(pulse)}^{*1}$	10	A
Body to drain diode reverse drain current	I_{DR}	4	A
Channel dissipation	Pch^{*2}	125	W
Channel temperature	Tch	150	$^\circ\text{C}$
Storage temperature	$Tstg$	-55 to +150	$^\circ\text{C}$

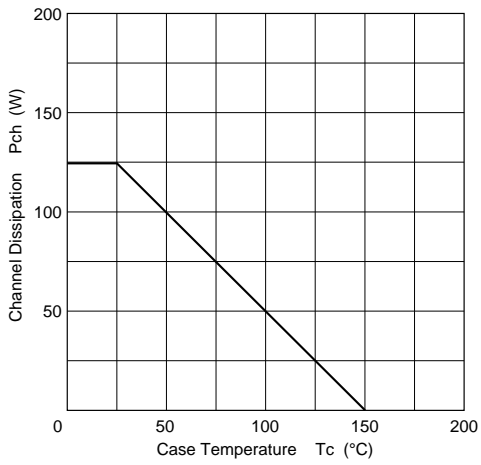
- Notes 1. $PW \leq 10 \mu\text{s}$, duty cycle $\leq 1\%$
2. Value at $T_c = 25^\circ\text{C}$

Electrical Characteristics (Ta = 25°C)

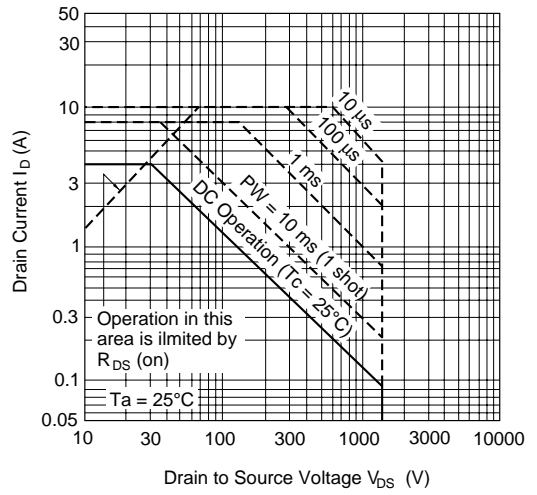
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	1500	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 1	μA	$V_{GS} = \pm 20 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	500	μA	$V_{DS} = 1200 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	4.0	V	$I_D = 1 \text{ mA}$, $V_{DS} = 10 \text{ V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	4.6	7.0	Ω	$I_D = 2 \text{ A}$ $V_{GS} = 15 \text{ V}^{*1}$
Forward transfer admittance	$ y_{fs} $	0.9	1.4	—	S	$I_D = 2 \text{ A}$ $V_{DS} = 20 \text{ V}^{*1}$
Input capacitance	C_{iss}	—	1700	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	C_{oss}	—	230	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	100	—	pF	$f = 1 \text{ MHz}$
Turn-on delay time	$t_{d(on)}$	—	25	—	ns	$I_D = 2 \text{ A}$
Rise time	t_r	—	80	—	ns	$V_{GS} = 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	230	—	ns	$R_L = 15 \Omega$
Fall time	t_f	—	80	—	ns	
Body to drain diode forward voltage	V_{DF}	—	0.85	—	V	$I_F = 4 \text{ A}$, $V_{GS} = 0$
Body to drain diode reverse recovery time	t_{rr}	—	2500	—	ns	$I_F = 4 \text{ A}$, $V_{GS} = 0$, $di_F / dt = 100 \text{ A} / \mu\text{s}$

Note 1. Pulse Test

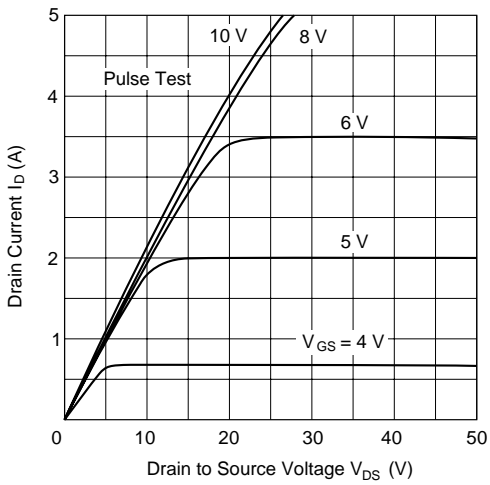
Power vs. Temperature Derating



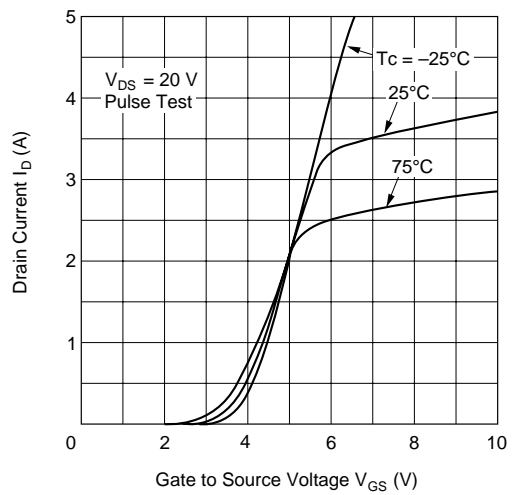
Maximum Safe Operation Area



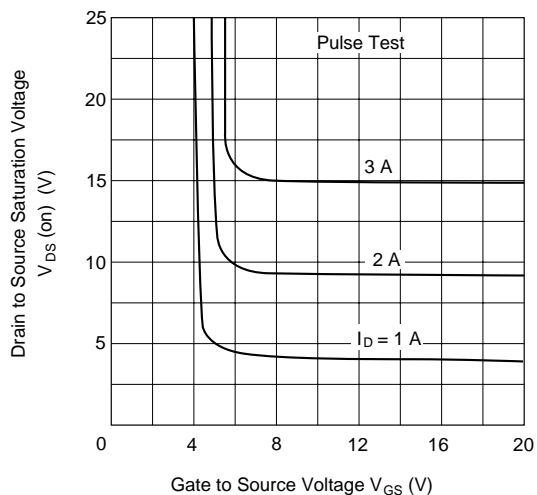
Typical Output Characteristics



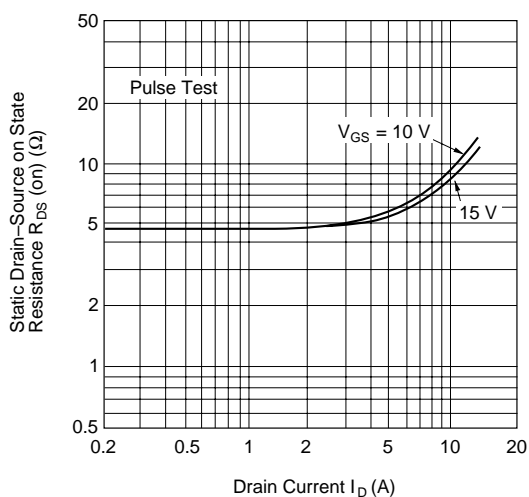
Typical Transfer Characteristics



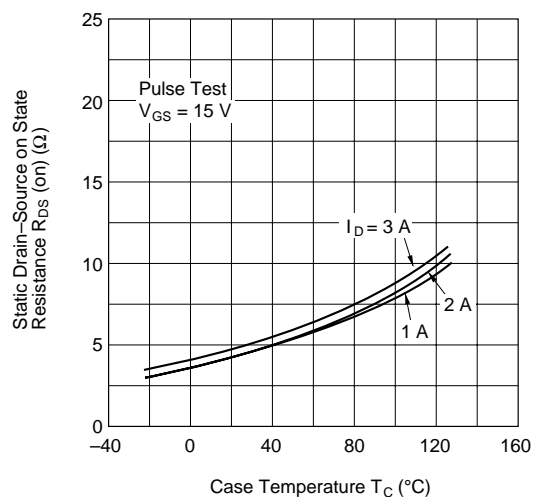
Drain to Source Saturation Voltage vs. Gate to Source Voltage



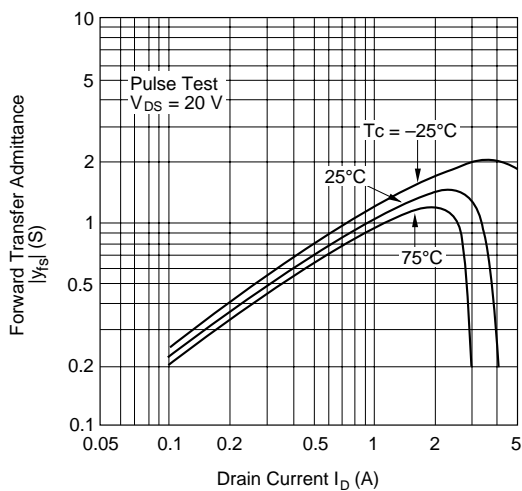
Static Drain to Source on State Resistance vs. Drain Current



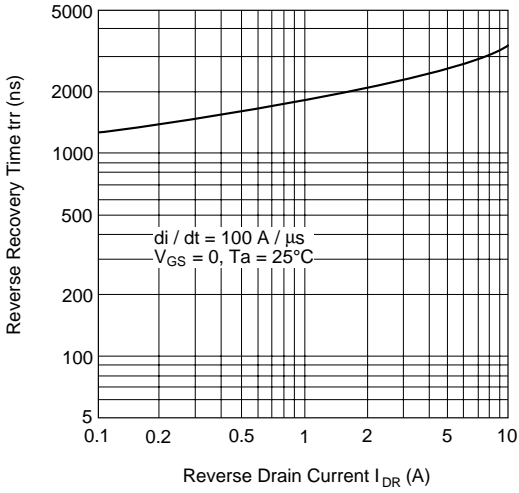
Static Drain to Source on State Resistance vs. Temperature



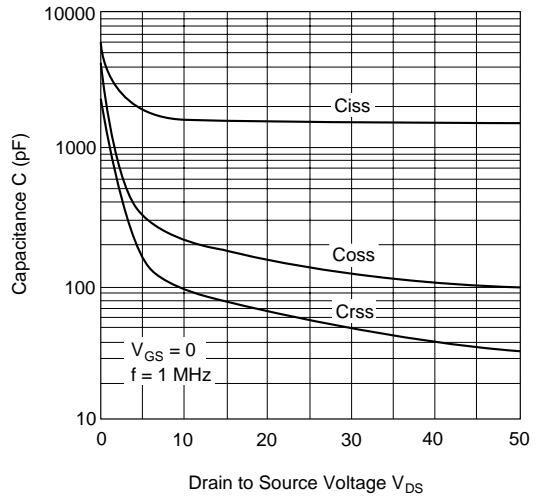
Forward Transfer Admittance vs. Drain Current



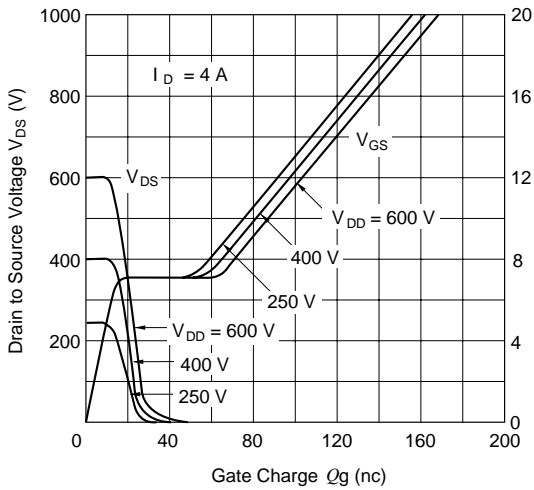
Body to Drain Diode Reverse Recovery Time



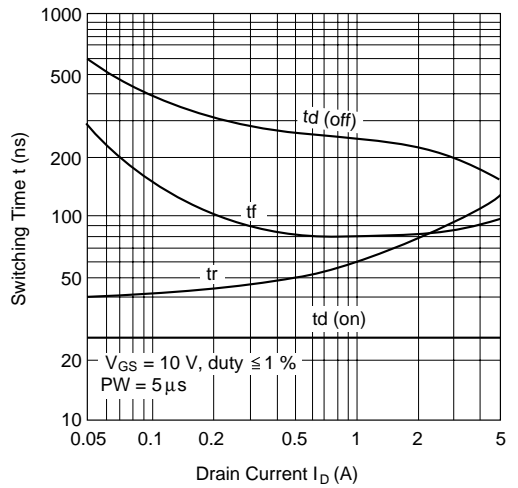
Typical Capacitance vs. Drain to Source Voltage



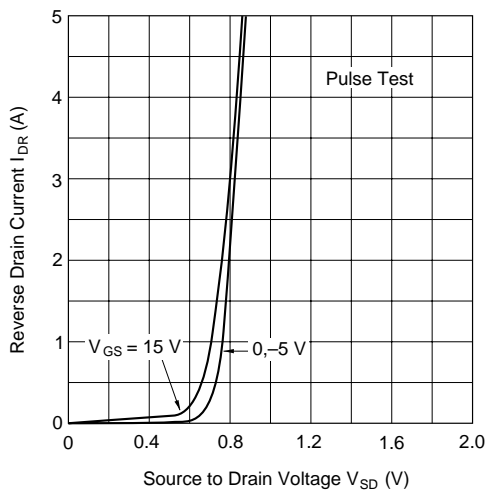
Dynamic Input Characteristics



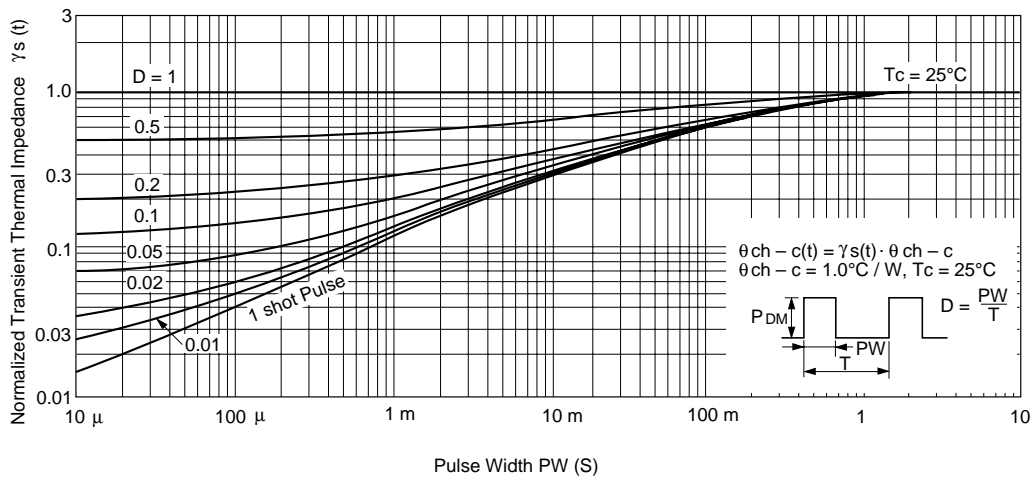
Switching Characteristics



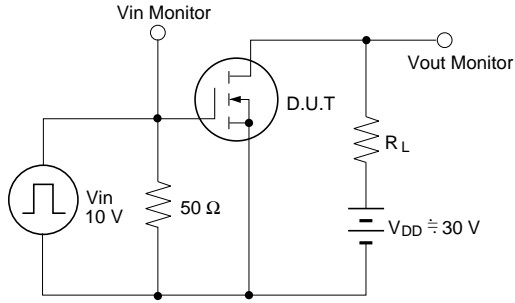
Reverse Drain Current vs. Source to Drain Voltage



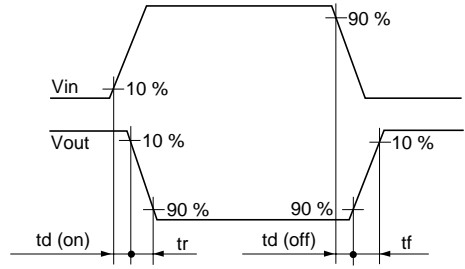
Normalized Transien Thermal Impedance vs. Pulse Width

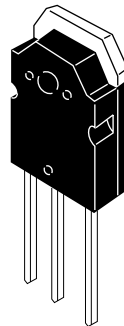
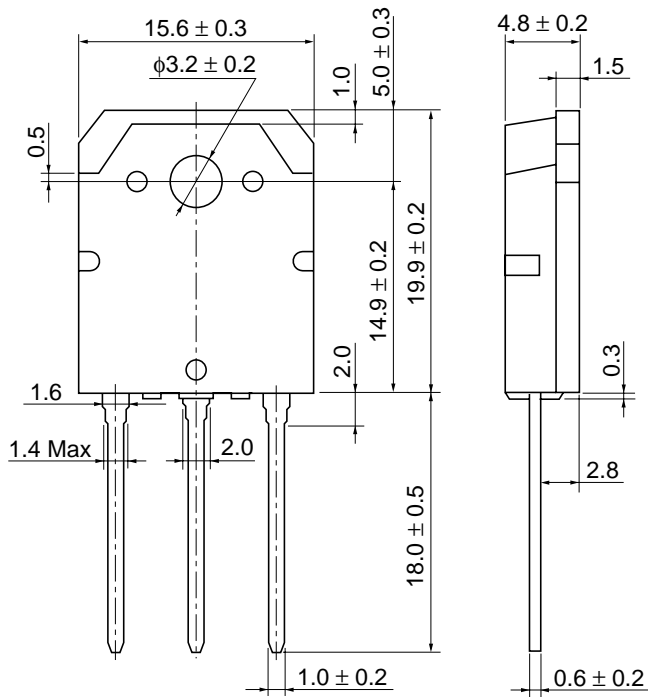


Switching Time Test Circuit



Waveforms





Hitachi Code	TO-3P
JEDEC	—
EIAJ	Conforms
Weight (reference value)	5.0 g

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