Silicon P Channel MOS FET Series Power Switching

HITACHI

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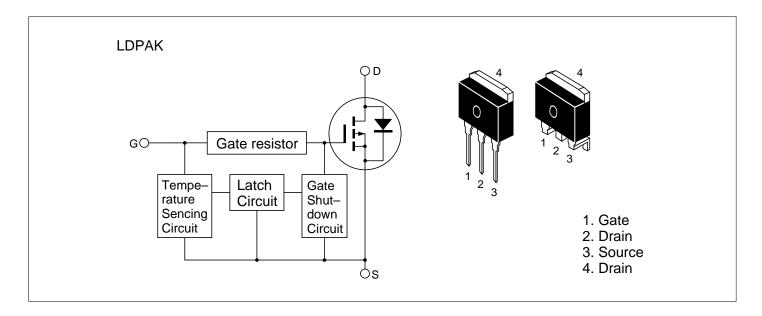
Features

This FET has the over temperature shut-down capability sensing to the junction temperature.

This FET has the built–in over temperature shut–down circuit in the gate area. And this circuit operation to shut–down the gate voltage in case of high junction temperature like applying over power consumption, over current etc.

- Logic level operation (-4 to -6 V Gate drive)
- High endurance capability against to the short circuit
- Built-in the over temperature shut-down circuit
- Latch type shut–down operation (Need 0 voltage recovery)

Outline





Absolute Maximum Ratings ($Ta = 25^{\circ}C$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V _{DSS}	-60	V
Gate to source voltage	V _{GSS+}	-16	V
Gate to source voltage	V _{GSS-}	3	V
Drain current	I _D	-15	A
Drain peak current	Note1 D(pulse)	-30	А
Body-drain diode reverse drain current	I _{DR}	-15	A
Channel dissipation	Pch Note2	50	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

Note: 1. PW \leq 10µs, duty cycle \leq 1 %

2. Value at $Tc = 25^{\circ}C$

Typical Operation Characteristics

Item	Symbol	Min	Тур	Max	Unit	Test Conditions
Input voltage	V _{IH}	-3.5	_	_	V	
	V _{IL}			-1.2	V	
Input current	I _{IH1}			-100	μA	$Vi = -8V, V_{DS} = 0$
(Gate non shut down)	I _{IH2}		_	-50	μA	$Vi = -3.5V, V_{DS} = 0$
	I _{IL}		_	-1	μA	$Vi = -1.2V, V_{DS} = 0$
Input current	I _{IH(sd)1}		-0.8		mA	$Vi = -8V, V_{DS} = 0$
(Gate shut down)	I _{IH(sd)2}		-0.35		mA	$Vi = -3.5V, V_{DS} = 0$
Shut down temperature	T _{sd}		175		°C	Channel temperature
Gate operation voltage	V _{OP}	-3.5		-13	V	

Electrical Characteristics (Ta = 25° C)

Item	Symbol	Min	Тур	Max	Unit	Test Conditions
Drain current	I _{D1}	-7			А	$V_{GS} = -3.5V, V_{DS} = -2V$
Drain current	I _{D2}			-10	mA	$V_{GS} = -1.2V, V_{DS} = -2V$
Drain to source breakdown voltage	V _{(BR)DSS}	-60			V	$I_{\rm D} = -10 {\rm mA}, V_{\rm GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS+}$	-16	_	_	V	$I_{g} = -100\mu A, V_{DS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS-}$	3	_	_	V	$I_{g} = 100 \mu A, V_{DS} = 0$
Gate to source leak current	I _{GSS+1}			-100	μA	$V_{\rm GS} = -8V, V_{\rm DS} = 0$
	I _{GSS+2}			-50	μA	$V_{GS} = -3.5V, V_{DS} = 0$
	I _{GSS+3}			-1	μA	$V_{GS} = -1.2V, V_{DS} = 0$
	I _{GSS-}			100	μA	$V_{GS} = 2.4 V, V_{DS} = 0$
Input current (shut down)	I _{GS(op)1}		-0.8		mA	$V_{\rm GS} = -8V, V_{\rm DS} = 0$
	I _{GS(op)1}		-0.35		mA	$V_{GS} = -3.5V, V_{DS} = 0$
Zero gate voltege drain current	I _{DSS}	_		-250	μΑ	$V_{\rm DS} = -50$ V, $V_{\rm GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-1.1		-2.25	V	$I_{\rm D} = -1 {\rm mA}, V_{\rm DS} = -10 {\rm V}$
Static drain to source on state resistance	R _{DS(on)}		100	130	mΩ	$I_{D} = -7.5A, V_{GS} = -4V^{Note3}$
Static drain to source on state resistance	R _{DS(on)}		70	90	mΩ	$I_{\rm D} = -7.5A$ $V_{\rm GS} = -10V^{\rm Note3}$
Forward transfer admittance	y _{fs}	5	10		S	$I_{\rm D} = -7.5$ A, $V_{\rm DS} = -10 V^{\rm Note3}$
Output capacitance	Coss		610		pF	$V_{DS} = -10V$, $V_{GS} = 0$
					•	f = 1 MHz
Turn-on delay time	t _{d(on)}		7.5		μs	$I_{\rm D} = -7.5$ A, $V_{\rm GS} = -5$ V
Rise time	t _r		36		μs	$R_{L} = 4\Omega$
Turn-off delay time	t _{d(off)}	_	32		μs	
Fall time	t _f		29		μs	
Body-drain diode forward	V _{DF}		-1.0		V	$I_{\rm F} = -15$ A, $V_{\rm GS} = 0$
voltage						
Body-drain diode reverse	t _{rr}		200		ns	$I_{\rm F} = -15$ A, $V_{\rm GS} = 0$
recovery time						diF/ dt =50A/µs
Over load shut down	t _{os1}		3.7		ms	$V_{GS} = -5V, V_{DD} = -12V$
operation time Note4	t _{os2}		1		ms	$V_{\rm GS} = -5V, V_{\rm DD} = -24V$
Noto: 2 Dulas test						

Note: 3. Pulse test

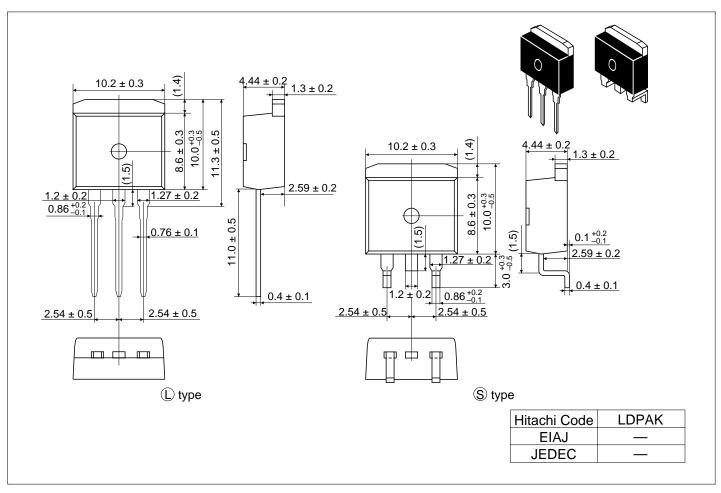
4. Including the junction temperature rise of the over loaded condition.

• See characteristics curve of HAF1001.

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Package Dimensions

Unit: mm



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