HM658512A Series

4 M PSRAM (512-kword × 8-bit)
2 k Refresh

HITACHI

ADE-203-218C(Z)
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Description

The Hitachi HM658512A is a CMOS pseudo static RAM organized 512-kword × 8-bit. It realizes higher density, higher performance and low power consumption by employing 0.8 µm Hi-CMOS process technology.

It offers low power data retention by self refresh mode. It also offers easy non multiplexed address interface and easy refresh functions. HM658512A is suitable for handy systems which work with battery back-up systems.

The device is packaged in a small 525-mil SOP (460-mil body SOP) or a 8 × 20 mm TSOP with thickness of 1.2 mm, or a 600-mil plastic DIP. High density custom cards made of Tape Carrier Packages are also available.

Features

- Single 5 V (±10%)
- High speed
  - Access time
    $\overline{CE}$ access time: 70/80/100 ns (max)
  - Cycle time
    Random read/write cycle time:
    115/130/160 ns (min)
- Low power
  - Active: 250 mW (typ)
  - Standby: 200 µW (typ)
- Directly TTL compatible
  All inputs and outputs
- Simple address configuration
  Non multiplexed address
- Refresh cycle
  - 2048 refresh cycles: 32 ms

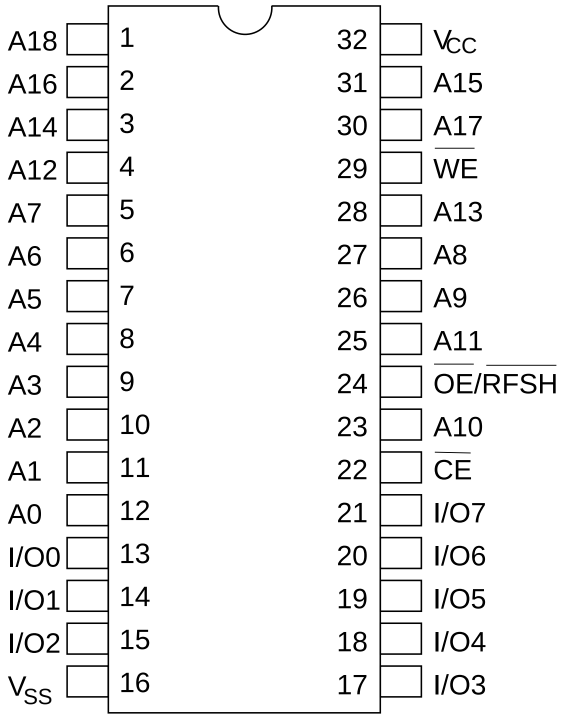
- Easy refresh functions
  Address refresh
  Automatic refresh
  Self refresh

Ordering Information

Type No.	Access time	Package
HM658512ALP-7	70 ns	600-mil 32-pin plastic DIP (DP-32)
HM658512ALP-8	80 ns	
HM658512ALP-10	100 ns	
HM658512ALP-7V	70 ns	
HM658512ALP-8V	80 ns	
HM658512ALP-10V	100 ns	
HM658512ALFP-7	70 ns	525-mil 32-pin plastic SOP (FP-32D)
HM658512ALFP-8	80 ns	
HM658512ALFP-10	100 ns	
HM658512ALFP-7V	70 ns	
HM658512ALFP-8V	80 ns	
HM658512ALFP-10V	100 ns	
HM658512ALTT-7	70 ns	400-mil 32-pin plastic TSOP (TTP-32D)
HM658512ALTT-8	80 ns	
HM658512ALTT-10	100 ns	
HM658512ALTT-7V	70 ns	
HM658512ALTT-8V	80 ns	
HM658512ALTT-10V	100 ns	
HM658512ALRR-7	70 ns	400-mil 32-pin plastic TSOP (TTP-32DR)
HM658512ALRR-8	80 ns	
HM658512ALRR-10	100 ns	
HM658512ALRR-7V	70 ns	
HM658512ALRR-8V	80 ns	
HM658512ALRR-10V	100 ns	

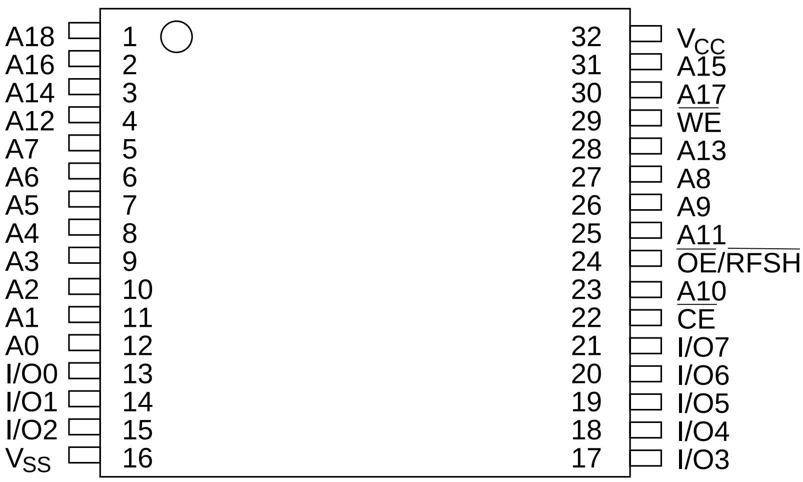
Pin Arrangement

HM658512ALP/ALFP Series



(Top view)

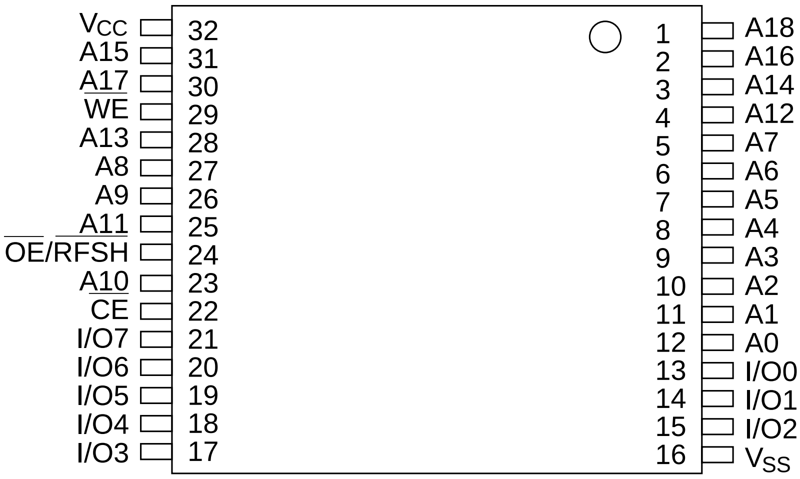
HM658512ALTT Series



(Top view)

Pin Arrangement (cont.)

HM658512ALRR Series

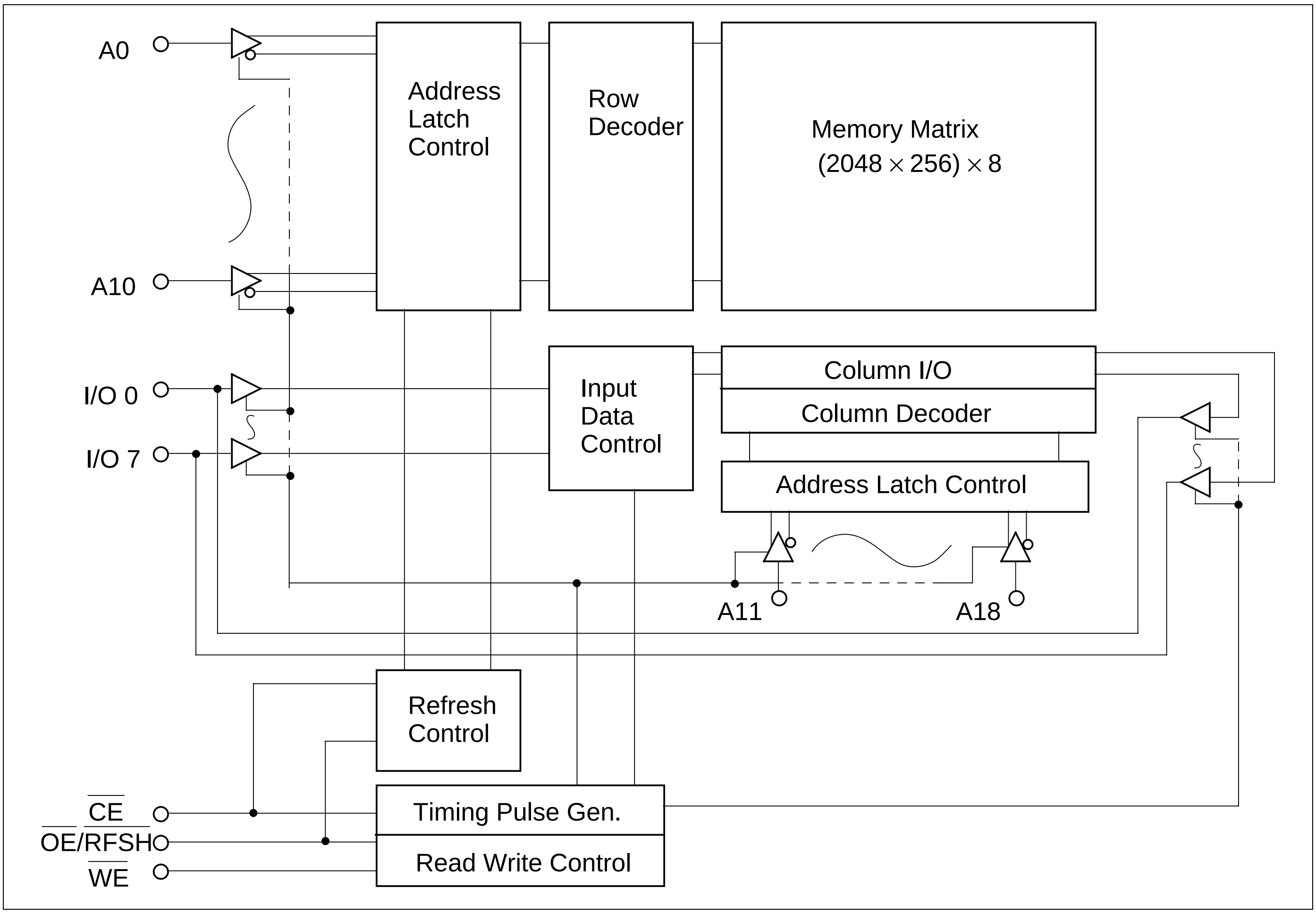


(Top view)

Pin Description

Pin name	Function
A0 to A18	Address
I/O0 to I/O7	Input/Output
$\overline{CE}$	Chip enable
$\overline{OE}$/$\overline{RFSH}$	Output enable/Refresh
$\overline{WE}$	Write enable
V_{CC}	Power supply
V_{SS}	Ground

Block Diagram



Pin Functions

$\overline{CE}$: Chip Enable (Input)

$\overline{CE}$ is a basic clock. RAM is active when $\overline{CE}$ is low, and is on standby when $\overline{CE}$ is high.

A0 to A18: Address Inputs (Input)

A0 to A10 are row addresses and A11 to A18 are column addresses. The entire addresses A0 to A18 are fetched into RAM by the falling edge of $\overline{CE}$.

$\overline{OE}/\overline{RFSH}$: Output Enable/Refresh (Input)

This pin has two functions. Basically it works as $\overline{OE}$ when $\overline{CE}$ is low, and as $\overline{RFSH}$ when $\overline{CE}$ is high (in standby mode). After a read or write cycle finishes, refresh does not start if $\overline{CE}$ goes high while $\overline{OE}/\overline{RFSH}$ is held low. In order to start a refresh in standby mode, $\overline{OE}/\overline{RFSH}$ must go high to reset the refresh circuits of the RAM. After the refresh circuits are reset, the refresh starts when $\overline{OE}/\overline{RFSH}$ goes low.

I/O0 to I/O7: Input/Output (Inputs and Outputs) These pins are data I/O pins.

$\overline{WE}$: Write Enable (Input)

RAM is in write mode when $\overline{WE}$ is low, and is in read mode when $\overline{WE}$ is high. I/O data is fetched into RAM by the rising edge of $\overline{WE}$ or $\overline{CE}$ (earlier timing) and the data is written into memory cells.

Refresh

There are three refresh modes : address refresh, automatic refresh and self refresh.

(1) Address refresh: Data is refreshed by accessing all 2048 row addresses every 32 ms. A read is one method of accessing those addresses. Each row address (2048 addresses of A0 to A10)must be read at least once every 32 ms. In address refresh mode, $\overline{OE}/\overline{RFSH}$ can remain high. In this case, the I/O pins remain at high impedance, but the refresh is done within RAM.

(2) Automatic refresh: Instead of address refresh, automatic refresh can be used. RAM goes to automatic refresh mode if $\overline{OE}/\overline{RFSH}$ falls while $\overline{CE}$ is high and it remains low for at least t_{FAP}. One automatic refresh cycle is executed by one low pulse of $\overline{OE}/\overline{RFSH}$. It is not necessary to input the refresh address from outside since it is generated internally by an on-chip address counter. 2048 automatic refresh cycles must be done every 32 ms.

(3) Self refresh: Self refresh mode is suitable for data retention by battery. In standby mode, a self refresh starts automatically when $\overline{OE}/\overline{RFSH}$ stays low for more than 8 µs. Refresh addresses are automatically specified by the on-chip address counter, and the refresh period is determined by the on-chip timer.

Automatic refresh and self refresh are distinguished from each other by the width of the $\overline{OE}/\overline{RFSH}$ low pulse in standby mode. If the $\overline{OE}/\overline{RFSH}$ low pulse is wider than 8 µs, RAM becomes into self refresh mode; if the $\overline{OE}/\overline{RFSH}$ low pulse is less than 8 µs, it is recognized as an automatic refresh instruction.

At the end of self refresh, refresh reset time (t_{RFS}) is required to reset the internal self refresh operation of the RAM. During t_{RFS}, $\overline{\text{CE}}$ and $\overline{\text{OE}}/\overline{\text{RFSH}}$ must be kept high. If auto refresh follows self refresh, low transition of $\overline{\text{OE}}/\overline{\text{RFSH}}$ at the beginning of automatic refresh must not occur during t_{RFS} period.

Notes on Using the HM658512A

Since pseudo static RAM consists of dynamic circuits like DRAM, its clock pins are more noise-sensitive than conventional SRAM's.

(1) If a short $\overline{\text{CE}}$ pulse of a width less than t_{CE} min is applied to RAM, an incomplete read occurs and stored data may be destroyed. Make sure that $\overline{\text{CE}}$ low pulses of less than t_{CE} min are inhibited. Note that a 10 ns $\overline{\text{CE}}$ low pulse may sometimes occur owing to the gate delay on the board if the $\overline{\text{CE}}$ signal is generated by the decoding of higher address signals on the board. Avoid these short pulses.

(2) $\overline{\text{OE}}/\overline{\text{RFSH}}$ works as refresh control in standby mode. A short $\overline{\text{OE}}/\overline{\text{RFSH}}$ low pulse may cause an incomplete refresh that will destroy data. Make sure that $\overline{\text{OE}}/\overline{\text{RFSH}}$ low pulse of less than t_{FAP} min are also inhibited.

(3) t_{OHC} and t_{OCD} are the timing specs which distinguish the $\overline{\text{OE}}$ function of $\overline{\text{OE}}/\overline{\text{RFSH}}$ from the $\overline{\text{RFSH}}$ function. The t_{OHC} and t_{OCD} specs must be strictly maintained.

(4) Start the HM658512A operating by executing at least eight initial cycles (dummy cycles) at least 100 µs after the power voltage reaches 4.5 V-5.5 V after power-on.

Function Table

$\overline{\text{CE}}$	$\overline{\text{OE}}/\overline{\text{RFSH}}$	$\overline{\text{WE}}$	I/O pin	Mode
L	L	H	Dout	Read
L	X	L	High-Z	Write
L	H	H	High-Z	—
H	L	X	High-Z	Refresh
H	H	X	High-Z	Standby

Note: X means H or L.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Terminal voltage with respect to V_{SS}	V_T	–1.0 to +7.0	V	1
Power dissipation	P_T	1.0	W	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	–55 to +125	°C	
Storage temperature under bias	Tbias	–10 to +85	°C	

Note: 1. With respect to V_{SS}

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
	V_{SS}	0	0	0	V	
Input voltage	V_{IH}	2.4	—	6.0	V	
	V_{IL}	–1.0	—	0.8	V	1

Note: 1. V_{IL} min = –3.0 V for pulse width 30 ns

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10 %, V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Notes
Operating power supply current	I_{CC1}	—	—	75	mA	$I_{I/O}$ = 0 mA t_{cyc} = min	
Standby power supply current	I_{SB1}	—	1	2	mA	$\overline{CE}$ = V_{IH} , Vin ≥ 0 V $\overline{OE}/\overline{RFSH}$ = V_{IH}	
	I_{SB2}	—	20	200	µA	$\overline{CE}$ ≥ V_{CC} – 0.2 V, Vin ≥ 0 V, $\overline{OE}/\overline{RFSH}$ ≥ V_{CC} – 0.2 V	1
				100	µA	$\overline{CE}$ ≥ V_{CC} – 0.2 V, Vin ≥ 0 V, $\overline{OE}/\overline{RFSH}$ ≥ V_{CC} – 0.2 V	2
Operating power supply current in self refresh mode	I_{CC2}	—	1	2	mA	$\overline{CE}$ = V_{IH} , Vin ≥ 0 V, $\overline{OE}/\overline{RFSH}$ = V_{IL}	
	I_{CC3}	—	70	200	µA	$\overline{CE}$ ≥ V_{CC} – 0.2 V, Vin ≥ 0 V, $\overline{OE}/\overline{RFSH}$ ≤ 0.2 V	1
			40	100	µA	$\overline{CE}$ ≥ V_{CC} – 0.2 V, Vin ≥ 0 V, $\overline{OE}/\overline{RFSH}$ ≤ 0.2 V	2
Input leakage current	I_{LI}	–10	—	10	µA	V_{CC} = 5.5 V, Vin = V_{SS} to V_{CC}	
Output leakage current	I_{LO}	–10	—	10	µA	$\overline{OE}/\overline{RFSH}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}	
Output voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA	
	V_{OH}	2.4	—	—	V	I_{OH} = –1 mA	

Notes: 1. Only for L-version.
2. Only for V-version.

Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit	Test conditions
Input capacitance	C_{in}	—	8	pF	V_{in} = 0 V
Input /output capacitance	$C_{I/O}$	—	10	pF	$V_{I/O}$ = 0 V

Note : This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

Test Conditions

- Input pulse levels: 0.4 V, 2.4 V
- Input rise and fall time: 5 ns
- Timing measurement level: 0.8 V, 2.2 V
- Reference levels: V_{OH} = 2.0 V, V_{OL} = 0.8 V
- Output load: 1 TTL Gate and C_L (100 pF) (Including scope and jig)

		HM658512A							
		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Random read or write cycle time	t_{RC}	115	—	130	—	160	—	ns	
Chip enable access time	t_{CEA}	—	70	—	80	—	100	ns	
Read-modify- write cycle time	t_{RWC}	160	—	180	—	220	—	ns	
Output enable access time	t_{OEA}	—	25	—	30	—	40	ns	
Chip disable to output in high-Z	t_{CHZ}	0	25	0	25	0	25	ns	1, 2
Chip enable to output in low-Z	t_{CLZ}	20	—	20	—	20	—	ns	2
Output disable to output in high-Z	t_{OHZ}	—	25	—	25	—	25	ns	1, 2
Output enable to output in low-Z	t_{OLZ}	0	—	0	—	0	—	ns	2
Chip enable pulse width	t_{CE}	70 n	10 µ	80 n	10 µ	100 n	10 µ	s	
Chip enable precharge time	t_P	35	—	40	—	50	—	ns	
Address setup time	t_{AS}	0	—	0	—	0	—	ns	
Address hold time	t_{AH}	20	—	20	—	25	—	ns	
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	0	—	ns	
Write command pulse width	t_{WP}	25	—	25	—	30	—	ns	
Chip enable to end of write	t_{CW}	70	—	80	—	100	—	ns	
Chip enable to output enable delay time	t_{OCD}	0	—	0	—	0	—	ns	
Output enable hold time	t_{OHC}	0	—	0	—	0	—	ns	

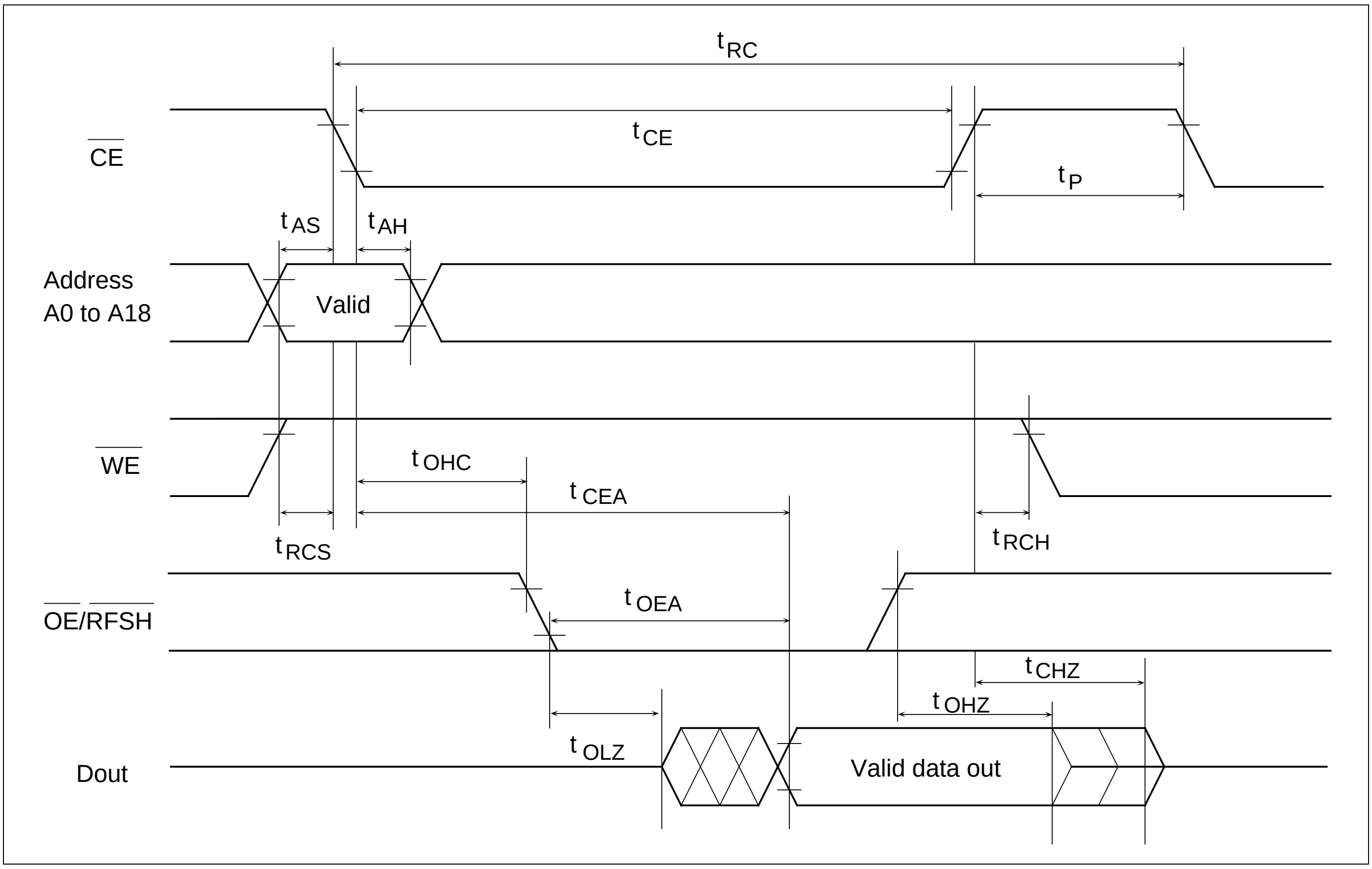
AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.) (cont.)

		HM658512A							
		-7		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Data in to end of write	t_{DW}	20	—	20	—	25	—	ns	
Data in hold time for write	t_{DH}	0	—	0	—	0	—	ns	
Output active from end of write	t_{OW}	5	—	5	—	5	—	ns	2
Write to output in high-Z	t_{WHZ}	—	20	—	20	—	25	ns	1, 2
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	6
Refresh command delay time	t_{RFD}	35	—	40	—	50	—	ns	
Refresh precharge time	t_{FP}	35	—	40	—	40	—	ns	
Refresh command pulse width for automatic refresh	t_{FAP}	70 n	8 µ	80 n	8 µ	80 n	8 µ	s	
Automatic refresh cycle time	t_{FC}	115	—	130	—	160	—	ns	
Refresh command pulse width for self refresh	t_{FAS}	8	—	8	—	8	—	µs	
Refresh reset time from self refresh	t_{RFS}	600	—	600	—	600	—	ns	9
Refresh period	t_{REF}	—	32	—	32	—	32	ms	2048 cycle

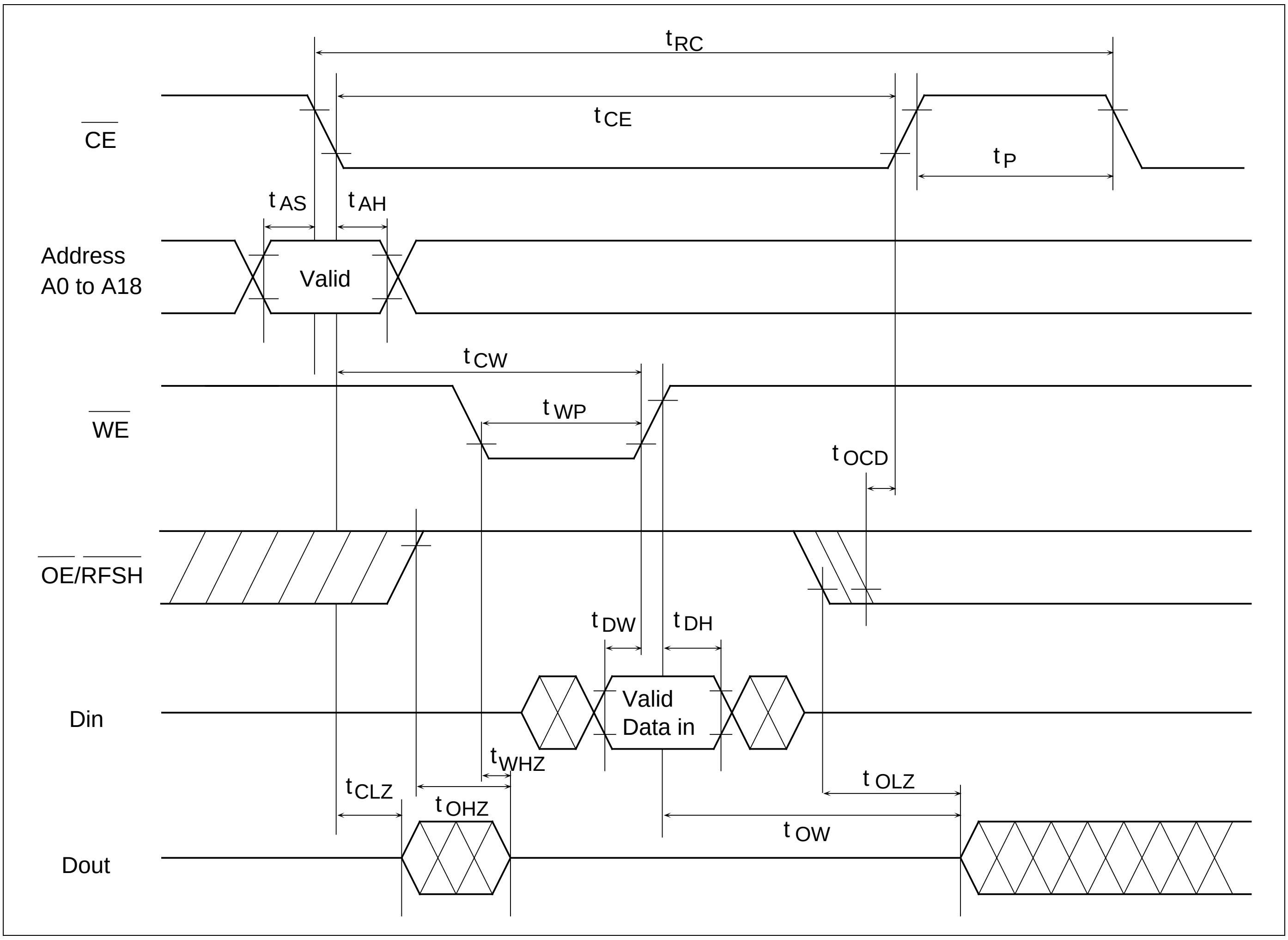
Notes: 1. t_{CHZ}, t_{OHZ}, t_{WHZ} are defined as the time at which the output achieves the open circuit condition.
2. t_{CHZ}, t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{WHZ} and t_{OW} are sampled under the condition of t_T = 5 ns and not 100% tested.
3. A write occurs during the overlap of low $\overline{CE}$ and low $\overline{WE}$. Write end is defined at the earlier of $\overline{WE}$ going high or $\overline{CE}$ going high.
4. If the $\overline{CE}$ low transition occurs simultaneously with or from the $\overline{WE}$ low transition, the output buffers remain in high impedance state.
5. In write cycle, $\overline{OE}$ or $\overline{WE}$ must disable output buffers prior to applying data to the device and at the end of write cycle data inputs must be floated prior to $\overline{OE}$ or $\overline{WE}$ turning on output buffers. During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
6. Transition time t_T is measured between V_{IH} (min) and V_{IL} (max). V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
7. After power-up, pause for more than 100 µs and execute at least 8 initialization cycles.
8. 2048 cycles of burst refresh or the first cycle of distributed automatic refresh must be executed within 15 µs after self refresh, in order to meet the refresh specification of 32 ms and 2048 cycles.
9. At the end of self refresh, refresh reset time (t_{RFS}) is required to reset the internal self refresh operation of the RAM. During t_{RFS}, $\overline{CE}$ and $\overline{OE}/\overline{RFSH}$ must be kept high. If automatic refresh follows self refresh, low transition of $\overline{OE}/\overline{RFSH}$ at the beginning of automatic refresh must not occur during t_{RFS} period.

Timing Waveform

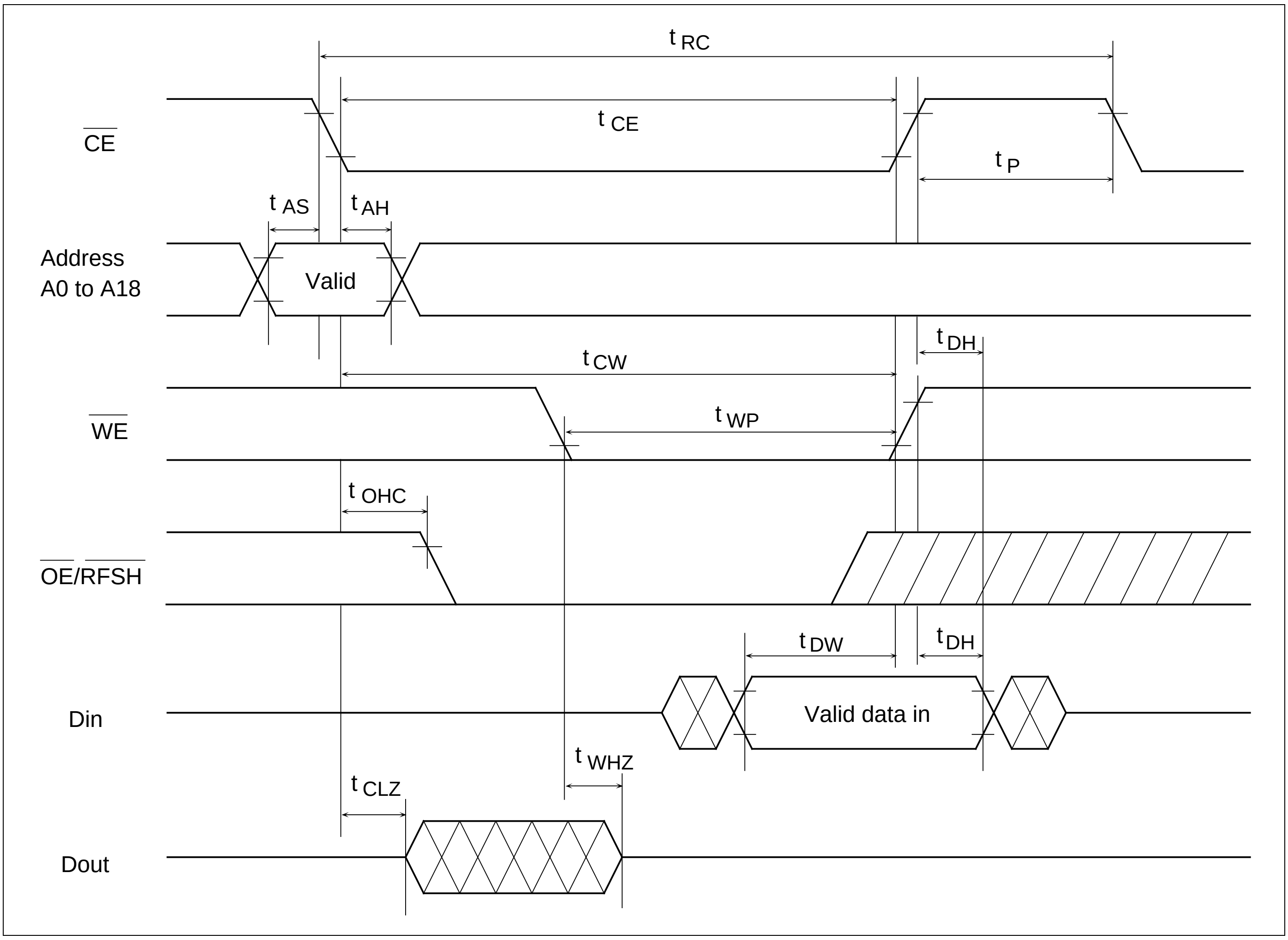
Read Cycle



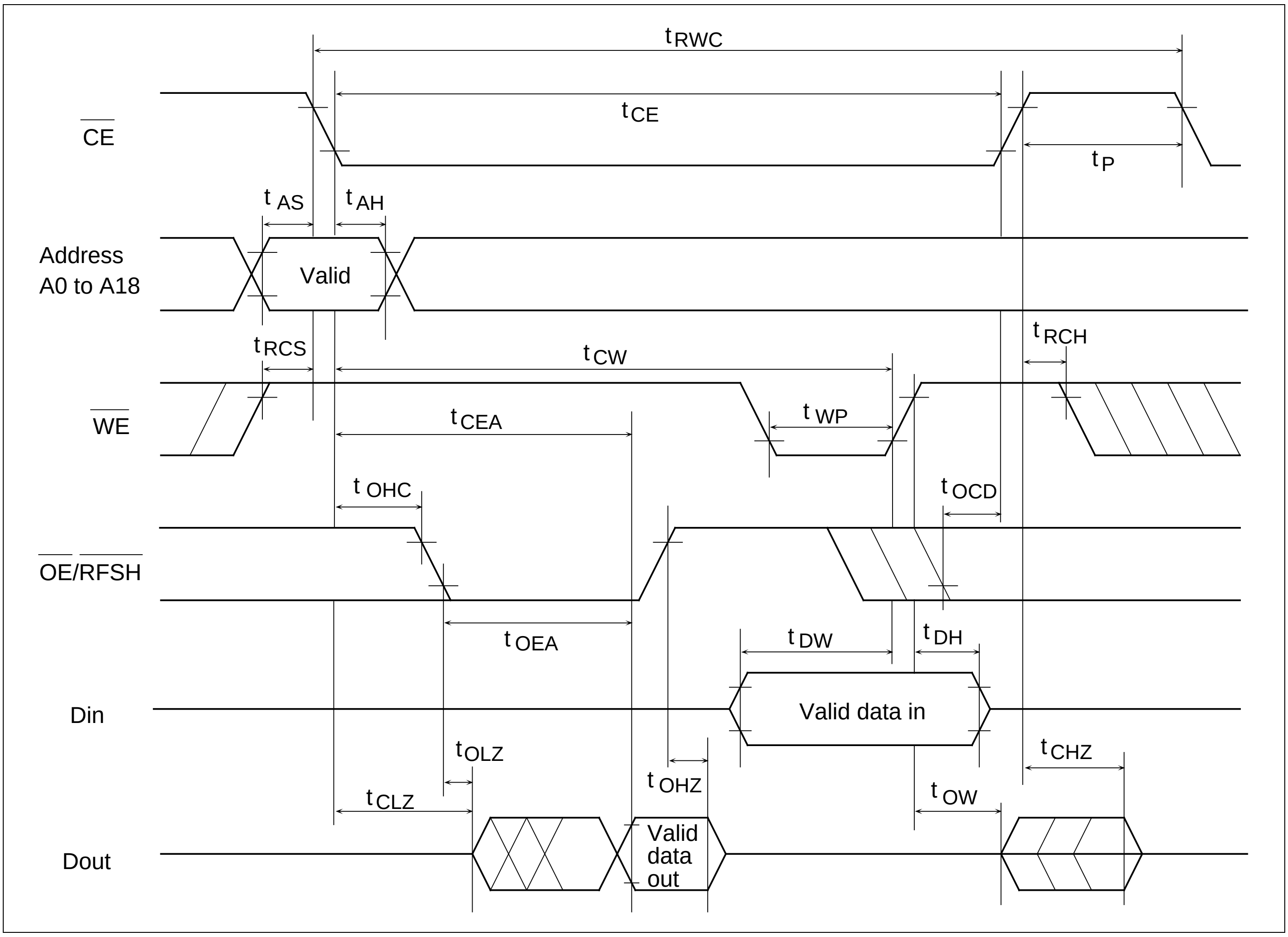
Write Cycle (1) ($\overline{OE}$ high)



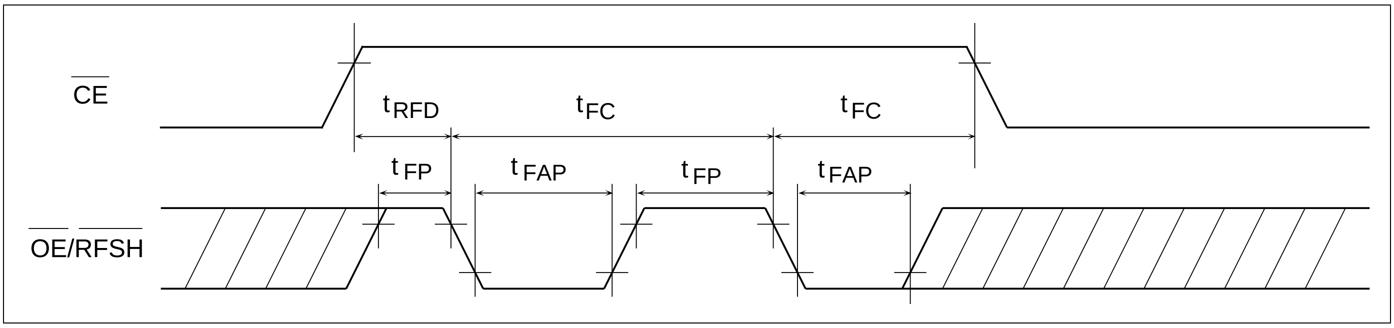
Write Cycle (2) ($\overline{OE}$ low)



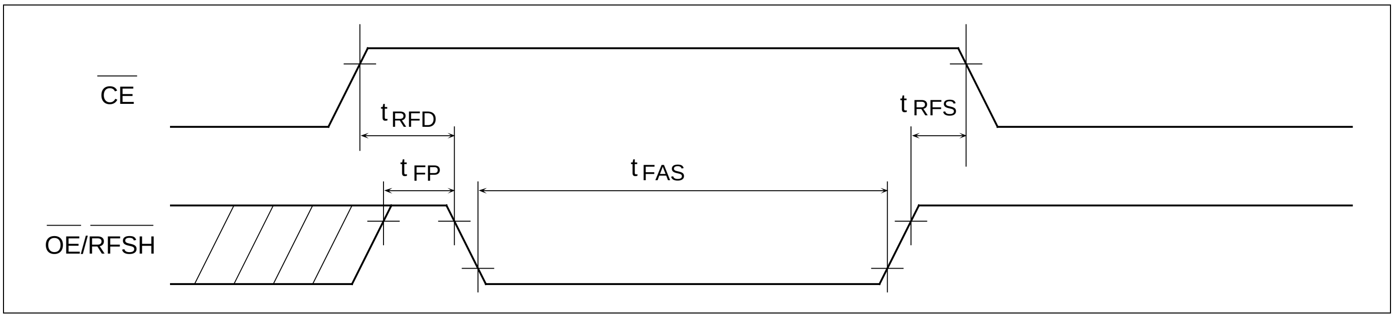
Read-Modify-Write Cycle



Automatic Refresh Cycle



Self Refresh Cycle

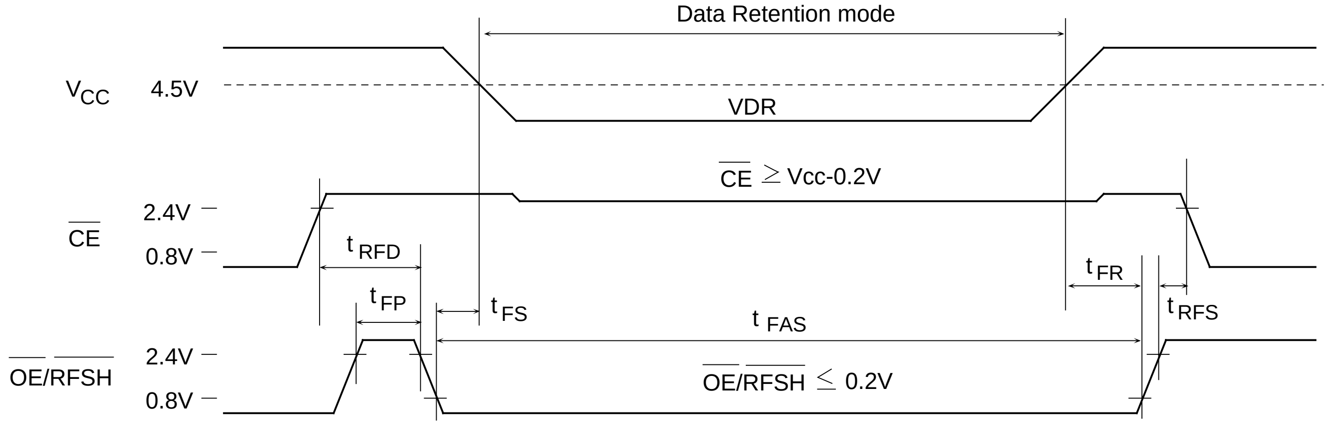


Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

This characteristics is guaranteed only for V-version.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
V_{CC} for data retention	V_{DR}	3.0	—	5.5	V	
Self refresh current	I_{CCDR}	—	—	50	µA	V_{CC} = 3.0 V, $\overline{CE} \geq V_{CC} - 0.2$ V $\overline{OE}/\overline{RFSH} \leq 0.2$ Vin ≥ 0 V
		—	—	100	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC} - 0.2$ V $\overline{OE}/\overline{RFSH} \leq 0.2$ Vin ≥ 0 V
Refresh setup time	t_{FS}	0	—	—	ns	
Operation recovery time	t_{FR}	5	—	—	ms	

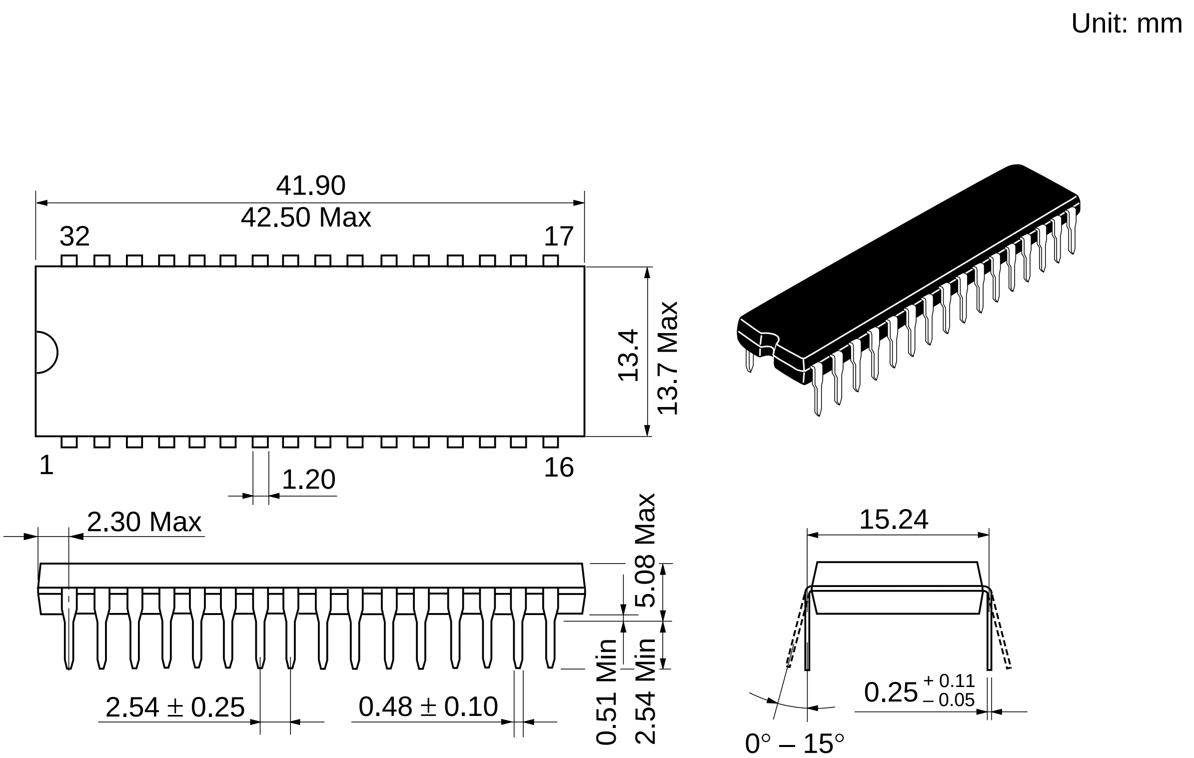
Low V_{CC} Data Retention Timing Waveform



Notes:
1. Rise time and fall time of power supply voltage must be smaller than 0.05 V/ms.
2. Keep $\overline{CE} \geq V_{CC} - 0.2$ V during data retention mode.
3. Regarding t_{RFD}, t_{FP}, t_{FAS} and t_{RFS}, refer to AC characteristics.
4. Input voltage should be lower than V_{CC} +1.5 V in data retention mode.

Package Dimensions

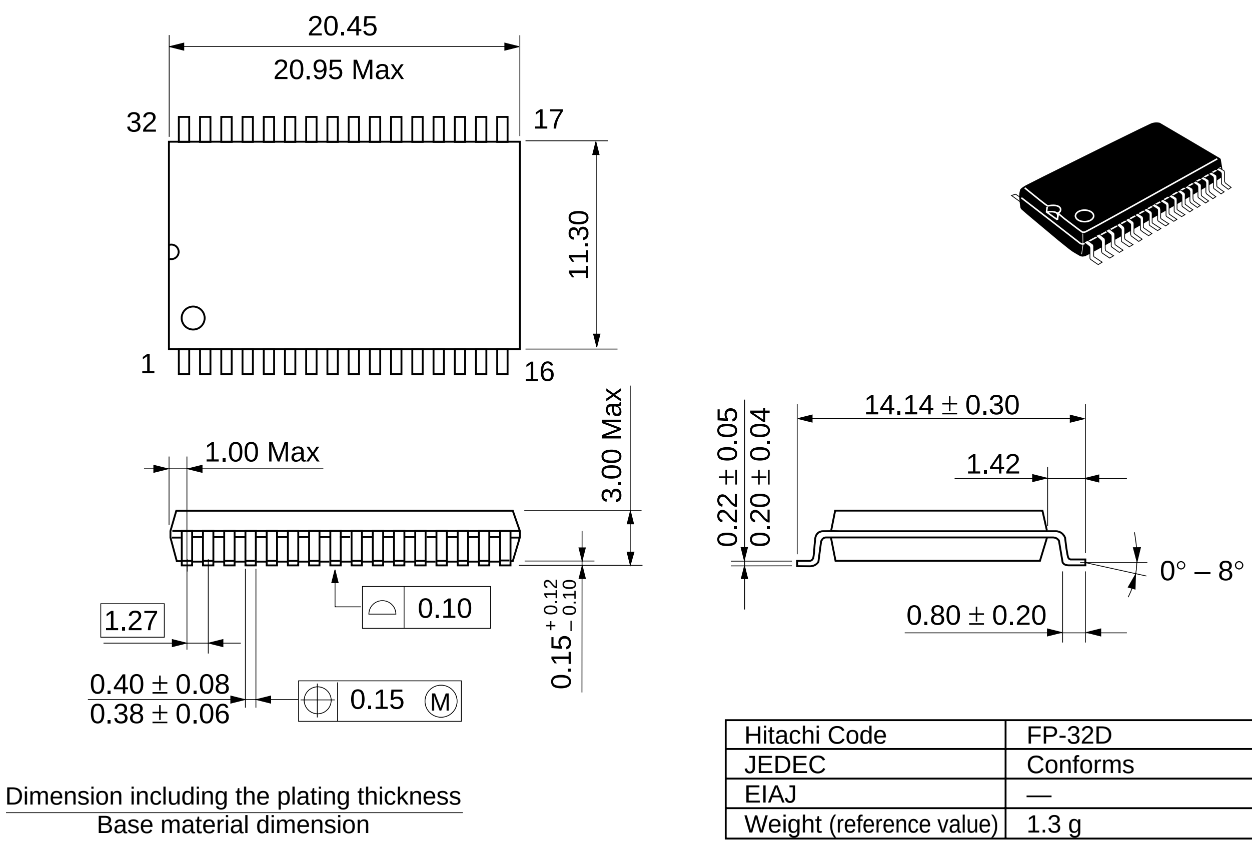
HM658512ALP Series (DP-32)



Hitachi Code	DP-32
JEDEC	—
EIAJ	Conforms
Weight (reference value)	5.1 g

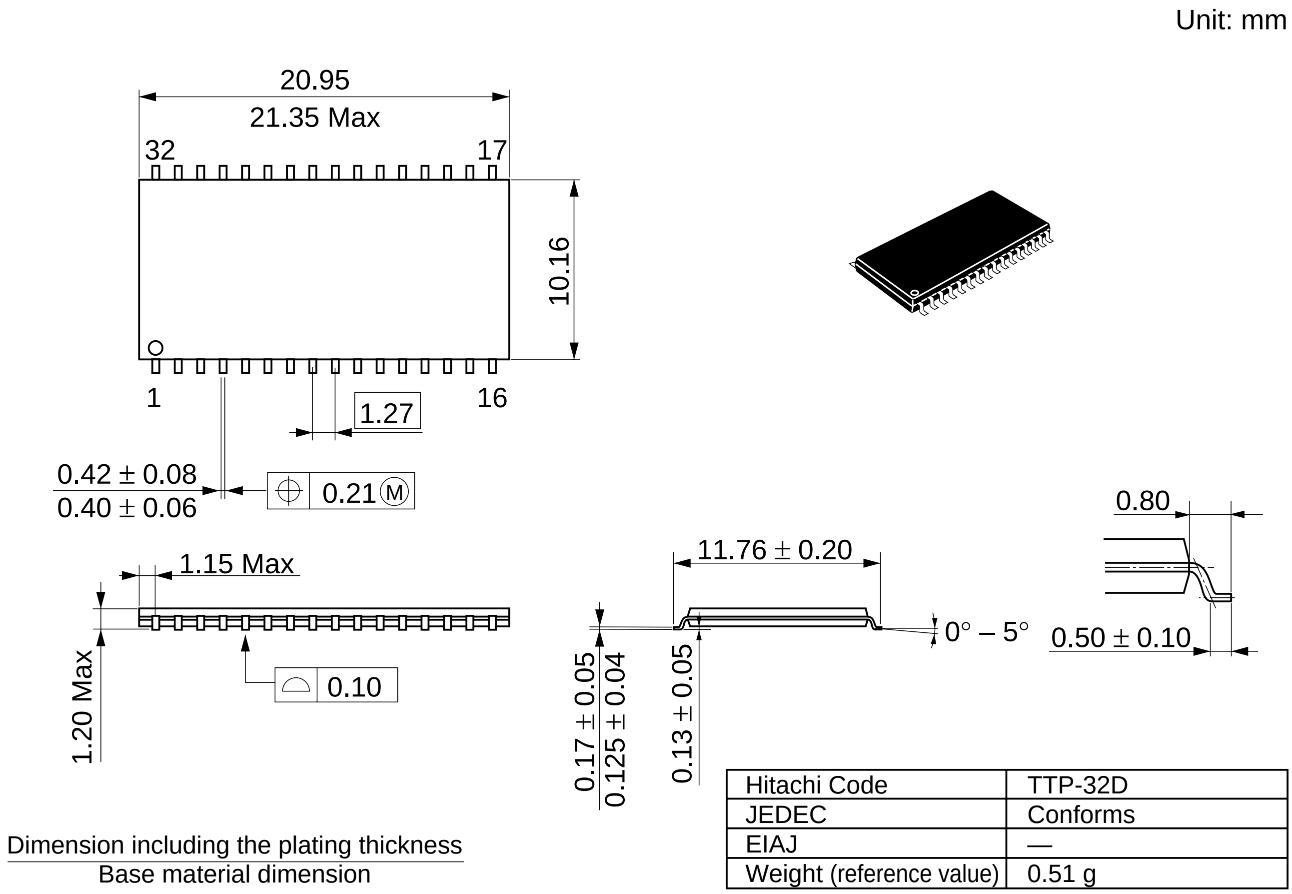
HM658512ALFP Series (FP-32D)

Unit: mm



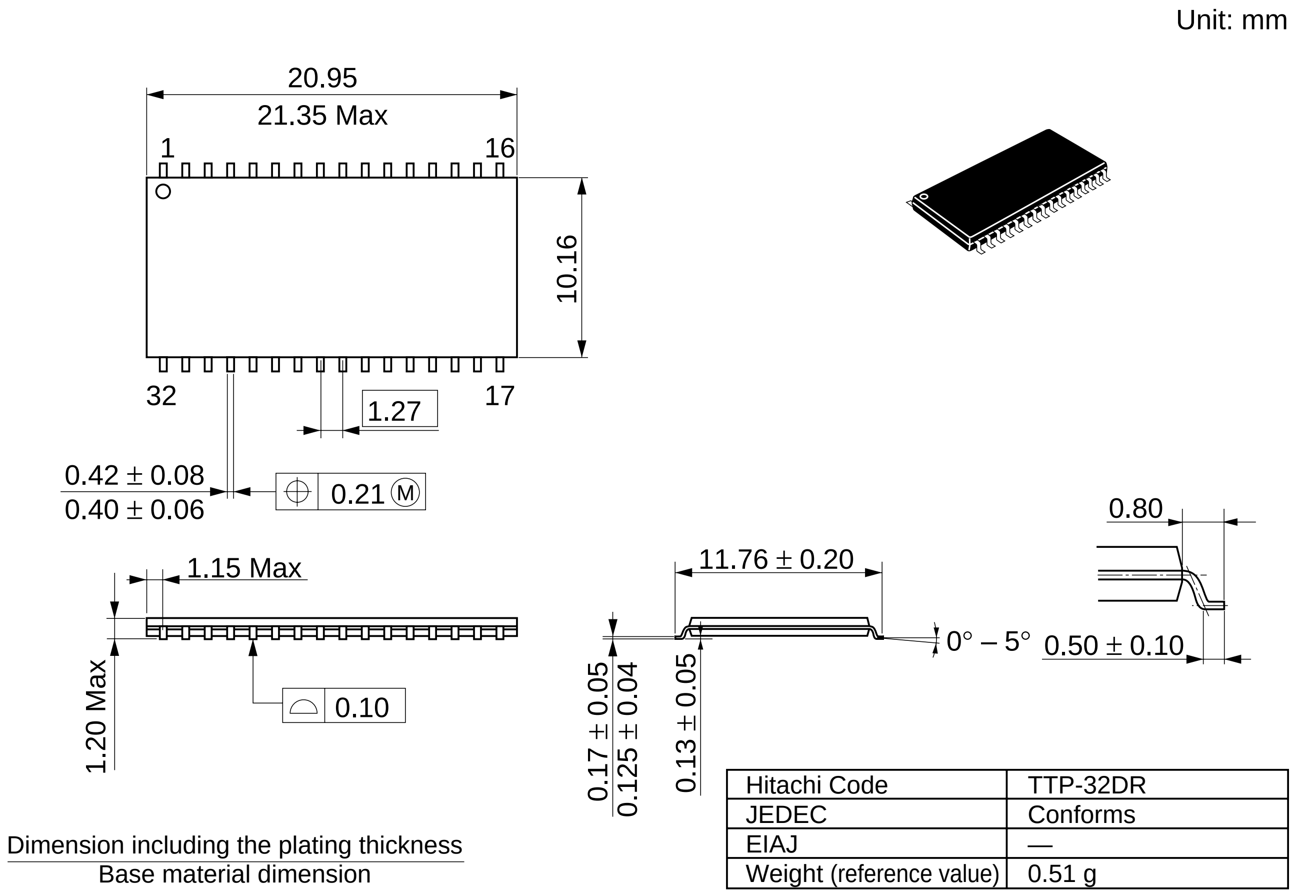
Hitachi Code	FP-32D
JEDEC	Conforms
EIAJ	—
Weight (reference value)	1.3 g

HM658512ALTT Series (TTP-32D)



Hitachi Code	TTP-32D
JEDEC	Conforms
EIAJ	—
Weight (reference value)	0.51 g

HM658512ALRR Series (TTP-32DR)



Hitachi Code	TTP-32DR
JEDEC	Conforms
EIAJ	—
Weight (reference value)	0.51 g

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