64k SRAM (8-kword × 8-bit) Wide Temperature Range version

HITACHI

ADE-203-492C (Z) Rev. 3.0 May. 8, 2000

Description

The Hitachi HM6264BI is 64k-bit static RAM organized 8-kword \times 8-bit. It realizes higher performance and low power consumption by 1.5 μ m CMOS process technology. The device, packaged in 450 mil SOP (foot print pitch width), 600 mil plastic DIP, is available for high density mounting.

Features

Single 5 V supply: 5 V ± 10%
Access time: 100/120 ns (max)

• Power dissipation:

— Standby: $10 \mu W (typ)$

— Operation: 15 mW (typ) (f = 1 MHz)

• Completely static memory

- No clock or timing strobe required

• Equal access and cycle times

• Common data input and output

— Three state output

• Directly TTL compatible

— All inputs and outputs

Battery backup operation capability

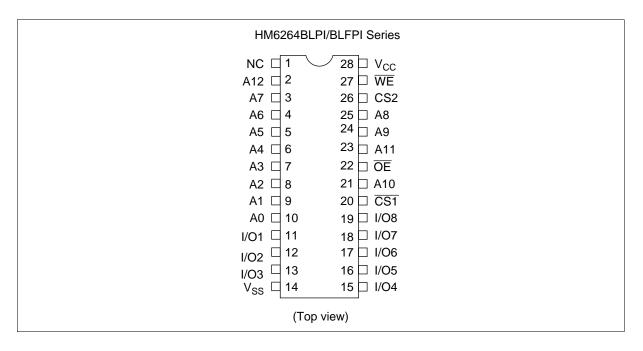
• Operating temperature range: -40°C to +85°C



Ordering Information

| Type No. | Access time | Package |
|------------------------------------|------------------|--------------------------------------|
| HM6264BLPI-10 HM6264BLPI-12 | 100 ns 120 ns | 600-mil, 28-pin plastic DIP (DP-28) |
| HM6264BLFPI-10T HM6264BLFPI-12T | 100 ns 120 ns | 450-mil, 28-pin plastic SOP(FP-28DA) |

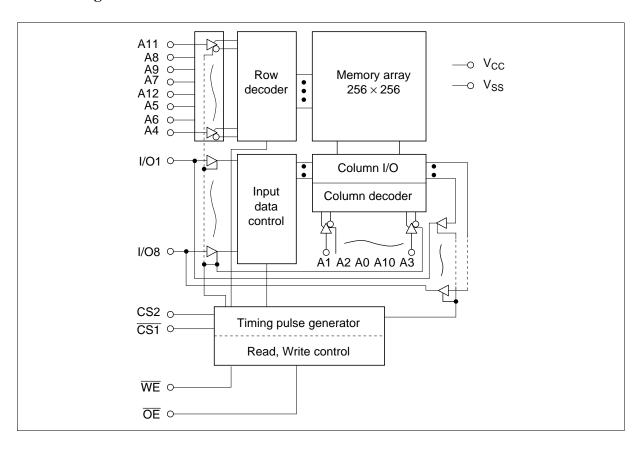
Pin Arrangement



Pin Description

| Pin name | Function |
|-----------------|-------------------|
| A0 to A12 | Address input |
| I/O1 to I/O8 | Data input/output |
| CS1 | Chip select 1 |
| CS2 | Chip select 2 |
| WE | Write enable |
| ŌĒ | Output enable |
| NC | No connection |
| V _{cc} | Power supply |
| V _{SS} | Ground |

Block Diagram



Function Table

| WE | CS1 | CS2 | OE | Mode | V _{cc} current | I/O pin | Ref. cycle |
|----|-----|-----|----|---------------------------|--------------------------|---------|--------------------|
| × | Н | × | × | Not selected (power down) | I_{SB}, I_{SB1} | High-Z | _ |
| × | × | L | × | Not selected (power down) | $I_{\rm SB},I_{\rm SB1}$ | High-Z | _ |
| Н | L | Н | Н | Output disable | I _{cc} | High-Z | _ |
| Н | L | Н | L | Read | I _{cc} | Dout | Read cycle (1)–(3) |
| L | L | Н | Н | Write | I _{cc} | Din | Write cycle (1) |
| L | L | Н | L | Write | I _{cc} | Din | Write cycle (2) |

Note: x: H or L

Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|--------------------------------|-----------------|---|------|
| Power supply voltage*1 | V _{cc} | -0.5 to +7.0 | V |
| Terminal voltage*1 | V _T | -0.5^{*2} to V _{CC} + 0.3^{*3} | 3 V |
| Power dissipation | P _T | 1.0 | W |
| Operating temperature | Topr | -40 to +85 | °C |
| Storage temperature | Tstg | -55 to +125 | °C |
| Storage temperature under bias | Tbias | -40 to +85 | °C |

Notes: 1. Relative to V_{ss}

2. V_T min: -3.0 V for pulse half-width ≤ 50 ns

3. Maximum voltage is 7.0 V

Recommended DC Operating Conditions ($Ta = -40 \text{ to } +85^{\circ}\text{C}$)

| Parameter | Symbol | Min | Тур | Max | Unit |
|--------------------|-----------------|--------|-----|-----------------------|------|
| Supply voltage | V _{cc} | 4.5 | 5.0 | 5.5 | V |
| | V _{ss} | 0 | 0 | 0 | V |
| Input high voltage | V _{IH} | 2.4 | _ | V _{cc} + 0.3 | V |
| Input low voltage | V _{IL} | -0.3*1 | _ | 0.6 | V |

Note: 1. V_{IL} min: -3.0 V for pulse half-width ≤ 50 ns

DC Characteristics (Ta = -40 to $+85^{\circ}$ C, $V_{CC} = 5$ V $\pm 10\%$, $V_{SS} = 0$ V)

| Parameter | Symbol | Min | Typ*1 | Max | Unit | Test conditions |
|--|-------------------|-----|-------|-----|------|---|
| Input leakage current | I _{LI} | _ | _ | 2 | μΑ | $Vin = V_{SS} to V_{CC}$ |
| Output leakage current | I _{LO} | _ | _ | 2 | μΑ | $\overline{\text{CS1}} = \text{V}_{\text{IH}} \text{ or CS2} = \text{V}_{\text{IL}} \text{ or } \overline{\text{OE}} = \text{V}_{\text{IH}} \text{ or } \overline{\text{WE}} = \text{V}_{\text{IL}}, \text{ V}_{\text{I/O}} = \text{V}_{\text{SS}} \text{ to V}_{\text{CC}}$ |
| Operating power supply current | I _{CCDC} | _ | 7 | 20 | mA | $\overline{\text{CS1}} = \text{V}_{\text{IL}}, \text{CS2} = \text{V}_{\text{IH}}, \text{I}_{\text{I/O}} = 0 \text{ mA}$ others = $\text{V}_{\text{IH}}/\text{V}_{\text{IL}}$ |
| Average operating power supply current | I _{CC1} | _ | 30 | 50 | mA | $\frac{\text{Min cycle, duty} = 100\%,}{\overline{\text{CS1}} = \text{V}_{\text{IL}}, \text{CS2} = \text{V}_{\text{IH}}, \text{I}_{\text{I/O}} = 0 \text{ mA}}{\text{others} = \text{V}_{\text{IH}}/\text{V}_{\text{IL}}}$ |
| | I _{CC2} | _ | 3 | 8 | mA | $\begin{split} & \frac{\text{Cycle time}}{\text{CS1}} = 1 \text{ µs, duty} = 100\%, \ I_{\text{I/O}} = 0 \text{ mA} \\ & \frac{\text{CS1}}{\text{CS}} \leq 0.2 \text{ V, CS2} \geq V_{\text{CC}} - 0.2 \text{ V,} \\ & V_{\text{IH}} \geq V_{\text{CC}} - 0.2 \text{ V, } V_{\text{IL}} \leq 0.2 \text{ V} \end{split}$ |
| Standby power supply current | I _{SB} | _ | 1 | 3 | mA | $\overline{\text{CS1}} = \text{V}_{\text{IH}}, \text{CS2} = \text{V}_{\text{IL}}$ |
| | _{SB1} *2 | _ | 2 | 200 | μΑ | $\label{eq:cstate} \begin{split} \overline{CS1} \ge V_{\text{CC}} - 0.2 \ \text{V}, \ CS2 \ge V_{\text{CC}} - 0.2 \ \text{V} \ \text{or} \\ 0 \ \text{V} \le CS2 \le 0.2 \ \text{V}, \ 0 \ \text{V} \le \text{Vin} \end{split}$ |
| Output low voltage | V_{OL} | _ | _ | 0.4 | V | I _{OL} = 2.1 mA |
| Output high voltage | V _{OH} | 2.4 | _ | _ | V | I _{OH} = -1.0 mA |

Notes: 1. Typical values are at $V_{cc} = 5.0 \text{ V}$, $Ta = +25^{\circ}\text{C}$ and not guaranteed.

2. $V_{IL} \min = -0.3V$

Capacitance (Ta = 25°C, f = 1.0 MHz)

| Parameter | Symbol | Min | Тур | Max | Unit | Test conditions |
|----------------------------|------------------|-----|-----|-----|------|-----------------|
| Input capacitance*1 | Cin | _ | _ | 5 | pF | Vin = 0 V |
| Input/output capacitance*1 | C _{I/O} | _ | _ | 7 | pF | $V_{I/O} = 0 V$ |

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = -40 to +85°C, $V_{CC} = 5$ V ± 10 %, unless otherwise noted.)

Test Conditions

• Input pulse levels: 0.6 V to 2.4 V

• Input and output timing reference level: 1.5 V

• Input rise and fall time: 10 ns

• Output load: 1 TTL Gate + C_L (100 pF) (Including scope & jig)

Read Cycle

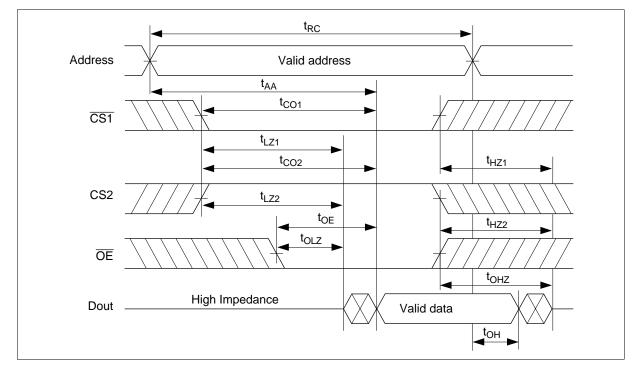
| | | | HM6264BI-10 | | HM6264BI-12 | | | |
|---|-----|------------------|-------------|-----|-------------|-----|------|-------|
| Parameter | | Symbol | Min | Max | Min | Max | Unit | Notes |
| Read cycle time | | t _{RC} | 100 | _ | 120 | _ | ns | |
| Address access time | | t _{AA} | _ | 100 | _ | 120 | ns | |
| Chip select access time | CS1 | t _{co1} | _ | 100 | _ | 120 | ns | |
| | CS2 | t _{CO2} | _ | 100 | _ | 120 | ns | |
| Output enable to output valid | | t _{oe} | _ | 50 | _ | 60 | ns | |
| Chip selection to output in low-Z | CS1 | t _{LZ1} | 10 | _ | 10 | _ | ns | 2 |
| | CS2 | t _{LZ2} | 10 | _ | 10 | _ | ns | 2 |
| Output enable to output in low-Z | | t _{oLZ} | 5 | _ | 5 | _ | ns | 2 |
| Chip deselection in to output in high-Z | CS1 | t _{HZ1} | 0 | 35 | 0 | 40 | ns | 1, 2 |
| | CS2 | t _{HZ2} | 0 | 35 | 0 | 40 | ns | 1, 2 |
| Output disable to output in high-Z | | t _{OHZ} | 0 | 35 | 0 | 40 | ns | 1, 2 |
| Output hold from address change | | t _{oh} | 10 | _ | 10 | _ | ns | |

Notes: 1. t_{HZ} is defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.

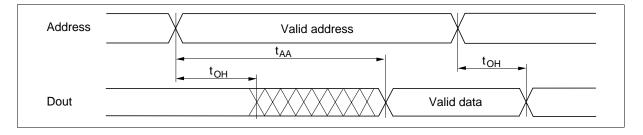
^{2.} At any given temperature and voltage condition, t_{HZ} maximum is less than t_{LZ} minimum both for a given device and from device to device.

^{3.} Address must be valid prior to or simultaneously with $\overline{\text{CS1}}$ going low or CS2 going high.

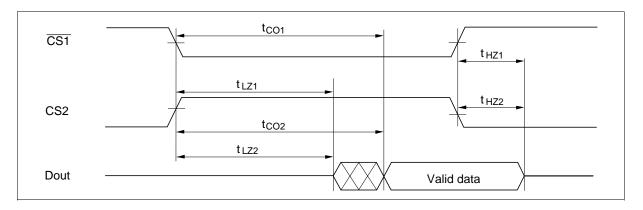
Read Timing Waveform (1) $(\overline{WE} = V_{IH})$



Read Timing Waveform (2) $(\overline{WE}=V_{IH},\,\overline{OE}=V_{IL})$



Read Timing Waveform (3) $(\overline{WE}=V_{IH},\,\overline{OE}=V_{IL})^{*3}$



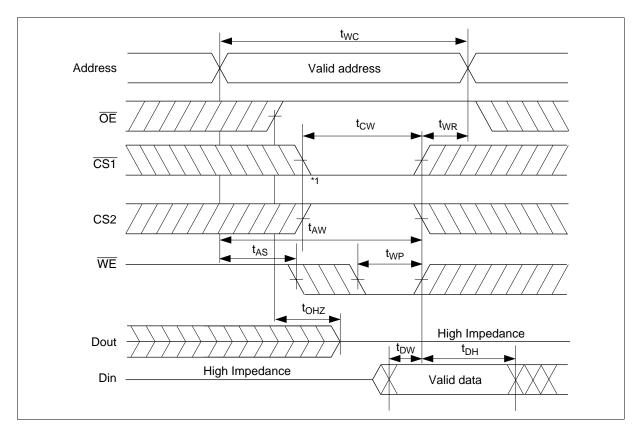
Write Cycle

| Parameter | Symbol | Min | Max | Min | Max | Unit | Notes |
|------------------------------------|------------------|-----|-----|-----|-----|------|-------|
| Write cycle time | t _{wc} | 100 | _ | 120 | _ | ns | |
| Chip selection to end of write | t _{cw} | 80 | _ | 85 | _ | ns | 2 |
| Address setup time | t _{AS} | 0 | _ | 0 | _ | ns | 3 |
| Address valid to end of write | t _{AW} | 80 | _ | 85 | _ | ns | |
| Write pulse width | t _{wP} | 60 | _ | 70 | _ | ns | 1, 9 |
| Write recovery time | t _{wr} | 0 | _ | 0 | _ | ns | 4 |
| WE to output in high-Z | t _{whz} | 0 | 35 | 0 | 40 | ns | 5 |
| Data to write time overlap | t _{DW} | 40 | _ | 40 | _ | ns | |
| Data hold from write time | t _{DH} | 0 | _ | 0 | _ | ns | |
| Output active from end of write | t _{ow} | 5 | _ | 5 | _ | ns | |
| Output disable to output in high-Z | t _{OHZ} | 0 | 35 | 0 | 40 | ns | 5 |

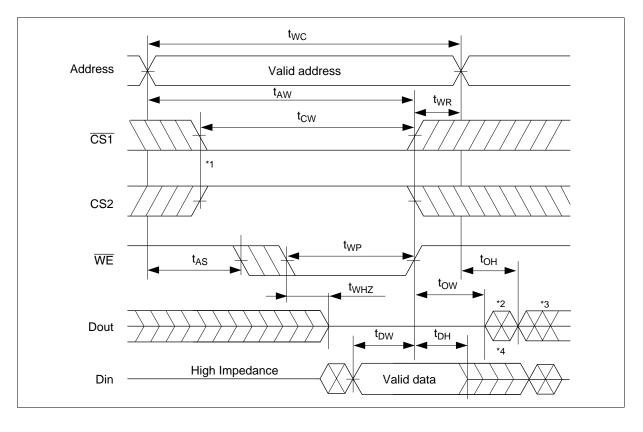
- Notes: 1. A write occurs during the overlap of a low $\overline{CS1}$, and high CS2, and a high \overline{WE} . A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and \overline{WE} going low. A write ends at the earliest transition among $\overline{CS1}$ going high CS2 going low and \overline{WE} going high. Time t_{WP} is measured from the beginning of write to the end of write.
 - 2. t_{cw} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
 - 3. t_{AS} is measured from the address valid to the beginning of write.
 - 4. t_{wR} is measured from the earliest of $\overline{\text{CS1}}$ or $\overline{\text{WE}}$ going high or CS2 going low to the end of write cycle.
 - 5. During this period, I/O pins are in the output state, therefore the input signals of the opposite phase to the outputs must not be applied.
 - 6. If CS1 goes low simultaneously with WE going low after WE goes low, the outputs remain in high impedance state.
 - 7. Dout is the same phase of the written data in this write cycle.
 - 8. Dout is the read data of the next address
 - 9. In the write cycle with $\overline{\text{OE}}$ low fixed, t_{WP} must satisfy the following equation to avoid a problem of data bus contention

 $t_{WP} \ge t_{WHZ} \max + t_{DW} \min$.

Write Timing Waveform (1) $(\overline{OE} \ Clock)$



Write Timing Waveform (2) (\overline{OE} Low Fixed) (\overline{OE} = V_{IL})



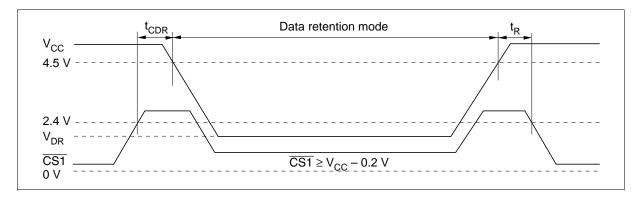
Low V_{CC} **Data Retention Characteristics** (Ta = -40 to +85°C)

| Parameter | Symbol | Min | Typ*1 | Max | Unit | Test conditions*3 |
|--------------------------------------|-------------------|-----|-------------------------|-------|------|---|
| V _{cc} for data retention | V_{DR} | 2.0 | _ | _ | V | $\label{eq:cstart} \begin{split} \overline{CS1} &\geq V_{\rm CC} - 0.2 \text{ V}, \\ CS2 &\geq V_{\rm CC} - 0.2 \text{ V or } CS2 \leq 0.2 \text{ V} \\ \text{Vin} &\geq 0 \text{ V} \end{split}$ |
| Data retention current | I _{CCDR} | _ | 1 * ¹ | 100*2 | μΑ | $\begin{tabular}{ll} $V_{CC} = 3.0 \text{ V}, 0 \text{ V} \leq \text{Vin} \leq \text{V}_{CC} \\ \hline $CS1 \geq \text{V}_{CC}$ -0.2 \text{ V}, $CS2 \geq \text{V}_{CC}$ -0.2 \text{ V} \\ $\text{or } 0 \text{ V} \leq \text{CS2} \leq 0.2 \text{ V} \\ \end{tabular}$ |
| Chip deselect to data retention time | t _{CDR} | 0 | _ | _ | ns | See retention waveform |
| Operation recovery time | t _R | 5 | _ | _ | ms | _ |

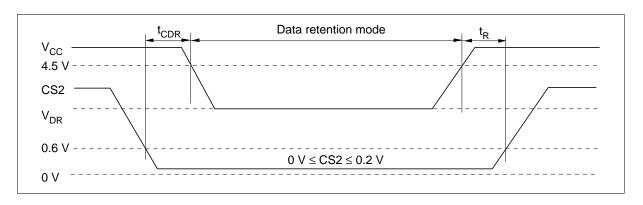
Notes: 1. Reference data at Ta = 25°C.

- 2. $10 \mu A \text{ max at Ta} = -40 \text{ to} + 40^{\circ} \text{C}.$
- 3. CS2 controls address buffer, \overline{WE} buffer, $\overline{CS1}$ buffer, \overline{OE} buffer, and Din buffer. If CS2 controls data retention mode, Vin levels (address, \overline{WE} , \overline{OE} , $\overline{CS1}$, I/O) can be in the high impedance state. If $\overline{CS1}$ controls data retention mode, CS2 must be $CS2 \ge V_{cc} 0.2$ V or 0 V $\le CS2 \le 0.2$ V. The other input levels (address, \overline{WE} , \overline{OE} , I/O) can be in the high impedance state.

$\textbf{Low}~\textbf{V}_{CC}~\textbf{Data}~\textbf{Retention}~\textbf{Timing}~\textbf{Waveform}~\textbf{(1)}~(\overline{CS1}~\textbf{Controlled})$

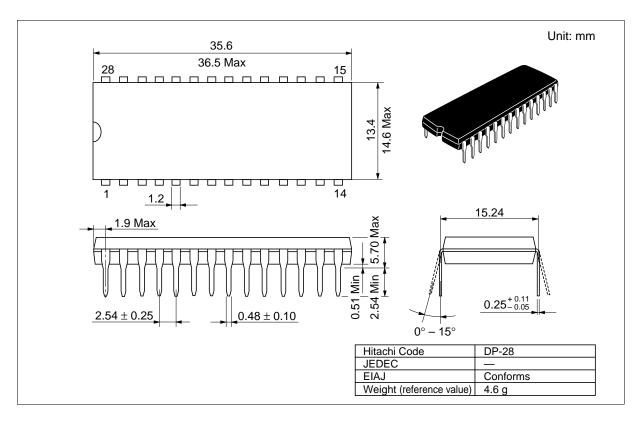


Low V_{CC} Data Retention Timing Waveform (2) (CS2 Controlled)



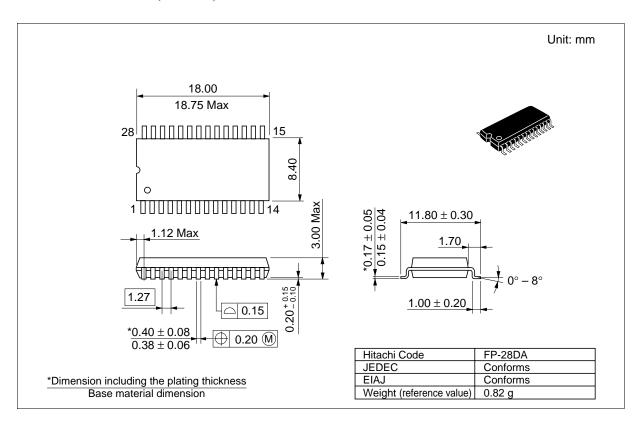
Package Dimensions

HM6264BLPI Series (DP-28)



Package Dimensions (cont.)

HM6264BLFPI Series (FP-28DA)



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Revision Record

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| 1.0 | Sep. 5, 1996 | Deletion of Preliminary | I. Ogiwara | K. Imato |
| 2.0 | Feb. 9, 1998 | Change of subtitle Change of FP-28DA | I. Ogiwara | K. Imato |
| 3.0 | May. 8, 2000 | Low V_{CC} Data Retention Characteristics Note 2: V_{IL} min = -0.3 V to 10 μ A max at Ta = -40 to + 40°C | | |