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# HM514100D Series

4,194,304-word × 1-bit Dynamic RAM

# HITACHI

ADE-203-680A (Z)  
Rev. 1.0  
Nov. 13, 1997

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## Description

The Hitachi HM514100D is a CMOS dynamic RAM organized 4,194,304 word × 1-bit. HM514100D has realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514100D offers Fast Page Mode as a high speed access mode. Multiplexed address input permits the HM514100D to be packaged in standard 300-mil 26-pin plastic SOJ.

## Features

- Single 5 V (±10%)
- Access time : 60 ns/70 ns/80 ns (max)
- Power dissipation
  - Active mode : 605 mW/550 mW/495 mW (max)
  - Standby mode : 11 mW (max)  
0.55 mW (max) (L-version)
- Fast page mode capability
- Refresh cycles
  - 1024 refresh cycles: 16 ms  
: 128 ms (L-version)
- 3 variations of refresh
  - $\overline{\text{RAS}}$ -only refresh
  - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh
  - Hidden refresh
- Test function
- Battery backup operation (L-version)

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## HM514100D Series

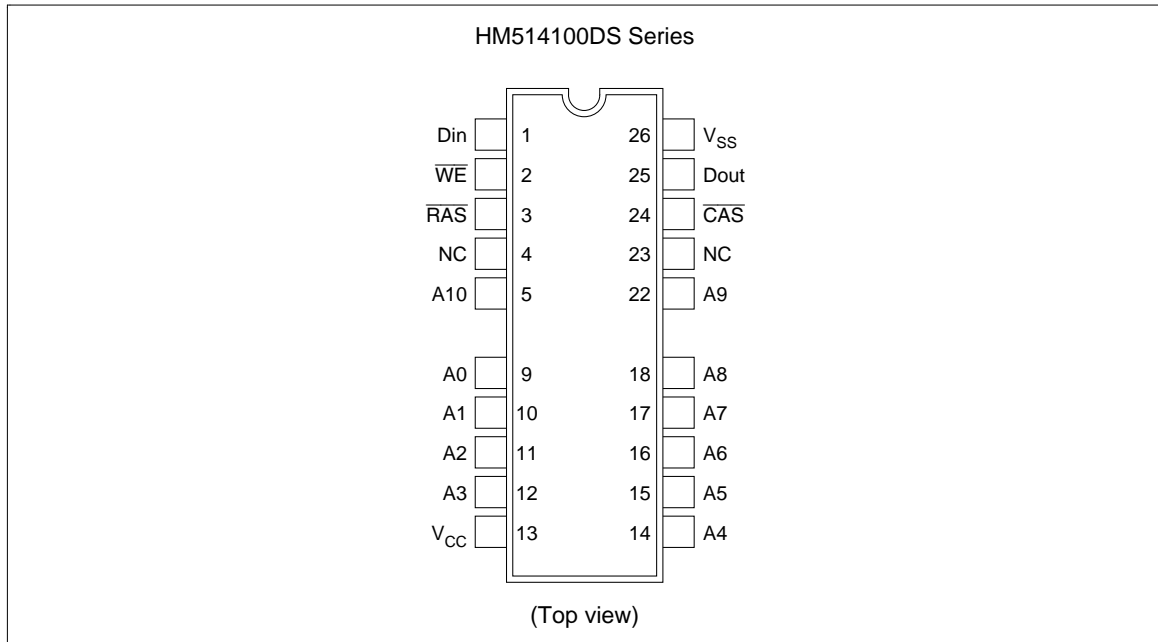
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### Ordering Information

Type No.	Access time	Package
HM514100DS-6	60 ns	300-mil 26-pin plastic SOJ (CP-26/20D)
HM514100DS-7	70 ns	
HM514100DS-8	80 ns	
HM514100DLS-6	60 ns	
HM514100DLS-7	70 ns	
HM514100DLS-8	80 ns	

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### Pin Arrangement

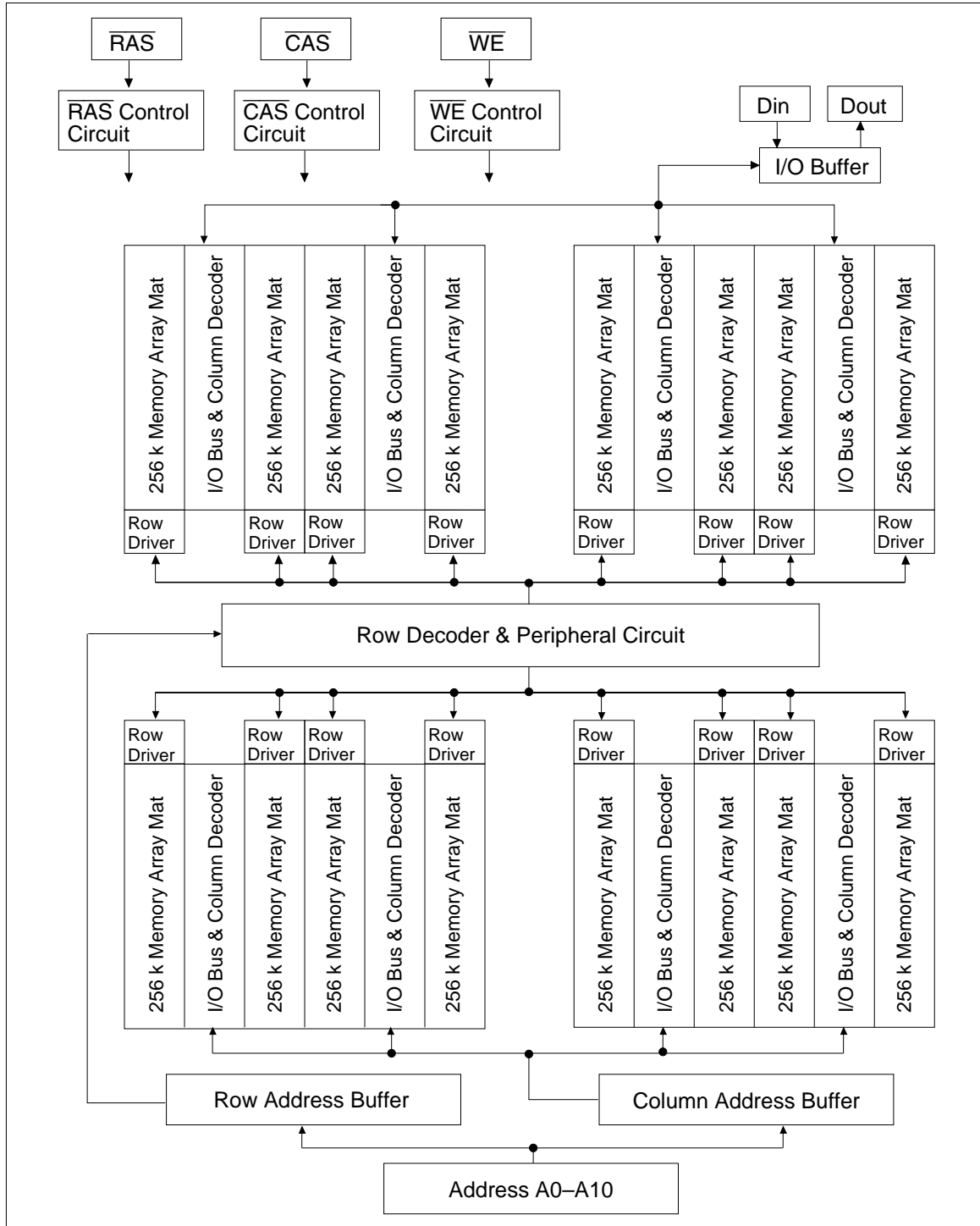


### Pin Description

Pin name	Function
A0 to A10	Address input <ul style="list-style-type: none"> <li>• Row Address A0 to A10</li> <li>• Column Address A0 to A10</li> <li>• Refresh Address A0 to A9</li> </ul>
Din	Data-in
Dout	Data-out
$\overline{\text{RAS}}$	Row address strobe
$\overline{\text{CAS}}$	Column address strobe
$\overline{\text{WE}}$	Read/Write enable
$V_{\text{CC}}$	Power supply
$V_{\text{SS}}$	Ground
NC	No connection

# HM514100D Series

## Block Diagram



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## HM514100D Series

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### Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to $V_{SS}$	$V_T$	-1.0 to +7.0	V
Supply voltage relative to $V_{SS}$	$V_{CC}$	-1.0 to +7.0	V
Short circuit output current	$I_{out}$	50	mA
Power dissipation	$P_T$	1.0	W
Operating temperature	$T_{opr}$	0 to +70	°C
Storage temperature	$T_{stg}$	-55 to +125	°C

### Recommended DC Operating Conditions ( $T_a = 0$ to $+70^\circ\text{C}$ )

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	$V_{SS}$	0	0	0	V	
	$V_{CC}$	4.5	5.0	5.5	V	1
Input high voltage	$V_{IH}$	2.4	—	6.5	V	1
Input low voltage	$V_{IL}$	-1.0	—	0.8	V	1

Note: 1. All voltage referred to  $V_{SS}$ .

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DC Characteristics (Ta = 0 to +70°C, V<sub>CC</sub> = 5 V ± 10%, V<sub>SS</sub> = 0 V)

Parameter	Symbol	HM514100D						Unit	Test conditions	Notes
		-6		-7		-8				
		Min	Max	Min	Max	Min	Max			
Operating current	I <sub>CC1</sub>	—	110	—	100	—	90	mA	$\overline{\text{RAS}}, \overline{\text{CAS}}$ cycling t <sub>RC</sub> = min	1, 2
Standby current	I <sub>CC2</sub>	—	2	—	2	—	2	mA	TTL interface RAS, CAS = V <sub>IH</sub> Dout = High-Z	
		—	1	—	1	—	1	mA	CMOS interface RAS, CAS ≥ V <sub>CC</sub> - 0.2 V Dout = High-Z	
Standby current (L-version)	I <sub>CC2</sub>	—	100	—	100	—	100	μA	CMOS interface $\overline{\text{RAS}}, \overline{\text{CAS}} = V_{IH}$ WE, Address and Din = V <sub>IH</sub> or V <sub>IL</sub> Dout = High-Z	4
$\overline{\text{RAS}}$ -only refresh current	I <sub>CC3</sub>	—	110	—	100	—	90	mA	t <sub>RC</sub> = min	2
Standby current	I <sub>CC5</sub>	—	5	—	5	—	5	mA	$\overline{\text{RAS}} = V_{IH}$ , $\overline{\text{CAS}} = V_{IL}$ Dout = enable	1
$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh current	I <sub>CC6</sub>	—	110	—	100	—	90	mA	t <sub>RC</sub> = min	
Fast page mode current	I <sub>CC7</sub>	—	110	—	100	—	90	mA	t <sub>PC</sub> = min	1, 3
Battery backup current (Standby with CBR refresh) (L-version)	I <sub>CC10</sub>	—	200	—	200	—	200	μA	t <sub>RC</sub> = 125 μs t <sub>RAS</sub> ≤ 1 μs WE = V <sub>IH</sub> , $\overline{\text{CAS}} = V_{IL}$ OE Address, Din = V <sub>IH</sub> or V <sub>IL</sub> Dout = High-Z	4
Input leakage current	I <sub>LI</sub>	-10	10	-10	10	-10	10	μA	0 V ≤ Vin ≤ 7 V	
Output leakage current	I <sub>LO</sub>	-10	10	-10	10	-10	10	μA	0 V ≤ Vout ≤ 7 V Dout = disable	
Output high voltage	V <sub>OH</sub>	2.4	V <sub>CC</sub>	2.4	V <sub>CC</sub>	2.4	V <sub>CC</sub>	V	High Iout = -5 mA	
Output low voltage	V <sub>OL</sub>	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

Notes: 1. I<sub>CC</sub> depends on output load condition when the device is selected. I<sub>CC</sub> max is specified at the output open condition.

2. Address can be changed twice or less while  $\overline{\text{RAS}} = V_{IL}$ .

3. Address can be changed once or less while  $\overline{\text{CAS}} = V_{IH}$ .

4. V<sub>CC</sub> - 0.2 V ≤ V<sub>IH</sub> ≤ 6.5 V and 0 V ≤ V<sub>IL</sub> ≤ 0.2 V.

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### Capacitance (Ta = 25°C, V<sub>CC</sub> = 5 V ± 10%)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address, Data-in)	C <sub>I1</sub>	—	5	pF	1
Input capacitance (Clocks)	C <sub>I2</sub>	—	7	pF	1
Output capacitance (Data-out)	C <sub>O</sub>	—	7	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2.  $\overline{\text{RAS}}, \overline{\text{CAS}} = V_{\text{IH}}$  to disable Dout.

### AC Characteristics (Ta = 0 to +70°C, V<sub>CC</sub> = 5 V ± 10%, V<sub>SS</sub> = 0 V)<sup>\*1, \*12, \*15</sup>

#### Test Conditions

- Input rise and fall time : 5 ns
- Input timing reference levels : 0.8 V, 2.4 V
- Output load : 2 TTL gate + C<sub>L</sub> (100 pF) (Including scope and jig)

#### Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

Parameter	Symbol	HM514100D						Unit	Notes
		-6		-7		-8			
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t <sub>RC</sub>	110	—	130	—	150	—	ns	
$\overline{\text{RAS}}$ precharge time	t <sub>RP</sub>	40	—	50	—	60	—	ns	
$\overline{\text{RAS}}$ pulse width	t <sub>RAS</sub>	60	10000	70	10000	80	10000	ns	18
$\overline{\text{CAS}}$ pulse width	t <sub>CAS</sub>	15	10000	20	10000	20	10000	ns	19
Row address setup time	t <sub>ASR</sub>	0	—	0	—	0	—	ns	
Row address hold time	t <sub>RAH</sub>	10	—	10	—	10	—	ns	
Column address setup time	t <sub>ASC</sub>	0	—	0	—	0	—	ns	
Column address hold time	t <sub>CAH</sub>	15	—	15	—	15	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t <sub>RCD</sub>	20	45	20	50	20	60	ns	8
$\overline{\text{RAS}}$ to column address delay time	t <sub>RAD</sub>	15	30	15	35	15	40	ns	9
$\overline{\text{RAS}}$ hold time	t <sub>RSH</sub>	15	—	20	—	20	—	ns	
$\overline{\text{CAS}}$ hold time	t <sub>CSH</sub>	60	—	70	—	80	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t <sub>CRP</sub>	10	—	10	—	10	—	ns	
Transition time (rise and fall)	t <sub>T</sub>	3	50	3	50	3	50	ns	7
Refresh period	t <sub>REF</sub>	—	16	—	16	—	16	ms	
Refresh period (L-version)	t <sub>REF</sub>	—	128	—	128	—	128	ms	

## HM514100D Series

### Read Cycle

Parameter	Symbol	HM514100D						Unit	Notes
		-6		-7		-8			
		Min	Max	Min	Max	Min	Max		
Access time from $\overline{\text{RAS}}$	$t_{\text{RAC}}$	—	60	—	70	—	80	ns	2, 3, 16
Access time from $\overline{\text{CAS}}$	$t_{\text{CAC}}$	—	15	—	20	—	20	ns	3, 4, 14, 16
Access time from address	$t_{\text{AA}}$	—	30	—	35	—	40	ns	3, 5, 14, 16
Read command setup time	$t_{\text{RCS}}$	0	—	0	—	0	—	ns	
Read command hold time to $\overline{\text{CAS}}$	$t_{\text{RCH}}$	0	—	0	—	0	—	ns	17
Read command hold time to $\overline{\text{RAS}}$	$t_{\text{RRH}}$	0	—	0	—	0	—	ns	17
Column address to $\overline{\text{RAS}}$ lead time	$t_{\text{RAL}}$	30	—	35	—	40	—	ns	
Output buffer turn-off time	$t_{\text{OFF}}$	0	15	0	20	0	20	ns	6

### Write Cycle

Parameter	Symbol	HM514100D						Unit	Notes
		-6		-7		-8			
		Min	Max	Min	Max	Min	Max		
Write command setup time	$t_{\text{WCS}}$	0	—	0	—	0	—	ns	10
Write command hold time	$t_{\text{WCH}}$	15	—	15	—	15	—	ns	
Write command pulse width	$t_{\text{WP}}$	10	—	10	—	10	—	ns	
Write command to $\overline{\text{RAS}}$ lead time	$t_{\text{RWL}}$	15	—	20	—	20	—	ns	
Write command to $\overline{\text{CAS}}$ lead time	$t_{\text{CWL}}$	15	—	20	—	20	—	ns	
Data-in setup time	$t_{\text{DS}}$	0	—	0	—	0	—	ns	11
Data-in hold time	$t_{\text{DH}}$	15	—	15	—	15	—	ns	11

### Read-Modify-Write Cycle

Parameter	Symbol	HM514100D						Unit	Notes
		-6		-7		-8			
		Min	Max	Min	Max	Min	Max		
Read-modify-write cycle time	$t_{\text{RWC}}$	130	—	155	—	175	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay time	$t_{\text{RWD}}$	60	—	70	—	80	—	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ delay time	$t_{\text{CWD}}$	15	—	20	—	20	—	ns	10
Column address to $\overline{\text{WE}}$ delay time	$t_{\text{AWD}}$	30	—	35	—	40	—	ns	10



## HM514100D Series

### Refresh Cycle

		HM514100D							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{\text{CAS}}$ setup time (CBR refresh cycle)	$t_{\text{CSR}}$	10	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ hold time (CBR refresh cycle)	$t_{\text{CHR}}$	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ precharge to $\overline{\text{CAS}}$ hold time	$t_{\text{RPC}}$	10	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ precharge time in normal mode	$t_{\text{CPN}}$	10	—	10	—	10	—	ns	

### Fast Page Mode Cycle

		HM514100D							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Fast page mode cycle time	$t_{\text{PC}}$	40	—	45	—	50	—	ns	
Fast page mode $\overline{\text{CAS}}$ precharge time	$t_{\text{CP}}$	10	—	10	—	10	—	ns	
Fast page mode $\overline{\text{RAS}}$ pulse width	$t_{\text{RASC}}$	—	100000	—	100000	—	100000	ns	13
Access time from $\overline{\text{CAS}}$ precharge	$t_{\text{ACP}}$	—	35	—	40	—	45	ns	3, 14, 16
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	$t_{\text{RHCP}}$	35	—	40	—	45	—	ns	

### Fast Page Mode Read-Modify-Write Cycle

		HM514100D							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Fast page mode read-modify-write cycle time	$t_{\text{PCM}}$	60	—	70	—	75	—	ns	
$\overline{\text{CAS}}$ precharge to $\overline{\text{WE}}$ delay time	$t_{\text{CPW}}$	35	—	40	—	45	—	ns	10

## HM514100D Series

### Test Mode Cycle

Parameter	Symbol	HM514100D						Unit	Notes
		-6		-7		-8			
		Min	Max	Min	Max	Min	Max		
Test mode $\overline{WE}$ setup time	$t_{WS}$	0	—	0	—	0	—	ns	
Test mode $\overline{WE}$ hold time	$t_{WH}$	10	—	10	—	10	—	ns	

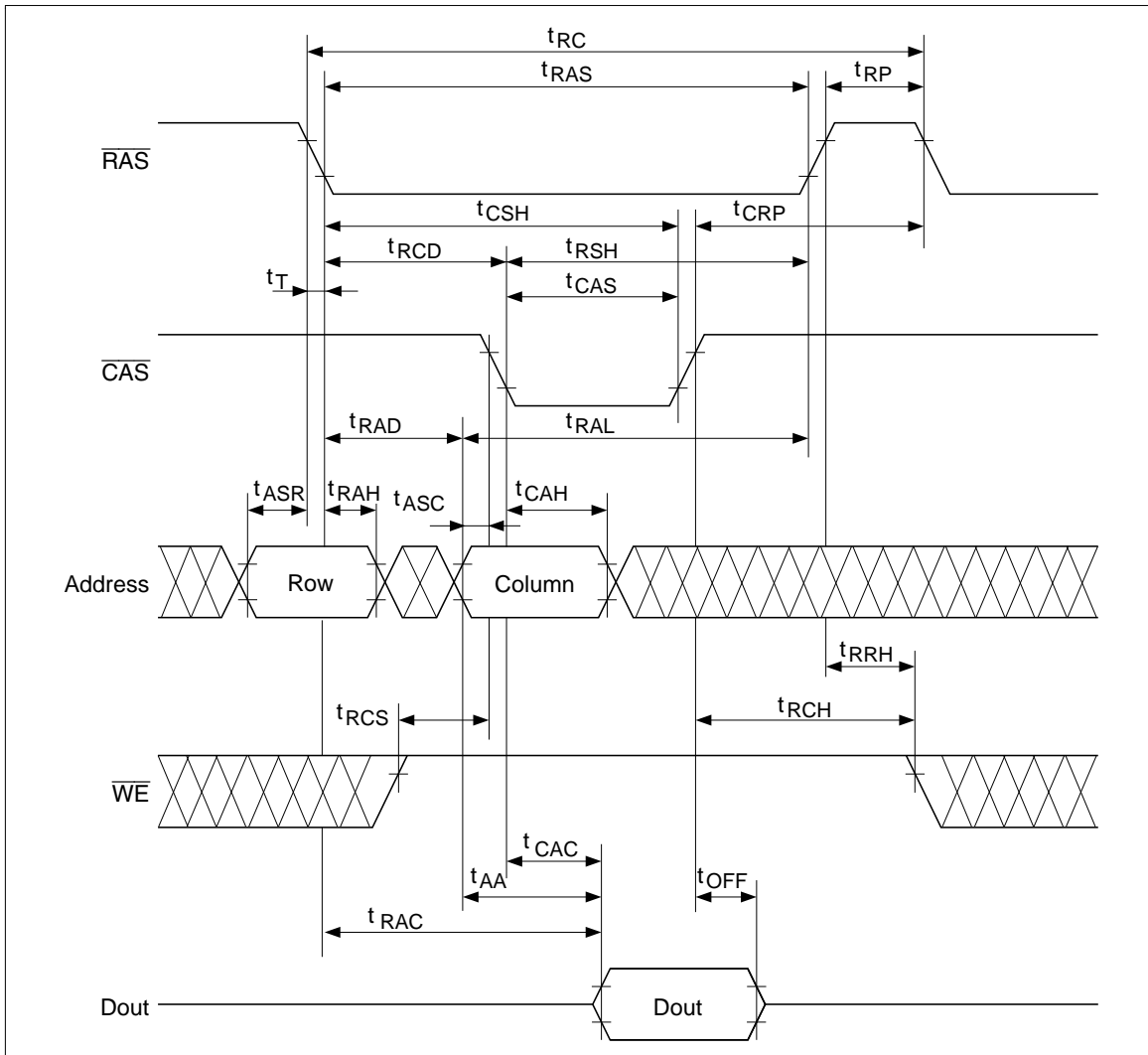
- Notes:
- AC measurements assume  $t_T = 5$  ns.
  - Assumes that  $t_{RCD} \leq t_{RCD}(\text{max})$  and  $t_{RAD} \leq t_{RAD}(\text{max})$ . If  $t_{RCD}$  or  $t_{RAD}$  is greater than the maximum recommended value shown in this table,  $t_{RAC}$  exceeds the value shown.
  - Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
  - Assumes that  $t_{RCD} \geq t_{RCD}(\text{max})$  and  $t_{RAD} \leq t_{RAD}(\text{max})$ .
  - Assumes that  $t_{RCD} \leq t_{RCD}(\text{max})$  and  $t_{RAD} \geq t_{RAD}(\text{max})$ .
  - $t_{OFF}(\text{max})$  defines the time at which the output achieves the open circuit condition and is not referred to output voltage levels.
  - $V_{IH}(\text{min})$  and  $V_{IL}(\text{max})$  are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
  - Operation with the  $t_{RCD}(\text{max})$  limit insures that  $t_{RAC}(\text{max})$  can be met,  $t_{RCD}(\text{max})$  is specified as a reference point only, if  $t_{RCD}$  is greater than the specified  $t_{RCD}(\text{max})$  limit, then access time is controlled exclusively by  $t_{CAC}$ .
  - Operation with the  $t_{RAD}(\text{max})$  limit insures that  $t_{RAC}(\text{max})$  can be met,  $t_{RAD}(\text{max})$  is specified as a reference point only, if  $t_{RAD}$  is greater than the specified  $t_{RAD}(\text{max})$  limit, then access time is controlled exclusively by  $t_{AA}$ .
  - $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$ ,  $t_{AWD}$  and  $t_{CPW}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if  $t_{WCS} \geq t_{WCS}(\text{min})$ , the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if  $t_{RWD} \geq t_{RWD}(\text{min})$ ,  $t_{CWD} \geq t_{CWD}(\text{min})$ ,  $t_{AWD} \geq t_{AWD}(\text{min})$  and  $t_{CPW} \geq t_{CPW}(\text{min})$ , the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
  - These parameters are referred to  $\overline{CAS}$  leading edge in an early write cycle and to  $\overline{WE}$  leading edge in a delayed write or read-modify-write cycle.
  - An initial pause of 100  $\mu\text{s}$  is required after power up followed by a minimum of eight initialization cycles ( $\overline{RAS}$ -only refresh cycle or  $\overline{CAS}$ -before- $\overline{RAS}$  refresh cycle). If the internal refresh counter is used, a minimum of eight  $\overline{CAS}$ -before- $\overline{RAS}$  refresh cycles is required.
  - $t_{RASC}$  defines  $\overline{RAS}$  pulse width in fast page mode cycles.
  - Access time is determined by the longest among  $t_{AA}$ ,  $t_{CAC}$  and  $t_{ACP}$ .
  - Test mode operation specified in this data sheet is 8-bit test function controlled by control address bits - - - RA10, CA10 and CA0. This test mode operation can be performed by  $\overline{WE}$ -and- $\overline{CAS}$ -before- $\overline{RAS}$  (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of eight test bits do not accord each other, the condition of the output data is high level. When the state of test bits do not accord, the condition of the output data is low level. Data output pin is Dout and data input pin is Din. In order to end this test mode operation, perform a  $\overline{CAS}$ -before- $\overline{RAS}$  refresh cycle or a  $\overline{RAS}$ -only refresh cycle.

16. In a test mode read cycle, the value of  $t_{RAC}$ ,  $t_{AA}$ ,  $t_{CAC}$  and  $t_{ACP}$  is delayed for 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
17. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied
18.  $t_{RAS}(\text{min}) = t_{RWD}(\text{min}) + t_{RWL}(\text{min}) + t_r$  in read-modify-write cycle.
19.  $t_{CAS}(\text{min}) = t_{CWD}(\text{min}) + t_{CWL}(\text{min}) + t_r$  in read-modify-write cycle.
20. XXX: H or L (H:  $V_{IH}(\text{min}) \leq V_{IN} \leq V_{IH}(\text{max})$ , L:  $V_{IL}(\text{min}) \leq V_{IN} \leq V_{IL}(\text{max})$ )  
/////: Invalid Dout  
When the address, clock and input pins are not described on timing waveforms, their pins must be applied  $V_{IH}$  or  $V_{IL}$ .

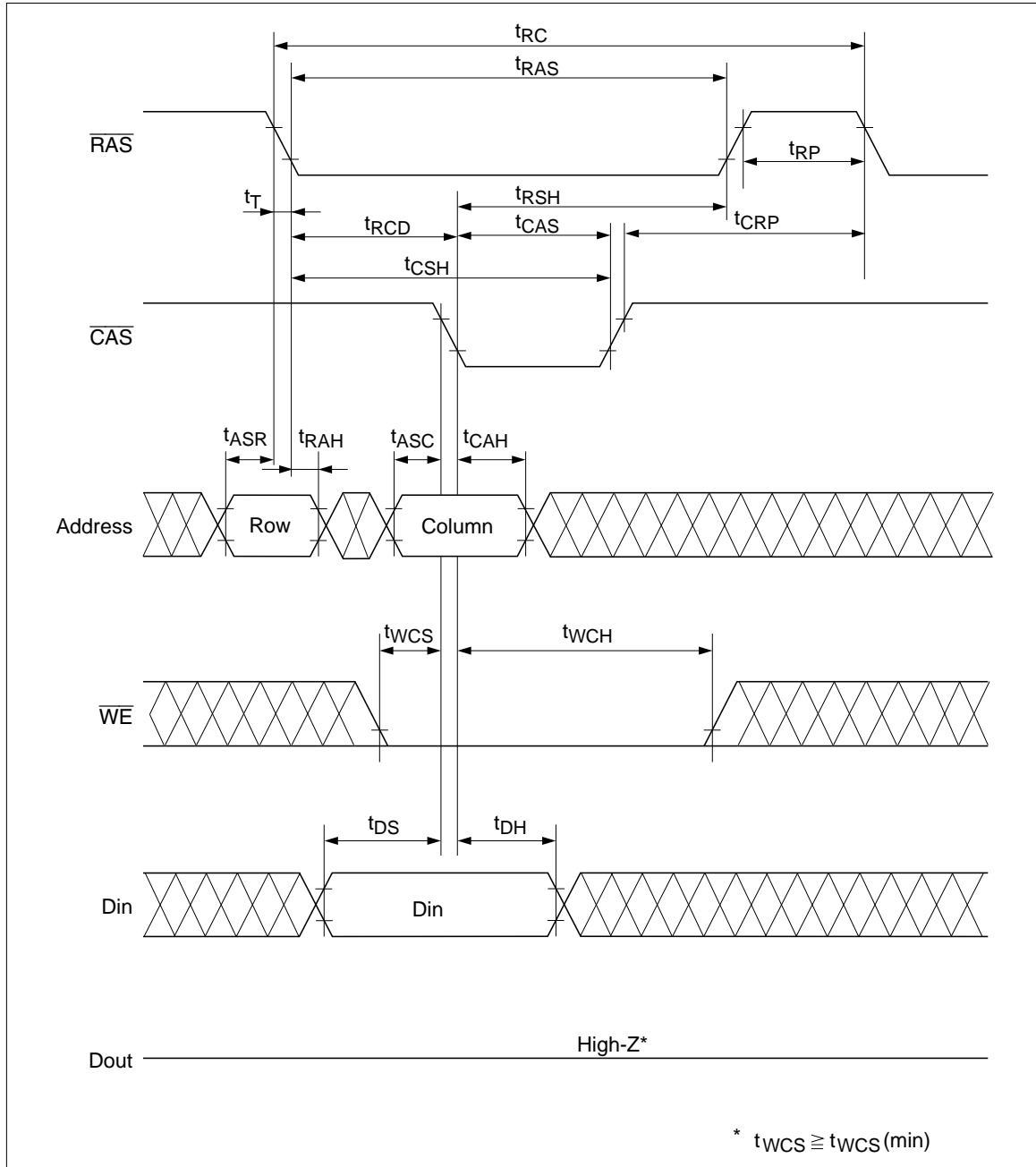
# HM514100D Series

## Timing Waveforms\*20

### Read Cycle

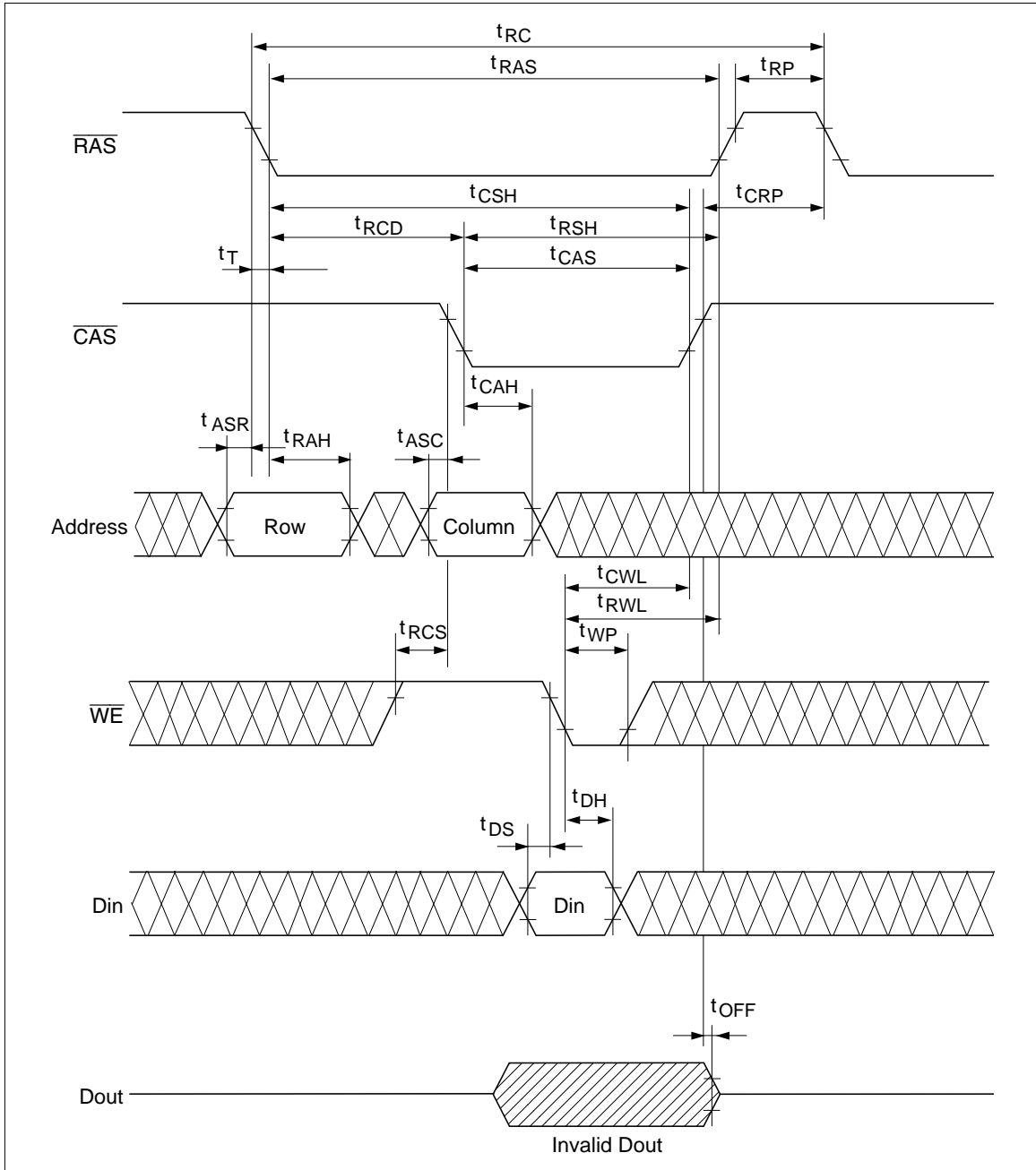


Early Write Cycle

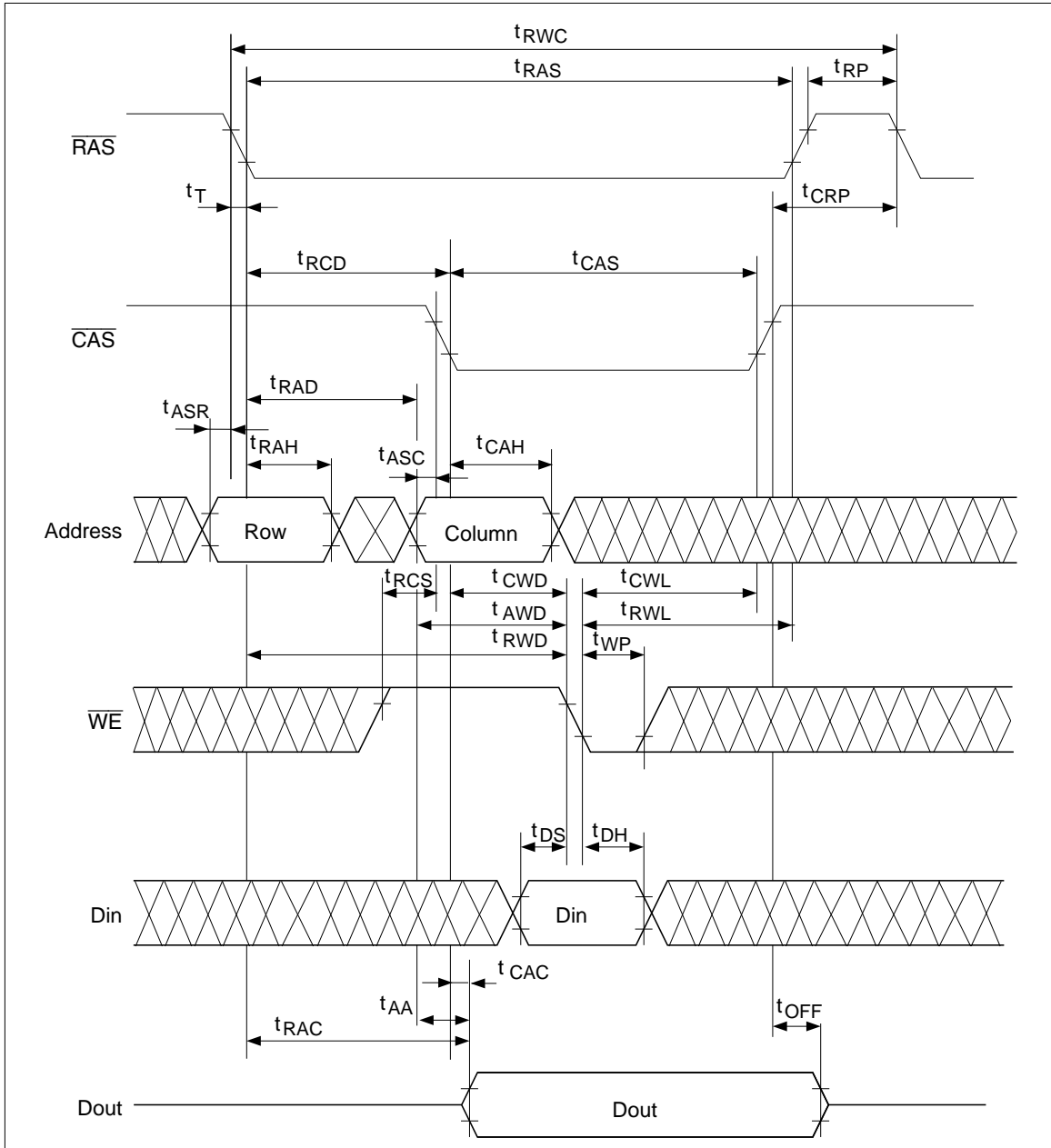


# HM514100D Series

## Delayed Write Cycle



Read-Modify-Write Cycle

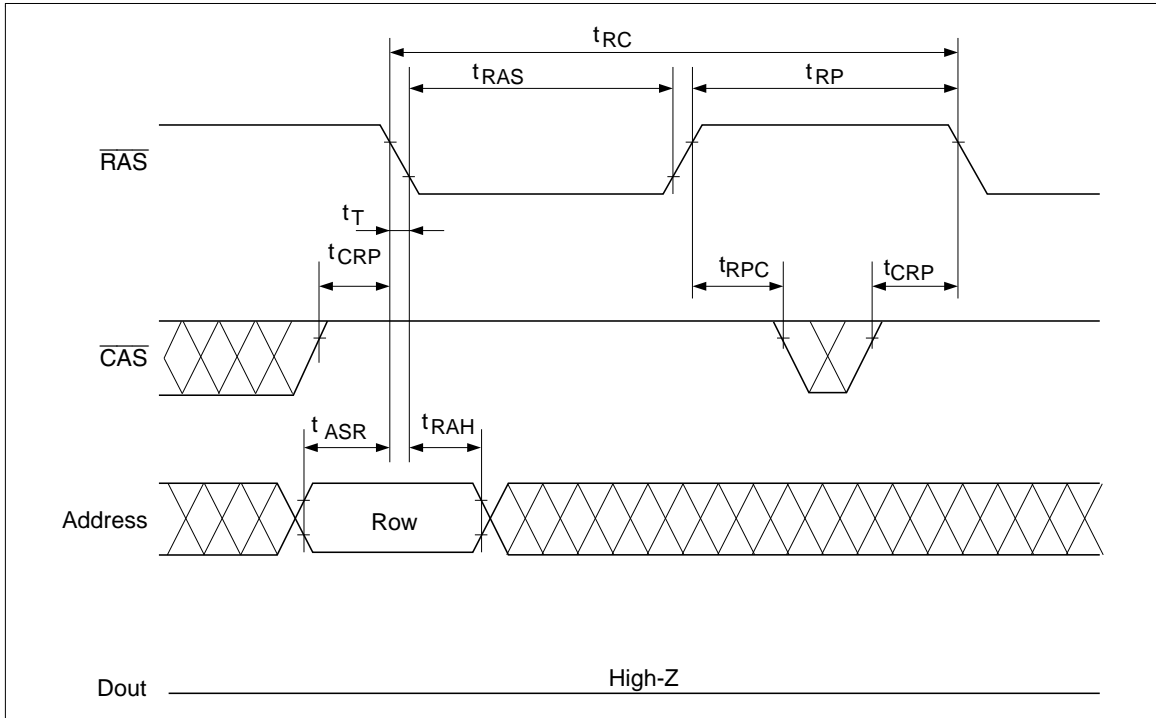


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## HM514100D Series

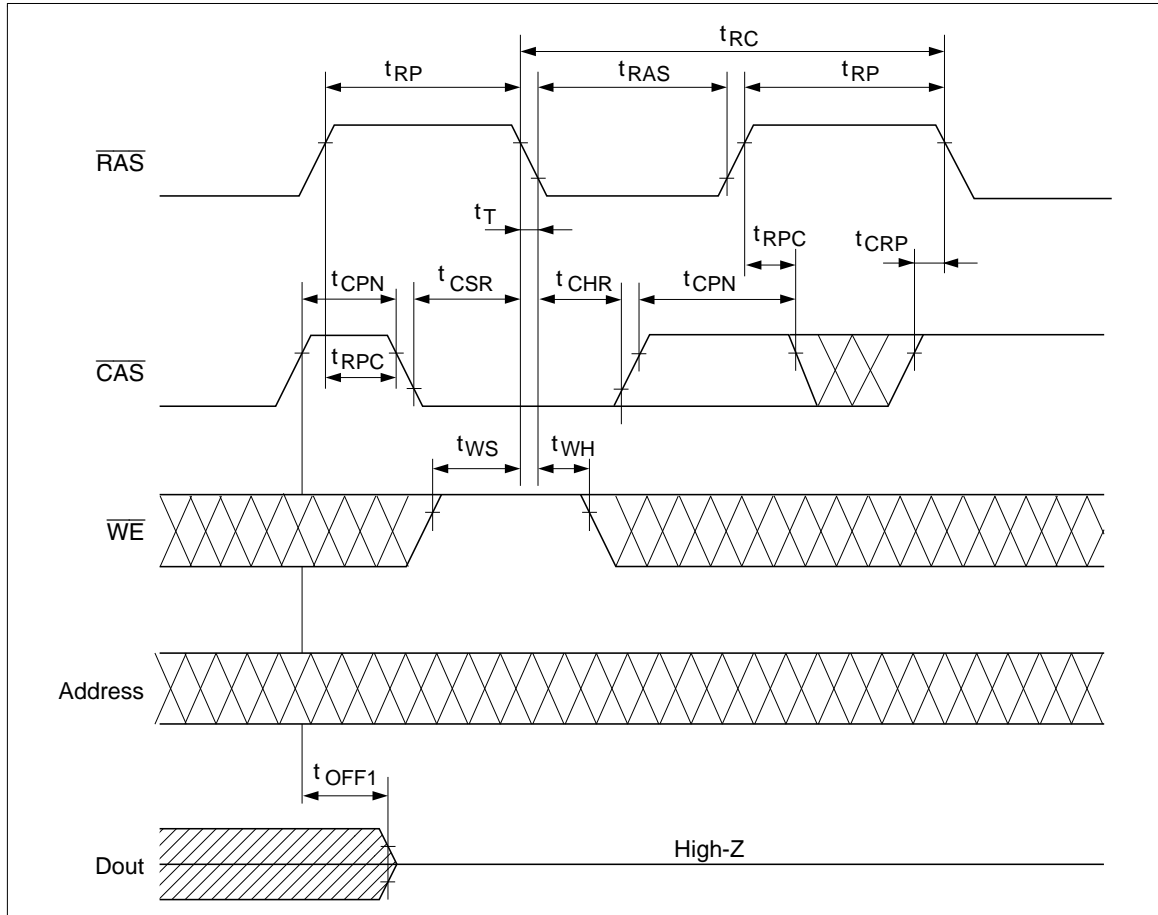
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### $\overline{\text{RAS}}$ -Only Refresh Cycle



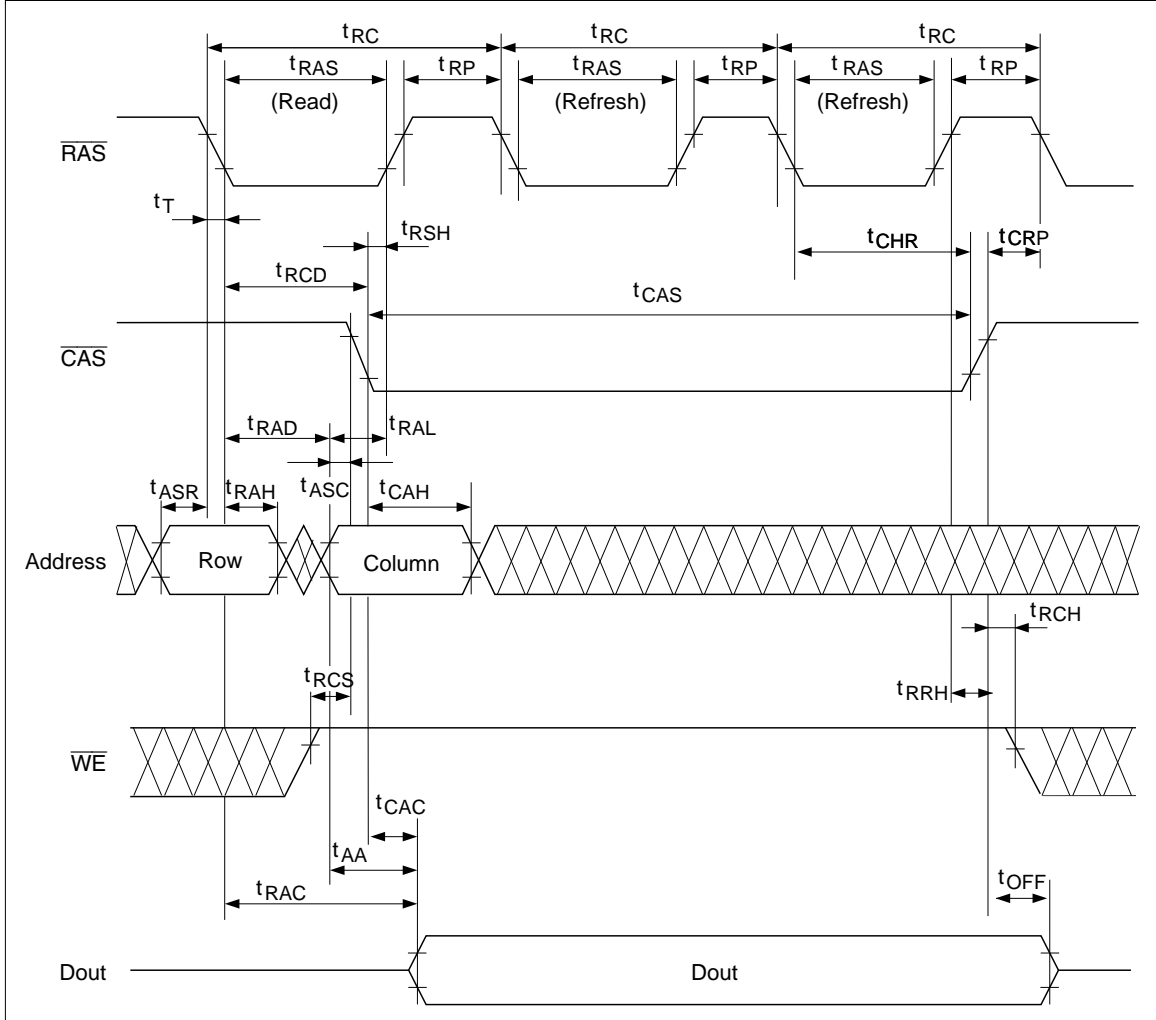


$\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$  Refresh Cycle

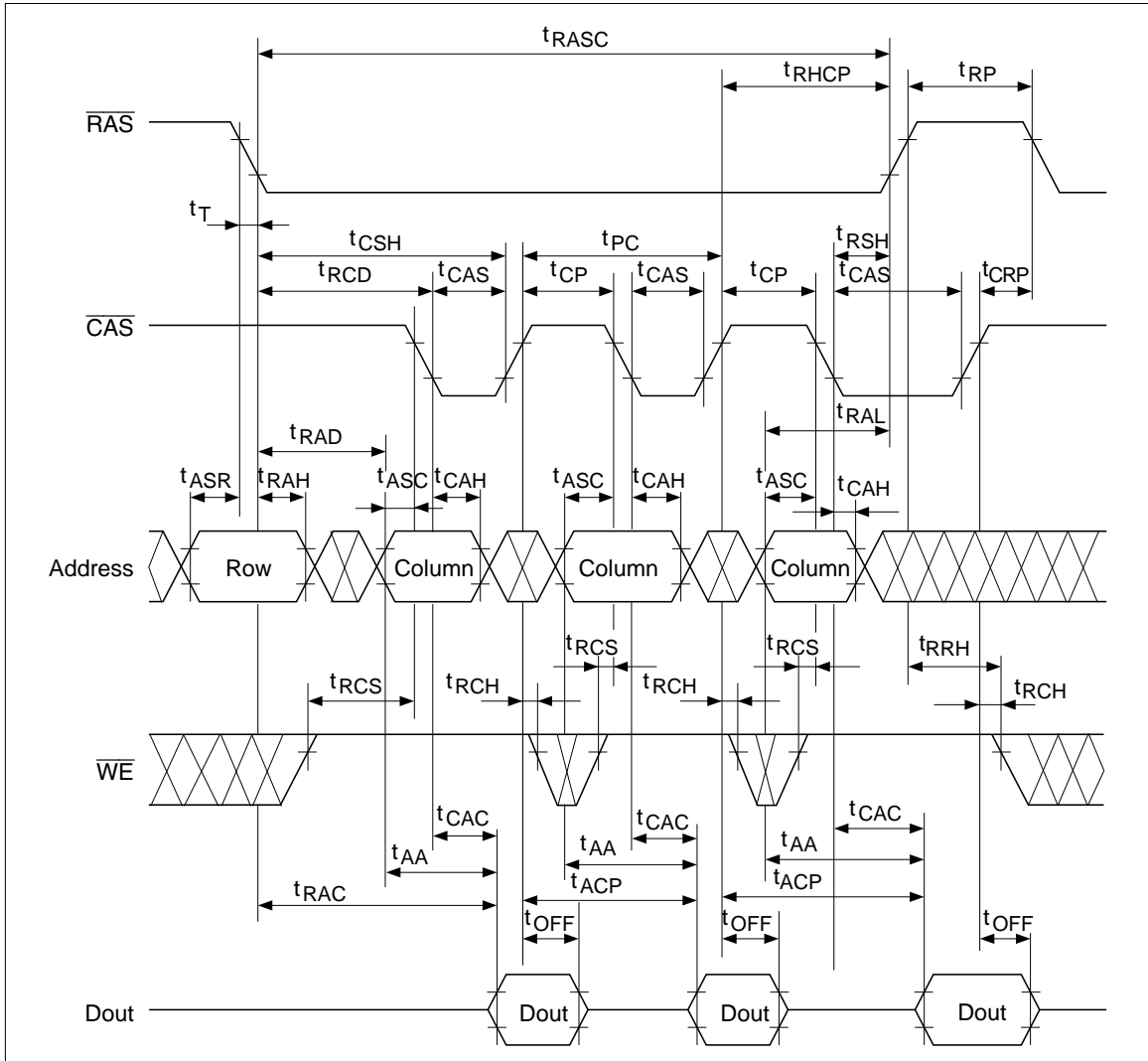


# HM514100D Series

## Hidden Refresh Cycle

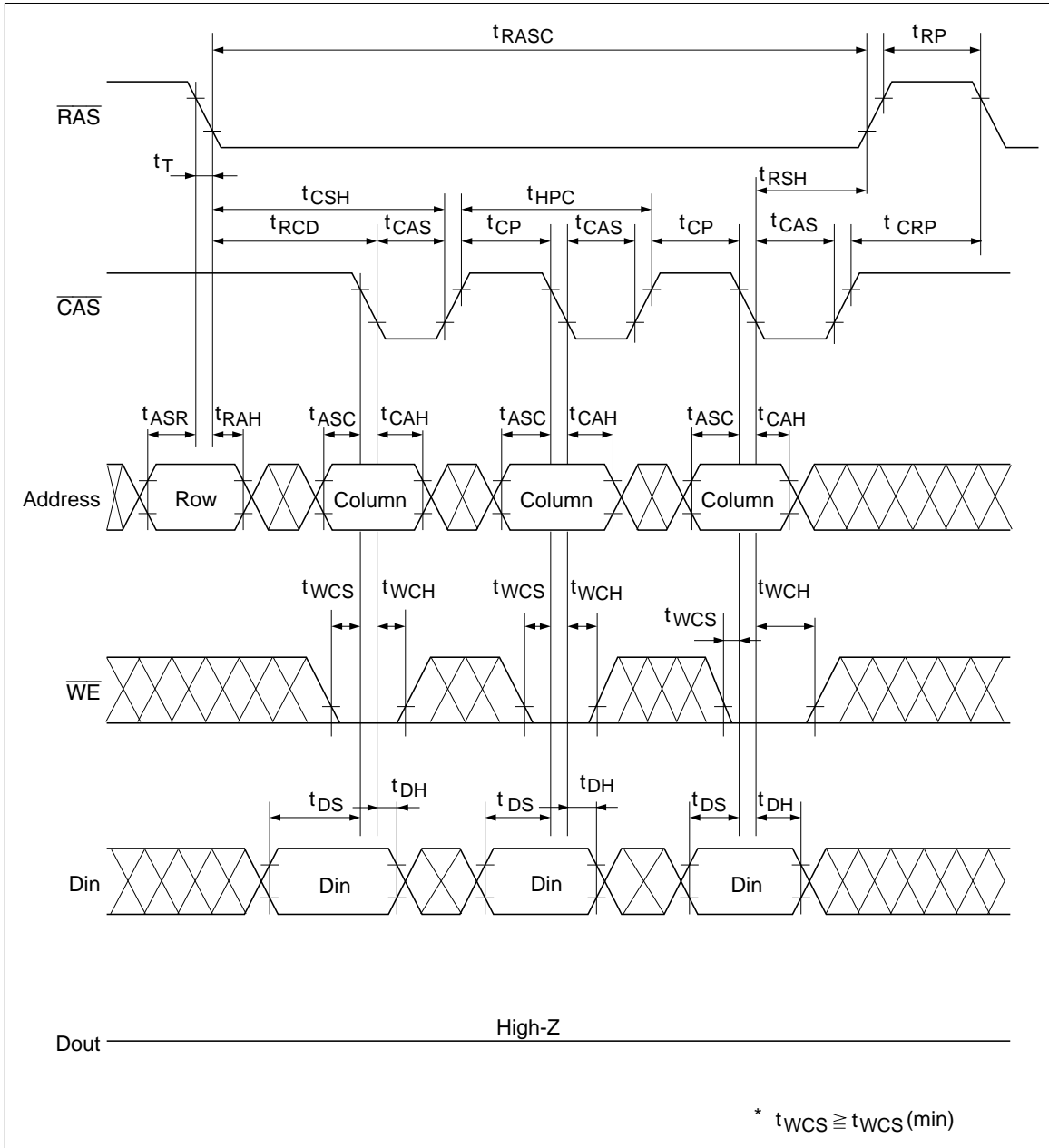


Fast Page Mode Read Cycle

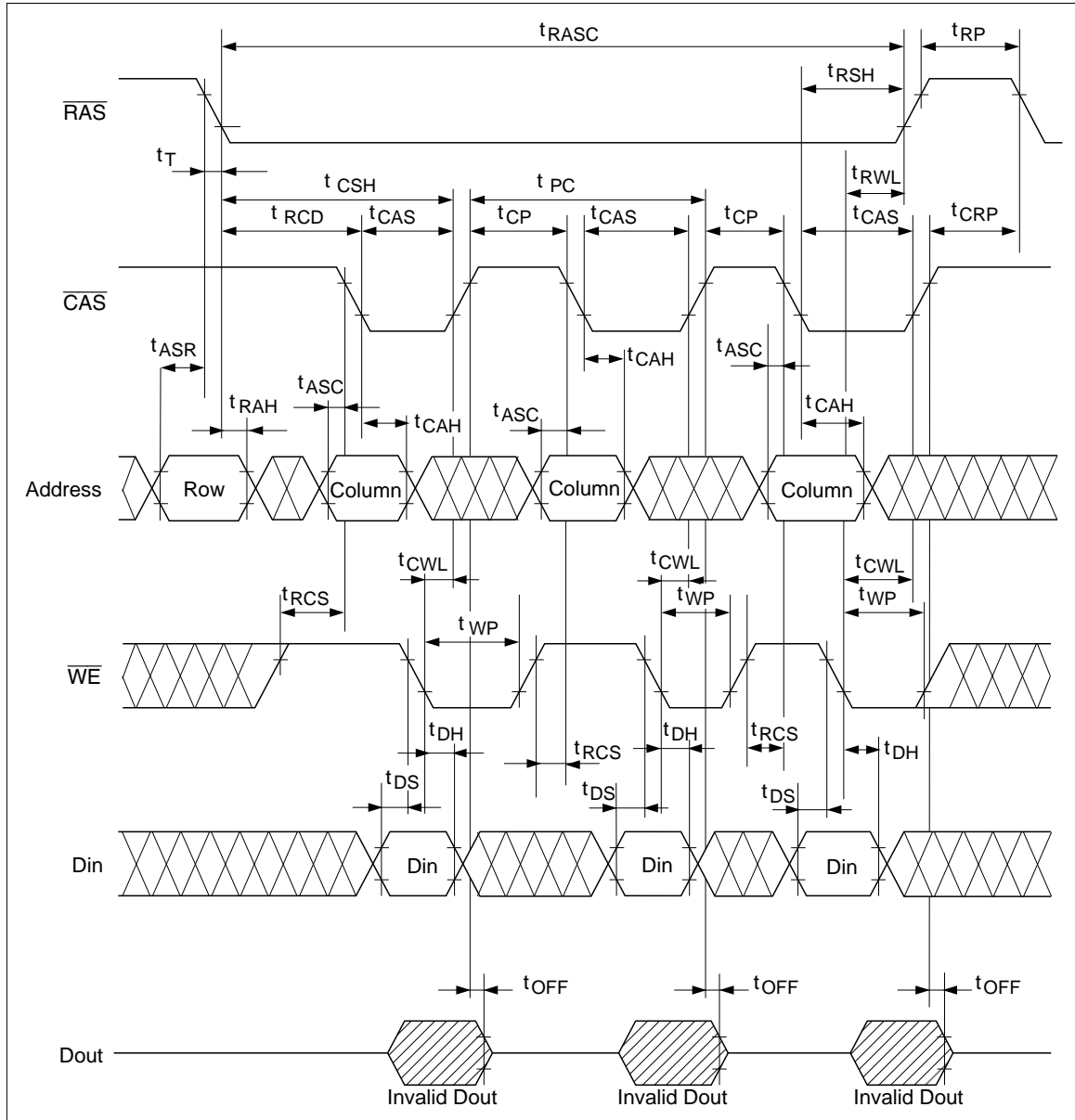


# HM514100D Series

## Fast Page Mode Early Write Cycle

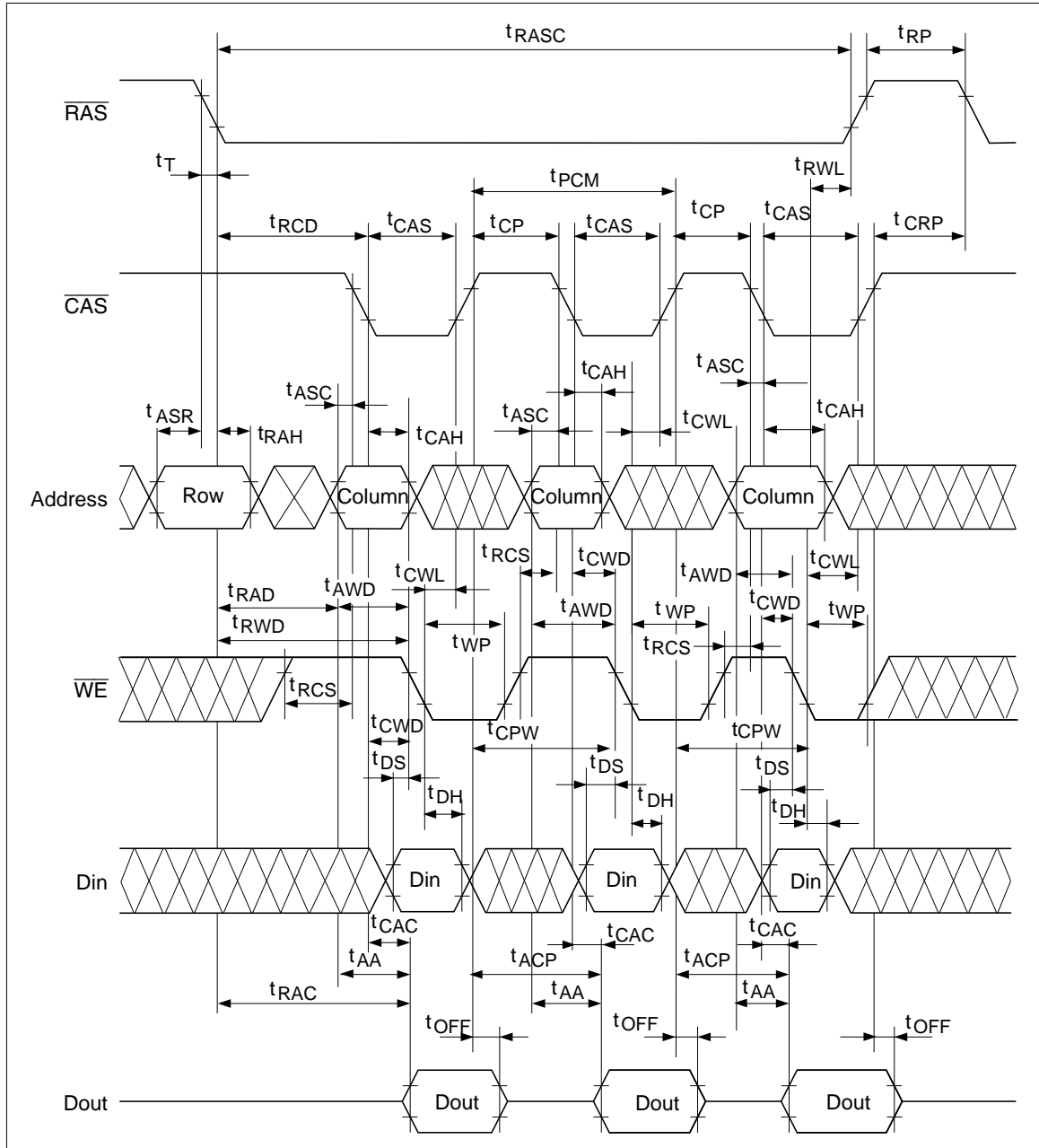


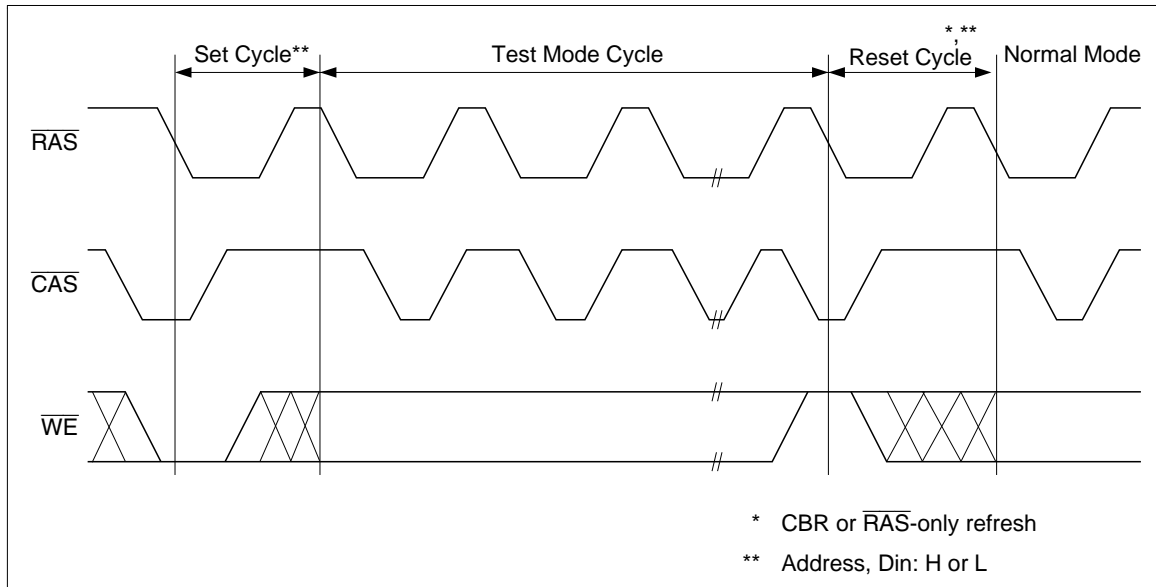
Fast Page Mode Delayed Write Cycle



# HM514100D Series

## Fast Page Mode Read-Modify-Write Cycle

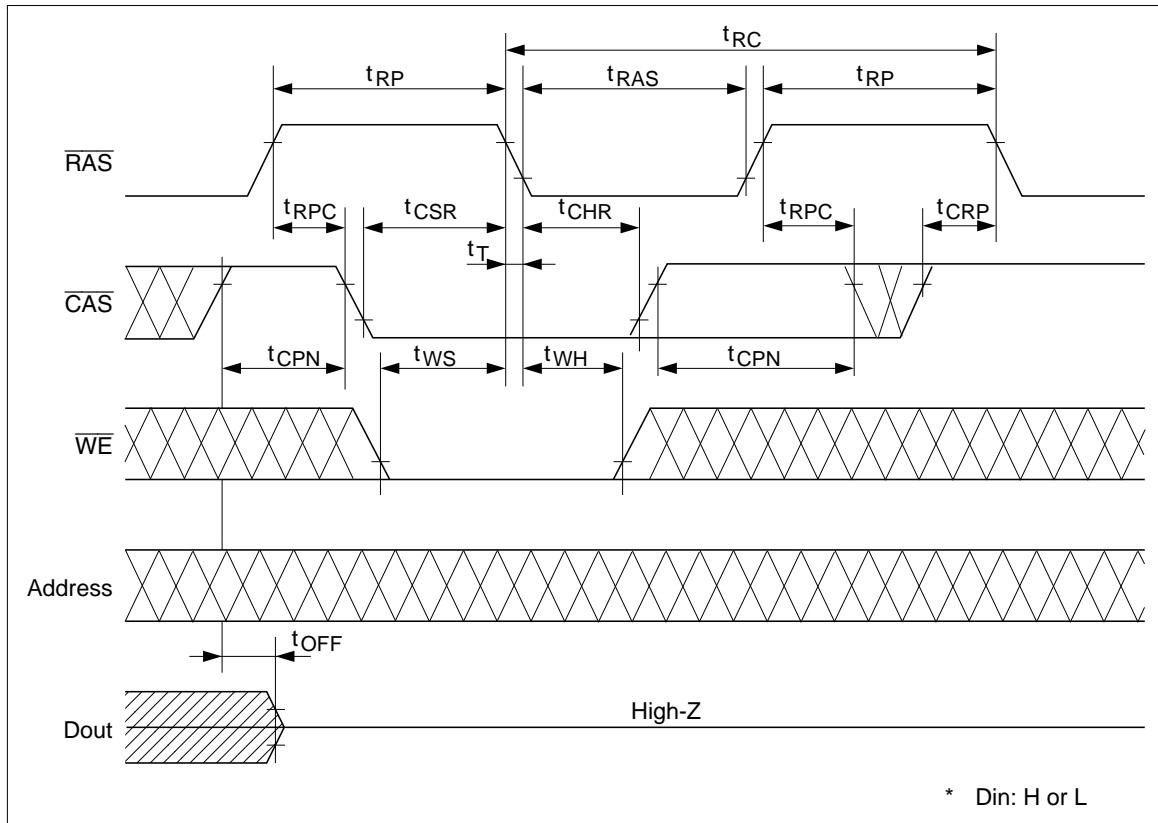


**Test Mode Cycle**

# HM514100D Series

## Test Mode Set Cycle

### $\overline{\text{WE}}$ -and- $\overline{\text{CAS}}$ -Before $\overline{\text{RAS}}$ -Refresh

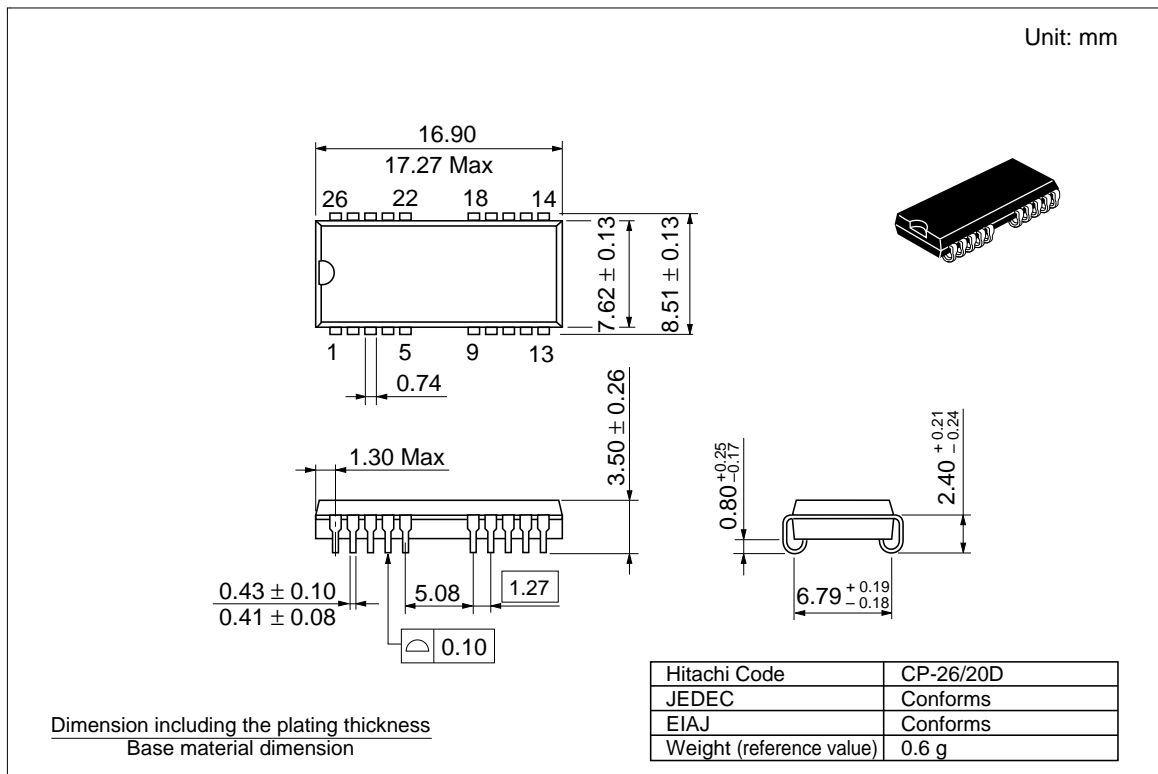




## HM514100D Series

### Package Dimensions

#### HM514100DS/DLS Series (CP-26/20D)



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## HM514100D Series

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**HM514100D Series**

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**Revision Record**

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0.0	Dec. 3, 1996	Initial issue	T. Oono	S. Suzuki
1.0	Nov. 13, 1997	Deletion of HM514100DTT Series		

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