

GaAs MMIC SP4T SWITCH NON-REFLECTIVE DC TO 3.5 GHz

FEBRUARY 2001

v02.0101

Features

- LOW INSERTION LOSS (2 GHz): 0.5dB
- SINGLE POSITIVE SUPPLY: Vdd = +5V
- INTEGRATED 2:4 TTL DECODER
- 16 LEAD QSOP PACKAGE



General Description

The HMC241QS16 is a low-cost non-reflective SP4T switch in a 16-lead QSOP package featuring wideband operation from DC to 3.5 GHz, covering all cellular/PCS (450 to 2000 MHz), wideband CDMA (2000-2300 MHz), wireless local loop (3500 MHz), industrial, scientific, and medical (900 and 2400 MHz), and CATV/DBS (50 to 2150 MHz) bands. The switch offers a single positive bias and true TTL/CMOS compatibility. A 2:4 decoder is integrated on the switch requiring only 2 control lines and a positive bias to select each path, replacing 8 control lines normally required by GaAs SP4T switches.

Guaranteed Performance

For TTL Control and Vdd = +5V in a 50 Ohm system, -40 to +85 deg C

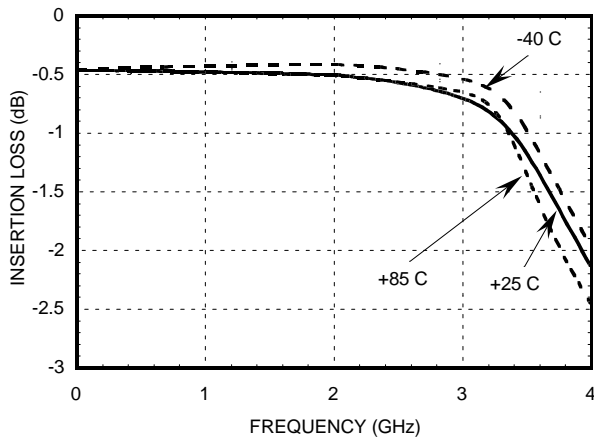
Parameter	Frequency	Min.	Typ.	Max.	Units
Insertion Loss	DC - 1.0 GHz		0.5	0.8	dB
	DC - 2.0 GHz		0.5	0.8	dB
	DC - 2.5 GHz		0.6	0.9	dB
	DC - 3.5 GHz		1.0	1.5	dB
Isolation	DC - 1.0 GHz	40	45		dB
	DC - 2.0 GHz	32	36		dB
	DC - 2.5 GHz	28	32		dB
	DC - 3.5 GHz	23	26		dB
Return Loss	"On State"	DC - 2.5 GHz	17	21	dB
		DC - 3.5 GHz	9	12	dB
Return Loss	RF1-4 "Off State"	0.3 - 3.5 GHz	8	12	dB
		0.5 - 2.5 GHz	12	16	dB
Input Power for 1dB Compression	0.3 - 3.5 GHz	22	25		dBm
Input Third Order Intercept (Two-Tone Input Power = +7dBm Each Tone)	0.3 - 3.5 GHz	40	44		dBm
Switching Characteristics	0.3 - 3.5 GHz				
tRISE, tFALL (10/90% RF)			40		ns
tON, tOFF (50% CTL to 10/90% RF)			150		ns

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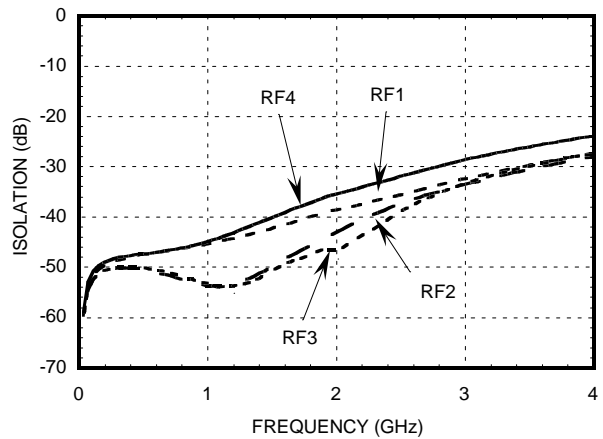
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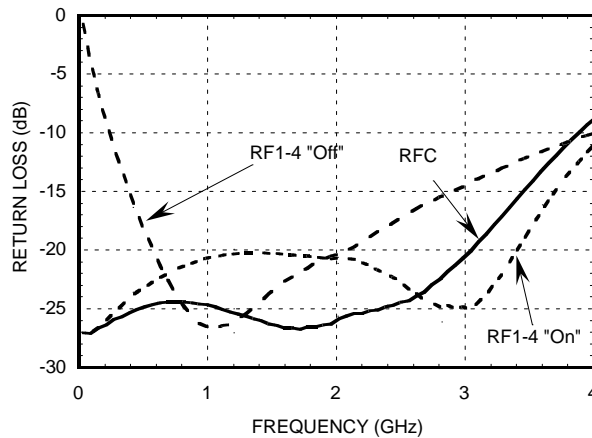
Insertion Loss



Isolation



Return Loss

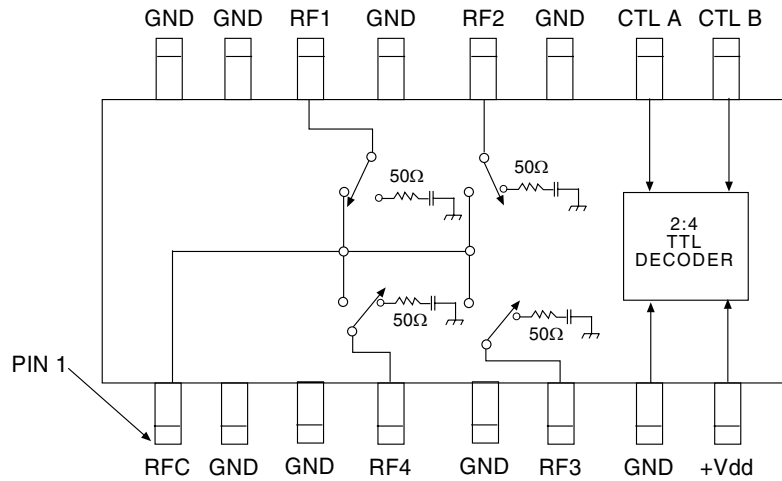


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Functional Diagram



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SMT SP4T SWITCHES

Absolute Maximum Ratings

Bias Voltage Range (Port Vdd)	+7.0 Vdc
Control Voltage Range (A & B)	-0.5V to Vdd + 1Vdc
Storage Temperature	-65 to +150 deg C
Operating Temperature	-40 to +85 deg C
Maximum Input Power Vdd = +5 Vdc	+20dBm (0.05-0.5GHz) +27dBm (0.5-3.5GHz)

NOTE:

- DC blocking capacitors are required at ports RFC and RF1, 2, 3, 4.

Truth Table

Control Input		Signal Path State
A	B	RFCOM to:
Low	Low	RF1
High	Low	RF2
Low	High	RF3
High	High	RF4

Bias Voltage & Current

Vdd Range = +5.0 Vdc ± 10%		
Vdd (Vdc)	Idd (Typ.) (mA)	Idd (Max.) (mA)
+5.0	4.0	7.0

TTL/CMOS Control Voltages

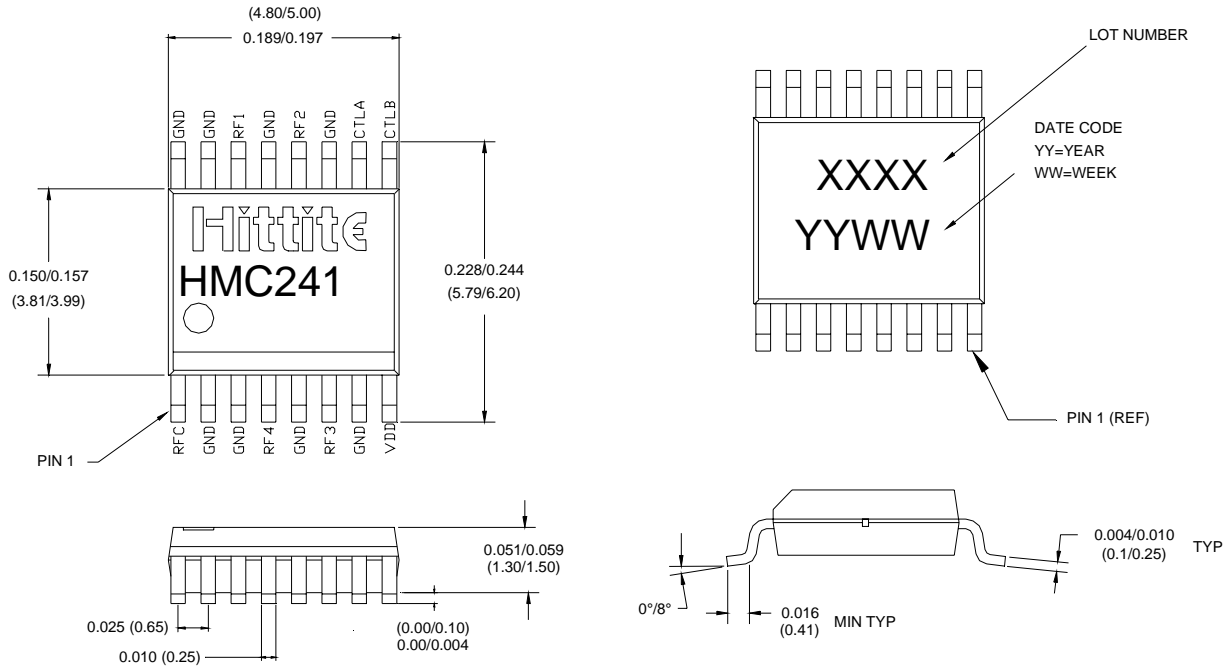
State	Bias Condition
Low	0 to +0.8 Vdc @ 5 uA Typ.
High	+2.0 to +5.0 Vdc @ 70 uA Typ.

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Outline Drawing



- 1) MATERIAL:
 - A) PACKAGE BODY: LOW STRESS INJECTION MOLDED PLASTIC, SILICA & SILICONE IMPREGNATED
 - B) LEADFRAME MATERIAL: COPPER ALLOY
2. PLATING: LEAD-TIN SOLDER PLATE
3. DIMENSIONS ARE IN INCHES (MILLIMETERS) UNLESS OTHERWISE SPECIFIED TOL. ARE $\pm 0.005 (\pm 0.13)$