HMC394LP4

GaAs HBT PROGRAMMABLE 5-BIT COUNTER, DC - 2.2 GHz

Typical Applications

Programmable divider for offsett synthesizer and variable divide by N applications:

- Satellite Communication Systems
- Pt-Pt and Pt-MPt Radios
- LMDS
- SONET

Features

SSB Phase Noise: -153 dBc/Hz @ 100 kHz

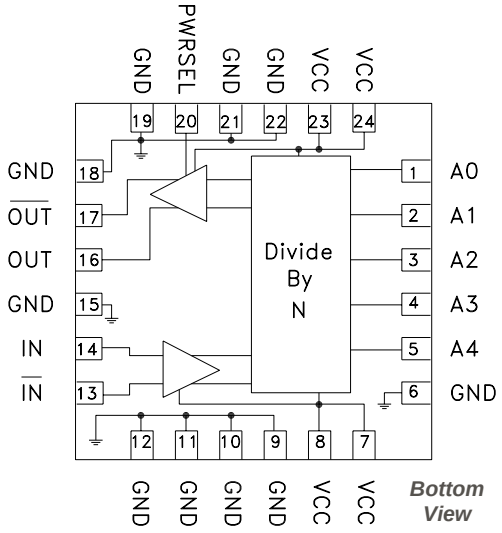
Selectable Division from 2 to 32

Parallel 5-Bit Control

Wide Input Power Range: -20 to +10 dBm

LP4 SMT Package

Functional Diagram



General Description

The HMC394LP4 is a low noise GaAs HBT programmable 5-bit counter in a leadless LP4 surface mount package. This device allows continuous division from N= 2 to 32 at input frequencies up to 2.2 GHz. The output voltage swing is 800 mV with a duty cycle inversely proportional to N. The low additive SSB phase noise of -153 dBc/Hz at 100 KHz offset makes this counter an excellent choice for low noise synthesizer applications.

Guaranteed Performance, Vcc= 5V, 25 Deg °C

Parameter	Conditions	Min.	Typ.	Max.	Units
Maximum Input Frequency				2.2	GHz
Minimum Input Frequency	Sine Wave Input. [1]	0.1			GHz
Input Power Range	Fin= 0.1 to 2.2 GHz	-15	>-20	+10	dBm
Output Power	Divide-by-2		4		dBm
SSB Phase Noise	Fin= 1 GHz, N= 4		-153		dBc/Hz
Output Transition Time			100		ps
Recommended Supply Voltage (Vcc)			5.0		Vdc
Supply Current (Icc)			200		mA

1. Divider will operate down to DC for square-wave input signal.

For price, delivery, and to place orders, please contact Hittite Microwave Corporation:
12 Elizabeth Drive, Chelmsford, MA 01824 Phone: 978-250-3343 Fax: 978-250-3373
Visit us at www.hittite.com, or Email at sales@hittite.com

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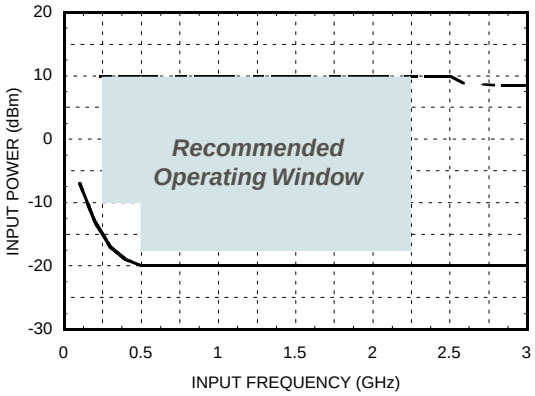
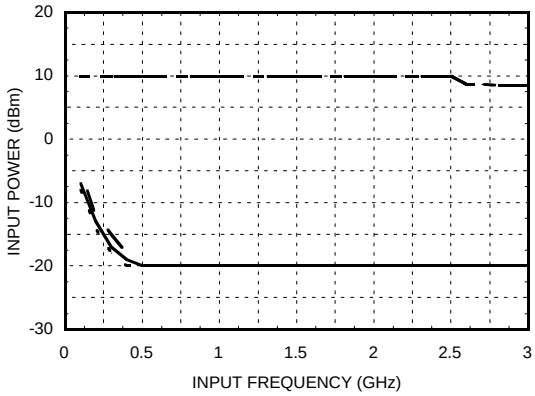
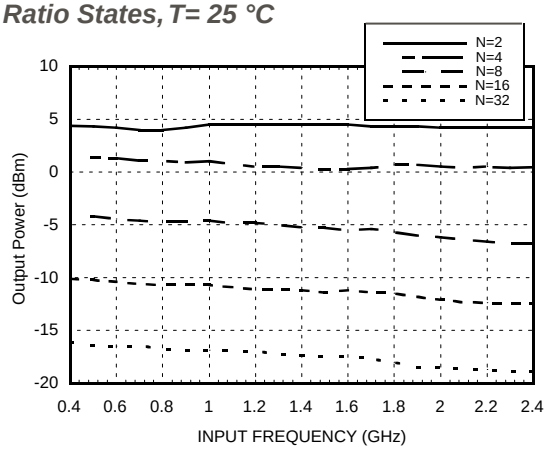
Input Sensitivity Window, 5 major Divide Ratio States, T= 25 °C



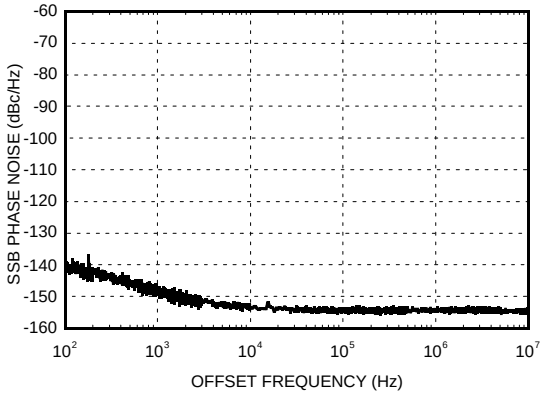
Input Sensitivity Window vs. Temperature, N= 16, T= -40 °C to +85 °C



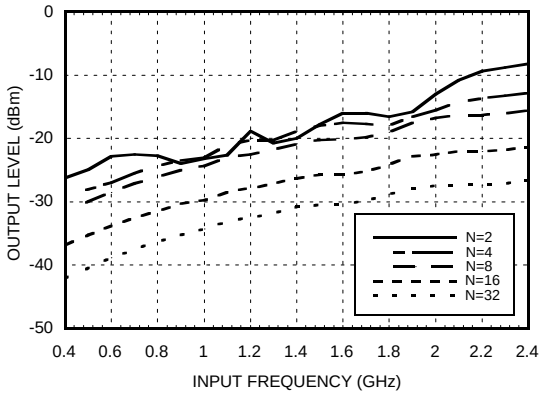
Output Power, 5 Major Divide Ratio States, T= 25 °C



SSB Phase Noise Performance, Fin= 1 GHz, N= 4, T= 25 °C



Fundamental Feedthru Power, Pin= 0 dBm, T= 25 °C



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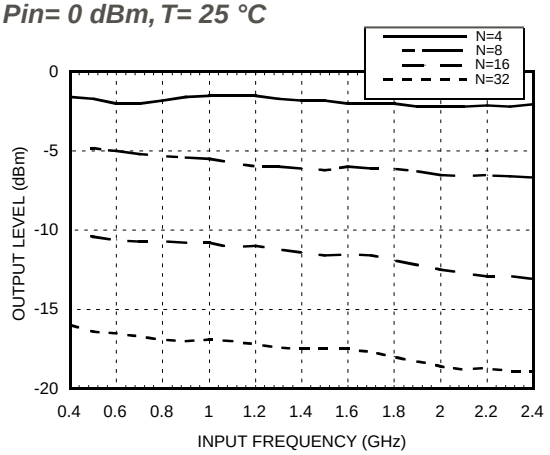
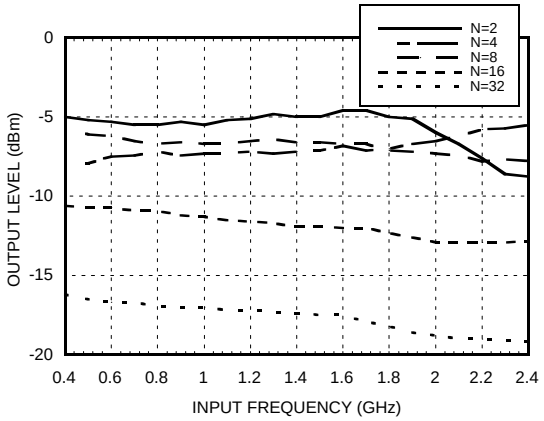
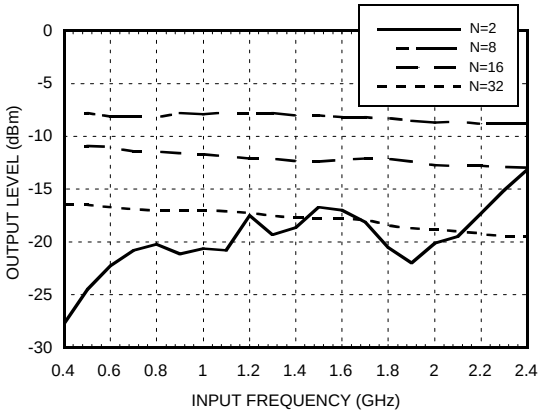
2nd Harmonic, Pin= 0 dBm, T= 25 °C



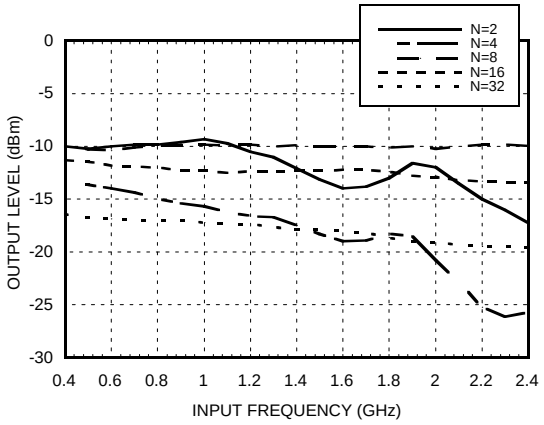
3rd Harmonic, Pin= 0 dBm, T= 25 °C



4th Harmonic, Pin= 0 dBm, T= 25 °C



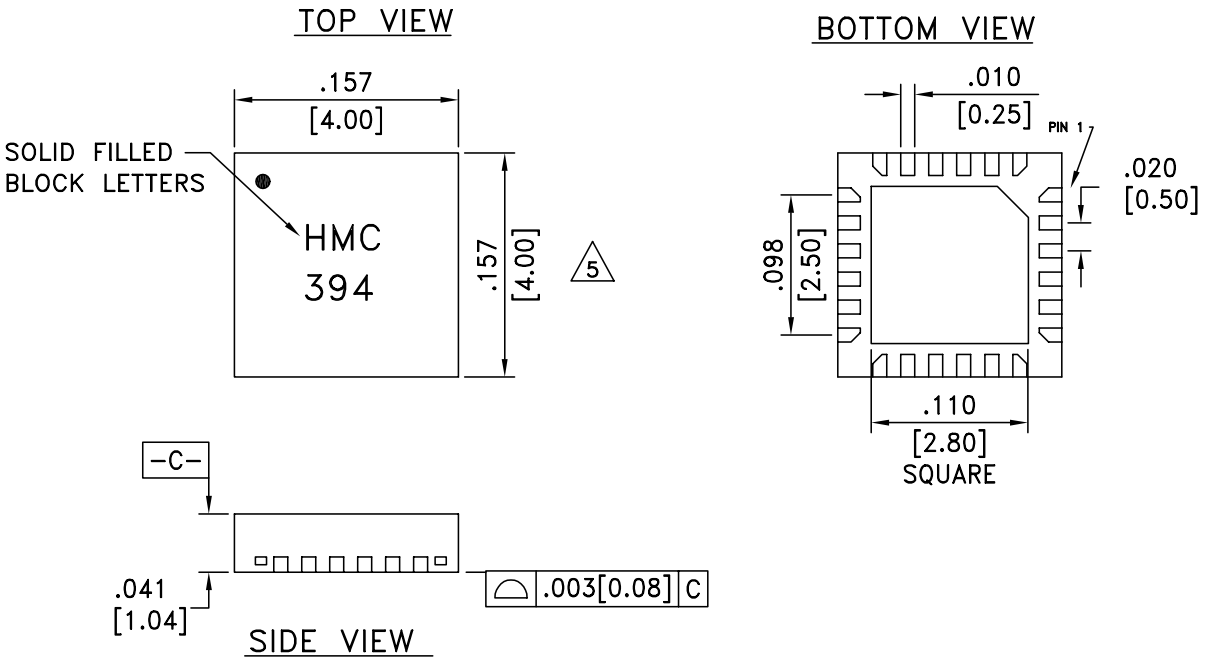
5th Harmonic, Pin= 0 dBm, T= 25 °C



Absolute Maximum Ratings

RF Input (Vcc = +5V)	+13 dBm
Vcc	+5.5V
VLogic	-1.6 to -1.2 Vcc
Storage Temperature	-65 to +150 deg C
Operating Temperature	-55 to +85 deg C

Pin Locations & Outline Drawing



1. MATERIAL:

   A. PACKAGE BODY - LOW STRESS INJECTION-MOLDED PLASTIC, SILICA & SILICONE INPREGNATED.
   B. LEADFRAME MATERIAL: COPPER ALLOY

2. PLATING: LEAD-TIN SOLDER PLATE

3. DIMENSIONS ARE IN INCHES (MILLIMETERS)

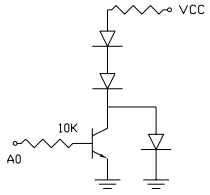
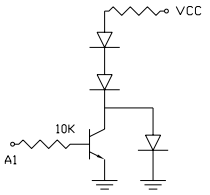
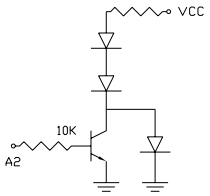
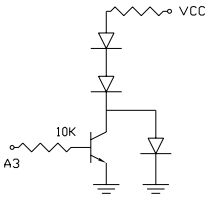
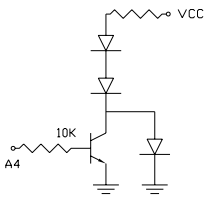
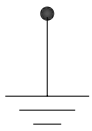
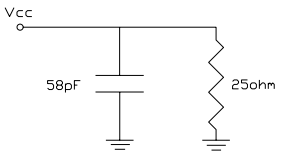
4. CHARACTERS TO BE HELVETICA MEDIUM, .020 HIGH USING WHITE INK, LOCATED APPROX AS SHOWN

5. DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.15mm PER SIDE.

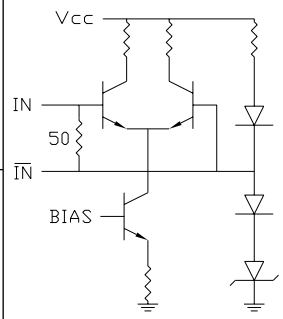
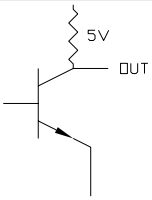
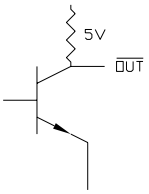
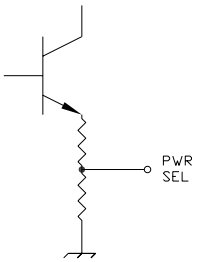
6. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM
   PAD BURR HEIGHT SHALL BE .25mm MAXIMUM.

7. PACKAGE WARP SHALL NOT EXCEED .050mm

Pin Description

Pin Number	Function	Description	Interface Schematic
1	AO	CMOS compatable control input bit 0 (LSB).	
2	A1	CMOS compatable control input bit 1.	
3	A2	CMOS compatable control input bit 2.	
4	A3	CMOS compatable control input bit 3.	
5	A4	CMOS compatable control input bit 4.	
6, 9, 10, 11, 12, 15, 18, 19, 21, 22	GND	Ground: Backside of package has exposed metal ground slug which must be connected to ground.	
7, 8, 23, 24	VCC	Supply voltage 5V ± 0.25V must be applied to all four pins.	

Pin Description *(continued)*

Pin Number	Function	Description	Interface Schematic
13	$\overline{IN}$	RF input 180° out of phase with pin 14 must be AC ground.	
14	IN	RF input must be DC blocked.	
16	OUT	Divided output pulse.	
17	$\overline{OUT}$	Divided output pulse 180° out of phase with pin 16.	
20	PWR SEL	In the low power mode, the power select pin is left floating. By grounding this pin, the output power is increased by approximately 6 dB.	

HMC394LP4 Programming Truth Table

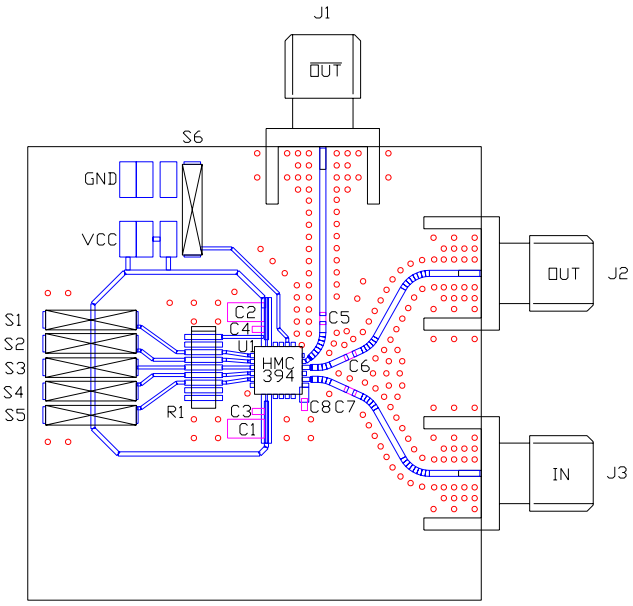
Function	(LSB) A0	A1	A2	A3	A4
/ 2	1	0	0	0	0
/ 3	0	1	0	0	0
/ 4	1	1	0	0	0
-	-	-	-	-	-
/ 32	1	1	1	1	1
Note: A0 through A4 are CMOS compatable logic control inputs.					

HMC394LP4 Evaluation PCB Truth Table

Note:
The evaluation PCB for the HMC394LP4 contains 10K Ohm pull up resistors for each of the five control inputs A0 through A4. Programming the 31 distinct division ratios, consists of installing or removing jumpers S1 through S5, as shown below.

Function	S1	S2	S3	S4	S5
/ 2	1	0	0	0	0
/ 3	0	1	0	0	0
/ 4	1	1	0	0	0
-	-	-	-	-	-
/ 32	1	1	1	1	1
Note: 0= Jumper installed. 1= Jumper no installed. Install jumper S6 for high power mode.					

HMC394LP4 Evaluation PCB



The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and backside ground slug should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Note: C1 and C3 bypass capacitors are not necessary if power supply trace is short.

Evaluation Circuit Board Layout Design Details

Item	Description
J1 - J3	PC Mount SMA RF Connector
C1 - C2*	1.0 µF Tantalum Capacitor
C3 - C4*	.01 µF Capacitor, 0603 Pkg.
C5 - C8	1000 pF Capacitor, 0603 Pkg.
R1*	Resister SIP 10 K Ohm
S1 - S6	Jumper (shunt) 2mm
U1	HMC394LP4 5-Bit Counter
PCB	104435 Eval Board
* Optional components.	