HT9202A/B/C/D/F/G/H/L/S

1-Memory/2-Memory Tone/Pulse Dialer

Faxback Doc. # 9007546

Features

- Universal specification
- Operating voltage: 2.0V~5.5V
- Low stand-by current
- Low memory retention current: 0.1μA (Typ.)
- Tone/pulse switchable
- Interface with LCD driver
- 32 digits for redialing
- 32 digits for the SA memory dialing
- One-key redialing
- Pause and P→T key for PBX
- 4×4 keyboard matrix
- 3.58MHz crystal or ceramic resonator
- Hand-free control
- Hold-line control
- Pause, P→T can be saved for redialing
- Lock function for the HT9202L
- Resistor options:
  - M/B ratio
  - Flash function and flash time
  - Pause and P→T duration
  - Pulse number
- Memory number:
  - HT9202A/B/C/D/S: 2 memories
  - HT9202F/G/H/L: 1 memory

General Description

The HT9202 series tone/pulse dialers are CMOS LSIs for the telecommunication system. They are designed to meet various dialing specifications through resistor options matrix.

The HT9202 series tone/pulse dialers are offered in various packages from 16 DIP to 24 SDIP. The 16 DIP version is suitable for low cost applications, while the 24 SDIP version supplies versatile functions such as: Hold-line, Hand-free and LCD dialing number display interface, all of which are suitable for feature phone applications.

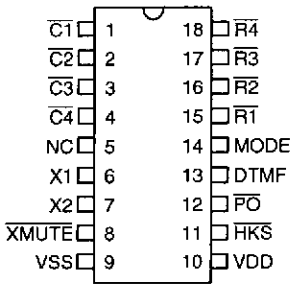
The HT9202L provides a long distance call lock for PABX.

Selection Table

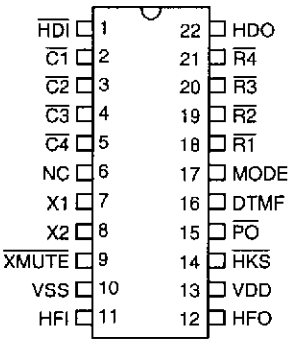
Function / Item	Memory No.	Memory Dialing	Hold-Line	Hand-Free	LCD Interface	Lock Function	Flash Function	Flash Time (ms)	Pulse No.	Tone Duration (ms)	Inter-Tone-Pause (ms)
HT9202A – 18 DIP	2	SA,R	—	—	—	—	Control	600	N,N+1 10–N	82.5	85.5
							Digit	600/300/98			
HT9202B – 22 SDIP	2	SA,R	√	√	—	—	Control	600	N,N+1 10–N	82.5	85.5
							Digit	600/300/98			
HT9202C – 20 DIP	2	SA,R	—	—	√	—	Control	600	N,N+1 10–N	82.5	85.5
							Digit	600/300/98			
HT9202D – 24 SDIP	2	SA,R	√	√	√	—	Control	600	N,N+1 10–N	82.5	85.5
							Digit	600/300/98			
HT9202F – 18 DIP	1	R	—	—	—	—	Control	600	N,N+1 10–N	82.5	85.5
							Digit	600/300/98			
HT9202G – 16 DIP	1	R	—	—	—	—	Control	600	N 10–N	100	106
							Digit	600/300/98			
HT9202H – 18 DIP	1	R/P	—	—	—	—	Control	600	N,N+1 10–N	82.5	85.5
							Digit	600/300/98			
HT9202L – 18 DIP	1	R	—	—	—	√	Control	600	N,N+1 10–N	82.5	85.5
							Digit	600/300/98			
HT9202S – 20 DIP	2	SA,R	√	—	—	—	Control	600	N,N+1 10–N	82.5	85.5
							Digit	600/300/98			

8th Feb '96

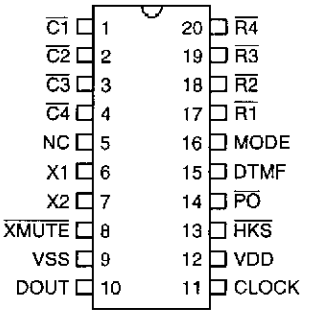
Package Information



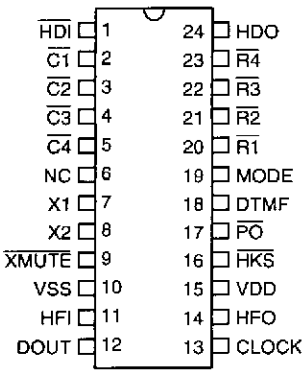
HT9202A
– 18 DIP



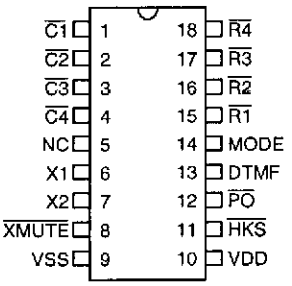
HT9202B
– 22 SDIP



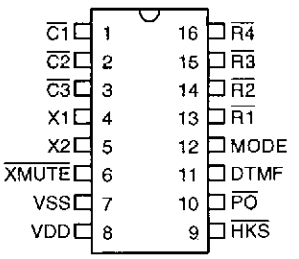
HT9202C
– 20 DIP



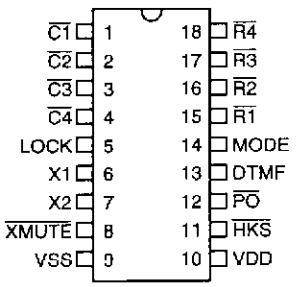
HT9202D
– 24 SDIP



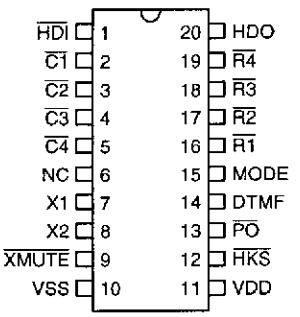
HT9202F/H
– 18 DIP



HT9202G
– 16 DIP



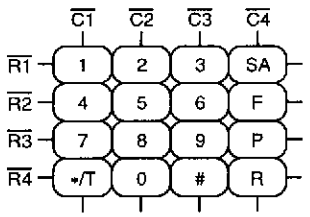
HT9202L
– 18 DIP



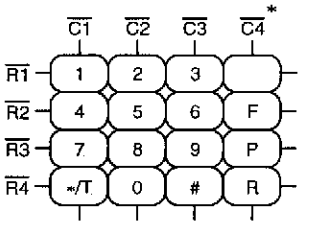
HT9202S
– 20 DIP

Keyboard Information

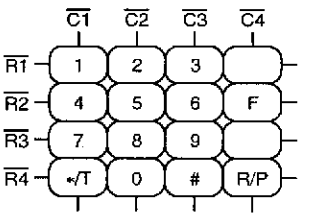
HT9202A/B/C/D/S



HT9202F/G/L



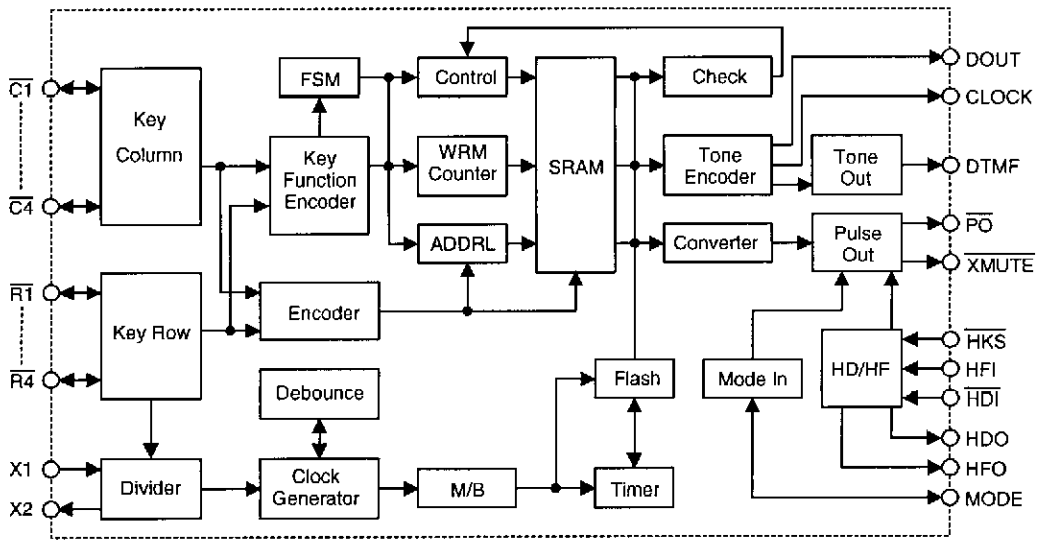
HT9202H



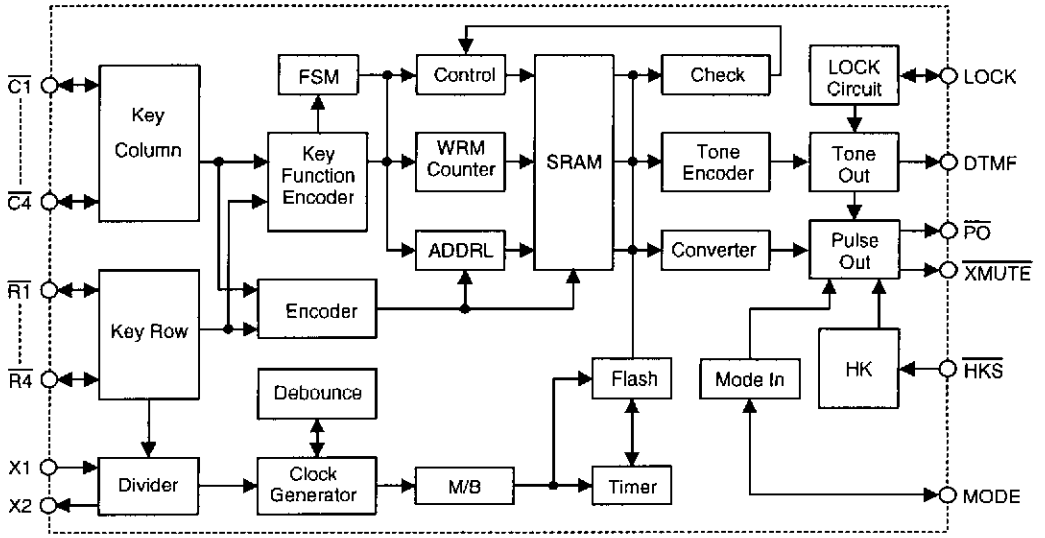
Note: HT9202F/L: $\overline{C4}^{*}=\overline{C4}$
HT9202G: $\overline{C4}=\overline{HKS}$

Block Diagram

HT9202A/B/C/D/S



HT9202F/G/H/L



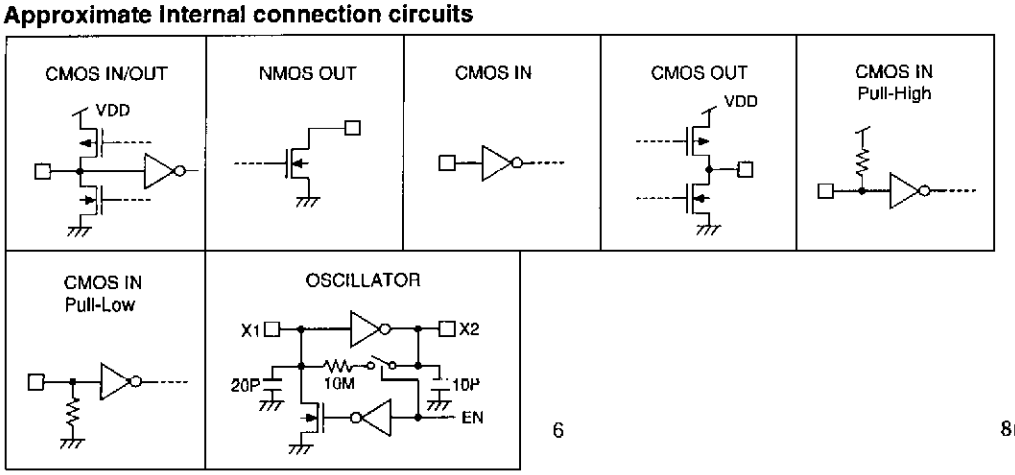
Pin Description

Pin Name	I/O	Internal Connection	Description
$\overline{C1}$~$\overline{C4}$ $\overline{R1}$~$\overline{R4}$	I/O	CMOS IN/OUT	These pins construct a 4×4 keyboard matrix to perform the keyboard input detecting and dialing specification setting functions. When on-hook ($\overline{HKS}$=high) all the pins are set to high. While off-hook the column group ($\overline{C1}$~$\overline{C4}$) stays low and the row group ($\overline{R1}$~$\overline{R4}$) is set to high for key input detecting. An inexpensive single contact 4×4 keyboard can be used as an input device. Pressing a key connects a single column to a single row, and actuates the system oscillator to result in a dialing signal output. If more than two keys are pressed at the same time, no response can be brought about. The key-in debounce time is 20ms. Refer to the keyboard table for keyboard arrangement and to the functional description for dialing specification selection.
X1	I	OSCILLATOR	The system oscillator consists of an inverter, a bias resistor and the necessary load capacitor on chip. Connecting a standard 3.579545MHz crystal or ceramic resonator to X1 and X2 terminals can implement the oscillator function. The oscillator is turned off in the stand-by mode, and is actuated whenever a keyboard entry is detected.
X2	O		
$\overline{XMUTE}$	O	NMOS OUT	The $\overline{XMUTE}$ is an NMOS open drain structure pulled to VSS during dialing signal transmitting. Otherwise, it is an open circuit. The $\overline{XMUTE}$ is used to mute the speech circuit when transmitting the dial signal.

Pin Name	I/O	Internal Connection	Description
$\overline{HKS}$	I	CMOS IN	This pin is used to monitor the status of the hook-switch and its combination with HFI can control the $\overline{PO}$ pin output to make or break the line. $\overline{HKS}$=VDD: On-hook state ($\overline{PO}$=low). Except HFI/$\overline{HDI}$ (hand-free/hold-line control input), other functions are all disabled. $\overline{HKS}$=VSS: Off-hook state ($\overline{PO}$=high). The chip is in the stand-by mode and ready to receive the key input.
$\overline{PO}$	O	CMOS OUT	This pin is a CMOS output structure which receives $\overline{HKS}$ and HFO signals to control the dialer so as to connect or disconnect the telephone line. $\overline{PO}$ outputs low to break line when $\overline{HKS}$ is high (on-hook) and HFO is low (hand-free inactive). $\overline{PO}$ outputs high to make line when $\overline{HKS}$ is low (off-hook) or HFO is high or HDO is high. During the off-hook state, the pin also outputs the dialing pulse train in pulse mode dialing. While in the tone mode, this pin is always high.
MODE	I/O	CMOS IN/OUT	This is a three-state input/output pin, provided to the user for selecting a dialing mode among Tone/20pps/10pps. MODE=VDD: Pulse mode, 10pps. MODE=OPEN: Pulse mode, 20pps. MODE=VSS: Tone mode. During the pulse mode dialing, switching this pin to the tone mode changes the following entrance of digits to the tone mode. When the chips are working in the tone mode, the switching from tone to the pulse mode will be recognized.
DTMF	O	CMOS OUT	This pin is active only when the chip transmits tone dialing signals. Otherwise, it always outputs low. The pin outputs tone signals to drive the external transmitter amplifier circuit. The load resistor should not be less than 5KΩ.
$\overline{HDI}$	I	CMOS IN Pull-High	This pin is a schmitt trigger input structure. Active low. Applying a negative going pulse to this pin can toggle the HDO output once. An external RC network is recommanded to use for the input debouncing. The pull-high resistance is 200KΩ typically.
HDO	O	CMOS OUT	The HDO is a CMOS output structure. Its output is toggle-controlled by a negative transition on $\overline{HDI}$. When HDO is toggled to high, $\overline{PO}$ keeps high to hold the line. The hold function can be released by setting HFO high or by an on-off hook operation or by another $\overline{HDI}$ input. The HDO pin can directly drive the HT3810 series melody generator to produce hold-line back ground melody. Refer to the functional description for the hold-line function.

Pin Name	I/O	Internal Connection	Description
HFI	I	CMOS IN Pull-Low	This pin is a schmitt trigger input structure. Active high. Applying a positive going pulse to HFI can toggle the HFO once and hence control the hand-free function. The pull-low resistance of HFI is 200KΩ typically. An external RC network is recommanded to use for the input debouncing.
HFO	O	CMOS OUT	The HFO is a CMOS output structure. Its output is toggle-controlled by a positive transition on HFI pin. When HFO is high, the hand-free function is enabled and $\overline{PO}$ outputs high to connect the line. The hand-free function can be released by setting HDO high or by an on-off-hook operation or by another HFI input. Refer to the functional description for the hand-free functional operation.
LOCK	I/O	CMOS IN/OUT	This is a three-state input/output pin, provided to the user for controlling the long distance call function with a lock-switch. LOCK=VDD: Normal dialing. LOCK=OPEN: "0, 9" is inhibited for use as the first key input. LOCK=VSS: "0" is inhibited for use as the first key input.
DOUT	O	NMOS OUT	This is an NMOS open drain output pin. It outputs the BCD code of the dialing digits to the LCD driver chip (HT16XX series) or μC for dialing number display. Refer to the functional description for the detailed timing.
CLOCK	O	NMOS OUT	NMOS open drain output. When dialing, it outputs a series of pulse trains for the DOUT data synchronization. The DOUT data is valid at the falling edge of clock.
VDD	I	—	Positive power supply, 2.0V~5.5V for normal operation.
VSS	I	—	Negative power supply

Approximate Internal connection circuits



Absolute Maximum Ratings

Supply Voltage ..... −0.3V to 6V
Storage Temperature ..... −50°C to 125°C
Input Voltage ..... V_{SS}−0.3 to V_{DD}+0.3V
Operating Temperature ..... −20°C to 75°C

Electrical Characteristics

(F_{OSC}=3.5795MHz, Ta=25°C)

Symbol	Parameter	Test Condition			Min.	Typ.	Max.	Unit
		V_{DD}	Condition					
V_{DD}	Operating Voltage	—	—		2	—	5.5	V
I_{DD}	Operating Current	2.5V	Pulse	Off-hook Keypad entry No load	—	0.2	1	mA
			Tone		—	0.6	2	mA
I_{STB}	Stand-by Current	1V	On-hook, no load No entry		—	—	1	μA
V_R	Memory Retention Voltage	—	—		1	—	5.5	V
I_R	Memory Retention Current	1V	On-hook		—	0.1	0.2	μA
V_{IL}	Input Low Voltage	—	—		V_{SS}	—	$0.2V_{DD}$	V
V_{IH}	Input High Voltage	—	—		$0.8V_{DD}$	—	V_{DD}	V
I_{XMO}	$\overline{\text{XMUTE}}$ Leakage Current	—	$V_{\overline{XMUTE}}$=12V No entry		—	—	1	μA
I_{OLXM}	$\overline{\text{XMUTE}}$ Sink Current	2.5V	$V_{\overline{XMUTE}}$=0.5V		1	—	—	mA
$I_{\overline{HKS}}$	$\overline{\text{HKS}}$ Pin Input Current	2.5V	$V_{\overline{HKS}}$=2.5V		—	—	0.1	μA
R_{HFI}	HFI Pull-Low Resistance	2.5V	V_{HFI}=2.5V		—	200	—	KΩ
$R_{\overline{HDI}}$	$\overline{\text{HDI}}$ Pull-High Resistance	2.5V	$V_{\overline{HDI}}$=0V		—	200	—	KΩ
I_{OH1}	Keypad Pin Source Current	2.5V	V_{OH}=0V		−4	—	−40	μA
I_{OL1}	Keypad Pin Sink Current	2.5V	V_{OL}=2.5V		200	400	—	μA
I_{OH2}	HFO Pin Source Current	2.5V	V_{OH}=2V		−1	—	—	mA
I_{OL2}	HFO Pin Sink Current	2.5V	V_{OL}=0.5V		1	—	—	mA
I_{OH3}	HDO Pin Source Current	2.5V	V_{OH}=2V		−1	—	—	mA
I_{OL3}	HDO Pin Sink Current	2.5V	V_{OL}=0.5V		1	—	—	mA
T_{FP}	Pause Time After Flash	—	Control key		—	0.2	—	s
			Digit key		—	1	—	
T_{RP}	One-key Redialing Pause Time	—	One-key redialing		—	1	—	s
T_{DB}	Key-in Debounce Time	—	—		—	20	—	ms
T_{BRK}	Break Time for One-key Redialing	—	One-key redialing		—	2	—	s
F_{OSC}	System Frequency	—	Crystal=3.5795MHz		3.5759	3.5795	3.5831	MHz

Pulse Mode Electrical Characteristics

(F_{OSC}=3.5795MHz, Ta=25°C)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
I_{POH}	$\overline{PO}$ Output Source Current	2.5V	V_{OH}=2V	-0.2	—	—	mA
I_{POL}	$\overline{PO}$ Output Sink Current	2.5V	V_{OL}=0.5V	0.2	0.6	—	mA
PR	Pulse Rate	—	MODE pin is connected to V_{DD}.	—	10	—	pps
			MODE pin is opened.	—	20	—	
M/B	Make/Break Ratio	—	A resistor is linked between $\overline{R2}$ and $\overline{C1}$.	—	33:66	—	%
			No resistor is linked between $\overline{R2}$ and $\overline{C1}$.	—	40:60	—	
T_{PDP}	Pre-digit-pause Time	—	M/B ratio=40:60	—	40 (10pps) 20 (20pps)	—	ms
			M/B ratio=33:66	—	33 (10pps) 17 (20pps)	—	
T_{IDP}	Inter-digit-pause Time	—	Pulse rate=10pps	—	800	—	ms
			Pulse rate=20pps	—	500	—	
T_M	Pulse Make Duration	—	A resistor is linked between $\overline{R2}$ and $\overline{C1}$.	—	33 (10pps) 17 (20pps)	—	ms
			No resistor is linked between $\overline{R2}$ and $\overline{C1}$.	—	40 (10pps) 20 (20pps)	—	
T_B	Pulse Break Duration	—	A resistor is linked between $\overline{R2}$ and $\overline{C1}$.	—	66 (10pps) 33 (20pps)	—	ms
			No resistor is linked between $\overline{R2}$ and $\overline{C1}$.	—	60 (10pps) 30 (20pps)	—	

Tone Mode Electrical Characteristics

(F_{OSC}=3.5795MHz, Ta=25°C)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
V_{TDC}	DTMF Output DC Level	—	—	0.45V_{DD}	—	0.7V_{DD}	V
I_{TOL}	DTMF Sink Current	2.5V	V_{DTMF}=0.5V	0.1	—	—	mA
V_{TAC}	DTMF Output AC Level	—	Row group, R_L=5KΩ	0.12	0.155	0.18	Vr.m.s

Symbol	Parameter	Test Condition			Min.	Typ.	Max.	Unit
		V_{DD}	Condition					
R_L	DTMF Output Load	2.5V	THD≤–23dB		5	—	—	KΩ
A_{CR}	Column Pre-emphasis	2.5V	Row group=0dB		1	2	3	dB
THD	Tone Signal Distortion	2.5V	R_L=5KΩ		—	–30	–23	dB
T_{TMIN}	Minimum Tone Duration	—	Auto-redial	HT9202A/B/C/D/F/H/L/S	—	82.5	—	ms
				HT9202G	—	100	—	ms
T_{ITPM}	Minimum Inter-tone Pause	—	Auto-redial	HT9202A/B/C/D/F/H/L/S	—	85.5	—	ms
				HT9202G	—	106	—	ms

THD (Distortion) (dB) = $20 \log (\sqrt{V1^2 + V2^2 + ... + Vn^2} / \sqrt{Vi^2 + Vh^2})$

Vi, Vh: Row group and column group signals

V1, V2, ... Vn: Harmonic signals (BW=300Hz~3500Hz)

Functional Description

Keyboard matrix

The $\overline{C1}$~$\overline{C4}$ and $\overline{R1}$~$\overline{R4}$ make up of a keyboard matrix. Together with a standard 4×4 keyboard, the keyboard matrix is used for dialing entrance. In addition, the keyboard matrix provides resistor option for different dialing specification selections. The keyboard arrangement for each of the HT9202 series are listed in **Keyboard Information**.

Tone frequency

Tone Name	Output Frequency (Hz)		% Error
	Specified	Actual	
$\overline{R1}$	697	699	+0.29%
$\overline{R2}$	770	766	–0.52%
$\overline{R3}$	852	847	–0.59%
$\overline{R4}$	941	948	+0.74%
$\overline{C1}$	1209	1215	+0.50%
$\overline{C2}$	1336	1332	–0.30%
$\overline{C3}$	1477	1472	–0.34%

% Error does not contain the crystal frequency drift.