HI-8050/51, HI-8150/51

January 2001

CMOS HIGH VOLTAGE DISPLAY DRIVER

GENERAL DESCRIPTION

The HI-8050, HI-8051, HI-8150 and HI-8151 are CMOS integrated circuits designed for high voltage LCD display drive applications. The HI-8050 & HI-8051 have TTL logic inputs whereas the HI-8150 & HI-8151 have CMOS logic inputs. They drive up to 38 segments at voltages between +5 and -30 volts. The optional negative converter on the HI-8050 & HI-8150 can be used to generate the negative display drive voltage. All products have test inputs to facilitate opens and shorts testing as well as automatic blanking of the display if the +5V power is lost.

The HI-8050 and HI-8150 are designed to replace the HI-8010 and HI-8020 devices in all 5 volt applications. They offer significantly enhanced ESD protection along with a considerably faster serial input data rate.

The data is serially clocked into the device on the negative edge of the clock and latched in parallel to the segment outputs on the high to low transition of the load input. Serial output data changes on the positive edge of the clock allowing the cascading ofmultiple drivers for larger displays.

The device layout supports all previous pinouts of the HI-8010/HI-8020 products. In addition, new technology and features afford new packaging options. Consult your Holt Sales Representative to explore the possibilities.

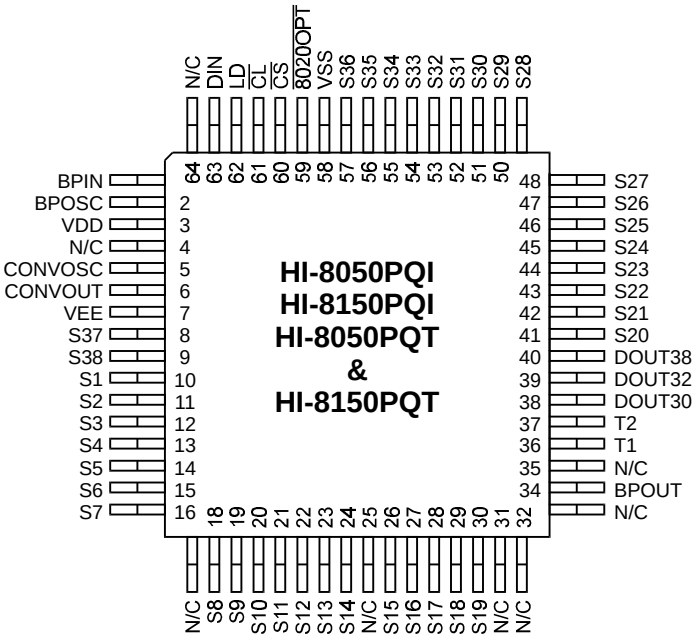
FEATURES

- 4 MHz serial input data rate
- 38 segment outputs
- Cascadable
- 5 Volt inputs translated to 35 Volts
- Test pins allow hardware all "ON", all "OFF" or alternating
- Monitors 5 volt supply and forces all segments to "OFF" condition if lost
- Negative voltage converter available on-chip
- CMOS low power
- Military processing available

APPLICATIONS

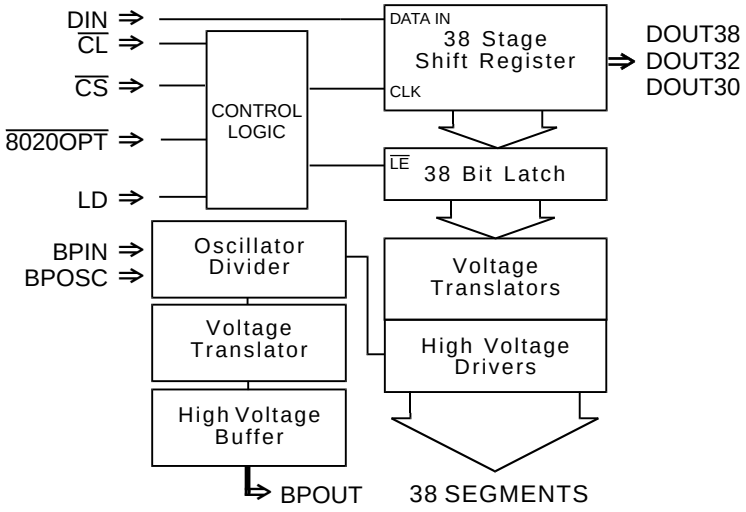
- Dichroic Liquid Crystal Displays
- Standard Liquid Crystal Displays
- 5 Volt Serial Data to Parallel High Voltage

PAD CONFIGURATION (Top View)



(See page 3-32A for HI-8051 & HI-8151 pin configurations)

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION TABLE

SIGNAL	FUNCTION	DESCRIPTION
VSS	POWER	0 Volts
$\overline{8020OPT}$	LOGIC INPUT	Open or high logic level selects the HI-8010/HI-8110 $\overline{CL}$ / $\overline{CS}$ logic. A low selects the HI-8020/HI-8120 Logic (HI-8050 & HI-8150 only)
$\overline{CS}$	LOGIC INPUT	Chip select - Active low
$\overline{CL}$	LOGIC INPUT	Serial data input clock - Active low
LD	LOGIC INPUT	Latches data in shift register to the segment outputs - Active high
DIN	LOGIC INPUT	Serial input data to the shift register
BPIN	INPUT	Backplane frequency input. Either driven from an external source or connected to BPOSC and an external resistor and capacitor.
BPOSC	OUTPUT	Internal oscillator pin. Connected to BPIN and an external resistor and capacitor
VDD	POWER	+5V ±5%, Positive voltage of the backplane and segments
CONVOSC	INPUT	Used in conjunction with CONVOUT to generate the negative VEE voltage on-chip (HI-8050 & HI-8150 only).
CONVOUT	OUTPUT	Used in conjunction with CONVOSC to generate the negative VEE voltage on-chip (HI-8050 & HI-8150 only).
VEE	POWER	Negative voltage of the backplane and segments - between VSS and VDD- 35V
S1 to S38	OUTPUT	Segment outputs to LCD display
BPOUT	OUTPUT	Backplane output to LCD display (See Figure 3 for cascading drivers)
T1	LOGIC INPUT	Used in conjunction with T2 to control display mode. Normal mode is logic low.
T2	LOGIC INPUT	Used in conjunction with T1 to control display mode. Normal mode is logic low.
DOUT30	OUTPUT	Logic output from the 30th bit of the shift register. Use for pattern verification or as the DIN of the next cascaded driver (HI-8050 & HI-8150 only).
DOUT32	OUTPUT	Logic output from the 32nd bit of the shift register. Use for pattern verification or as the DIN of the next cascaded driver (HI-8050 & HI-8150 only).
DOUT38	OUTPUT	Logic output from the 38th bit of the shift register. Use for pattern verification or as the DIN of the next cascaded driver.

FUNCTIONAL DESCRIPTION

INPUT LOGIC

The data is clocked into a serial shift register from the DIN input on the negative edge of $\overline{CL}$ while $\overline{CS}$ is held low. LD is normally held low and pulsed high only when data from the shift register is parallel latched to the segment outputs. $\overline{CS}$ must be low when LD is pulsed. The latches are transparent while LD is high. A logic "1" in the shift register causes the corresponding segment output to be out of phase with the BP output. All four logic inputs are TTL compatible on the HI-8050/51and CMOS compatible on the HI-8150/51.

BPOSC and BPIN

The user has the option of creating the backplane frequency internally or providing a signal from an external source. For an internal oscillator, BPIN and BPOSC are connected together and the appropriate R & C combination is applied as shown in Figure 1. The resulting backplane frequency is approximately:

$$f_{BP} = \frac{1}{256\ RC} \quad . \quad (R = 220K\Omega,\ C = 220pF,\ f_{BP} \approx 100HZ)$$

The value of the resistor must be greater than 30KΩ.

Alternatively, BPOSC is left open and an external backplane signal of the desired frequency is applied to the BPIN input.

VEE & NEGATIVE VOLTAGE CONVERTER

VEE can be connected to a negative power supply. Alternatively, the HI-8050 & HI-8150 have the option of generating the VEE voltage with a built-in -25 volt negative voltage converter (See Figure 2). When not used, the open CONVOSC pin is detected and all power consuming circuitry is disabled. The converter will survive a short between two segments and stillmaintain a VEE voltage of -20V.

DOUT

The DOUT30, DOUT32, and DOUT38 pins are available for cascading devices to drive more segments (See Figure 3) and for verifying the integrity of the shift register data. The outputs can drive 2 TTL loads. They change on the positive edge of $\overline{CL}$.

AUTOMATIC SEGMENTS OFF

A threshold device detects when the 5V supply is below approximately 1V and forces all the segments and the backplane to the same level. This feature is used to discharge the VEE capacitor when the 5V power is switched off, to prolong the life of the LCD display.

$\overline{8020OPT}$

The $\overline{CL}$ and $\overline{CS}$ inputs function the same as the HI-8010 and HI-8110 product (See Figure 5) if this pin is left open or held high. If held low, the two pins function the same as the HI-8020 and HI-8120 product (See Figure 6). This input is available only on the HI-8050 (TTL) and HI-8150 (CMOS) products.

TEST INPUTS

The test functions available are:

T2	T1	Display Mode
0	0	Normal
0	1	All Off
1	0	All On
1	1	Alternating On/Off Segments

The test inputs must be tied to the appropriate logic level for correct circuit operation. Both test inputs are TTL compatible on the HI-8050/51 and CMOS compatible on the HI-8150/51.

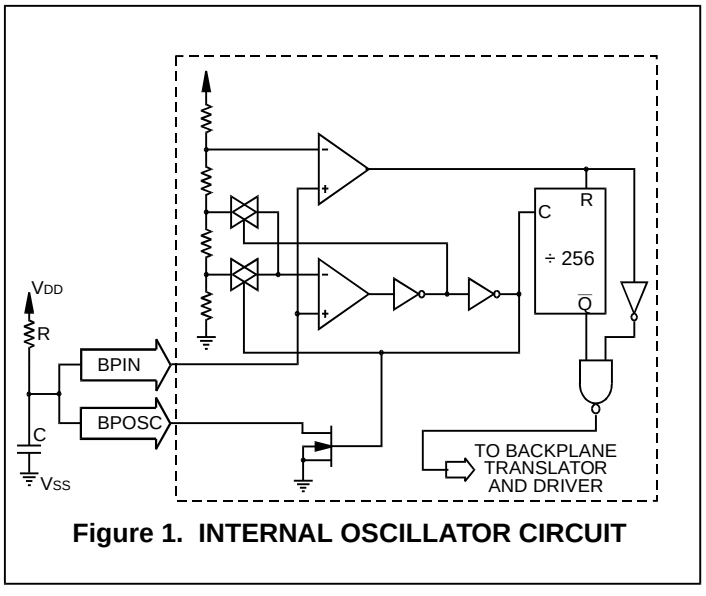


Figure 1. INTERNAL OSCILLATOR CIRCUIT

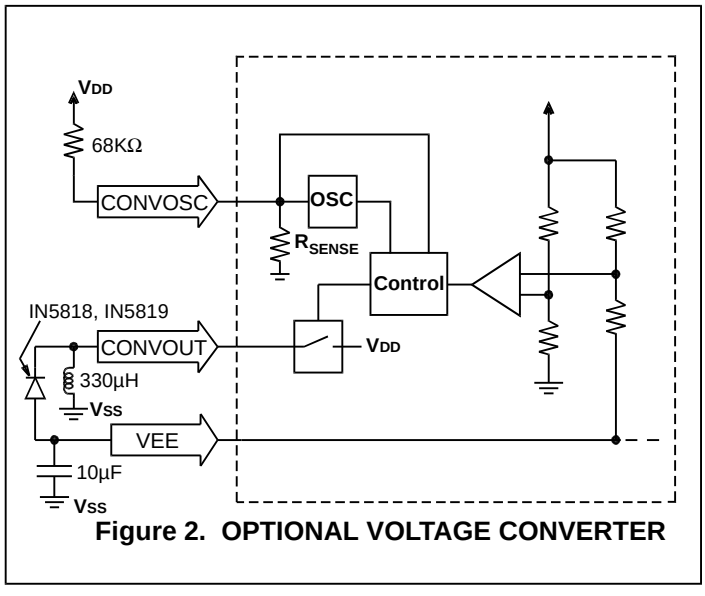


Figure 2. OPTIONAL VOLTAGE CONVERTER

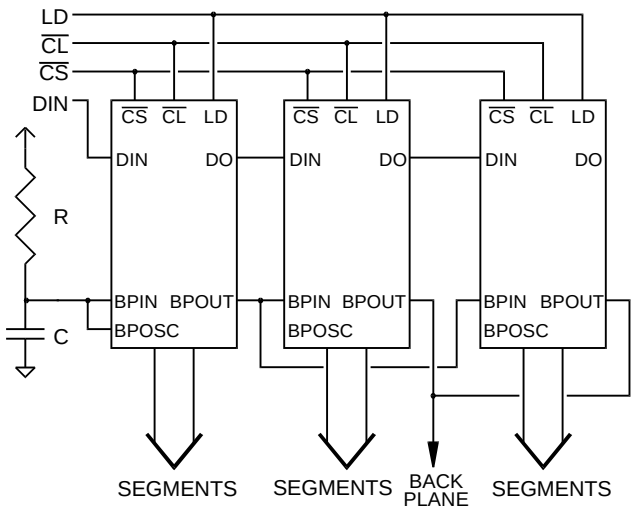


Figure 3. RC OSCILLATOR AND CASCADED DEVICES

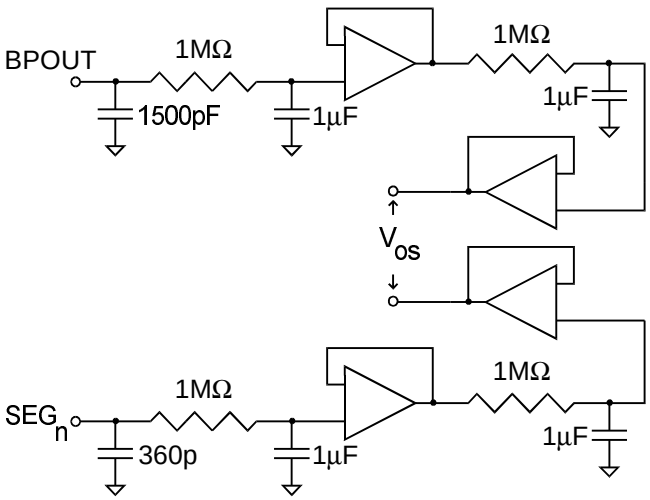


Figure 4. OFFSET MEASUREMENT

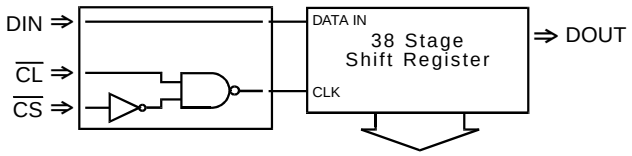


Figure 5. HI-8010/HI-8110 $\overline{CL}$ & $\overline{CS}$ LOGIC ($\overline{8020OPT}$ = OPEN or HIGH)

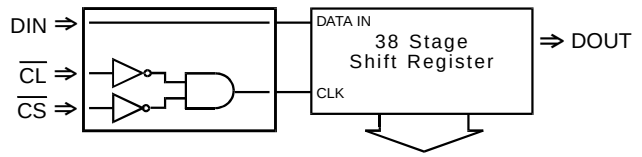


Figure 6. HI-8020/HI-8120 $\overline{CL}$ & $\overline{CS}$ LOGIC ($\overline{8020OPT}$ = LOW)

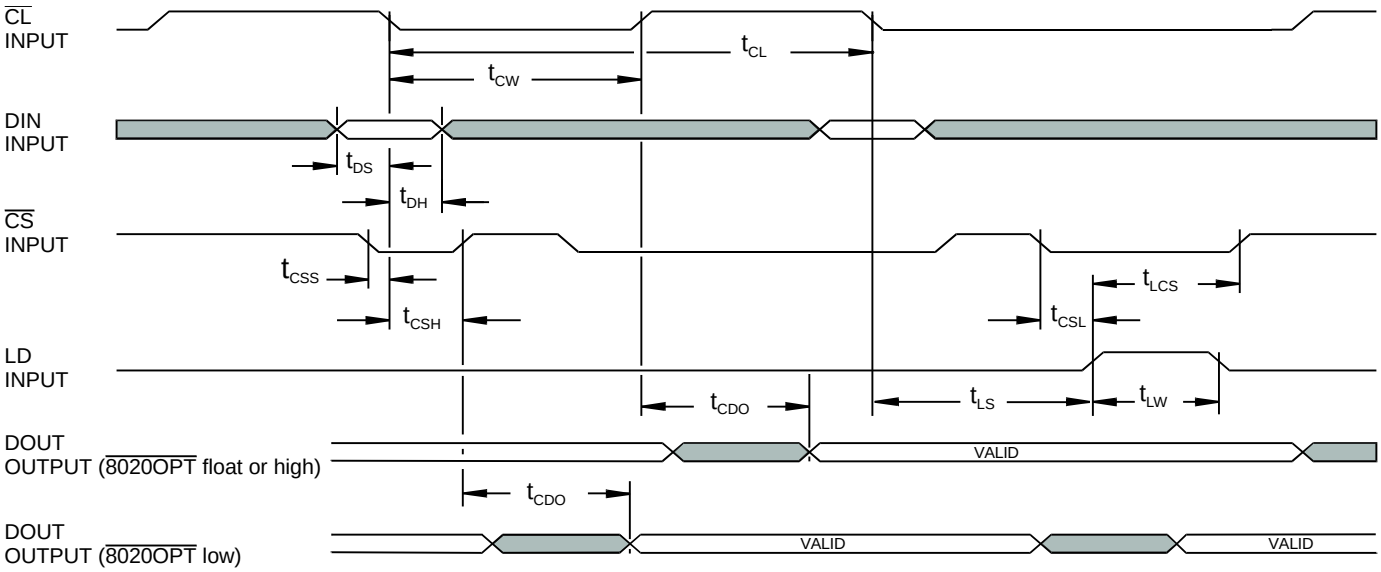


Figure 7. TIMING DIAGRAM

ABSOLUTE MAXIMUM RATINGS

Voltages referenced to VSS = 0V

Supply Voltage VDD .....0V to 7V VEE.....VDD-35V to 0V	Operating Temperature Range(Industrial) ..... -40°C to +85°C (Hi-Temp/Mil) ..... -55°C to +125°C
Voltage at any input, except BPIN..-0.3V to VDD+0.3V	Storage Temperature ..... -65°C to +125°C
Voltage at BPIN input .....VDD-35V to VDD+0.3V	Solder Temperature (Leads) ..... +280°C for 10 sec. (Package) ..... +220°C
DC current per input pin .....10 mA	
Power Dissipation.....500 mW	Junction Temperature, Tj .. .. ≤+175°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

VDD = 5V ±5%, VEE = -25V, VSS = 0V, TA = operating temperature range (unless otherwise specified).

PARAMETER		SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Operating Voltage		VDD		3.0		7.0	V
Supply Current: (Converter Off, f_{BP} = 0Hz)		IDD	Static, No Load			200	µA
		IEE	Static, No Load			120	µA
Input Low Voltage, HI-8050/51 only (except BPIN)		VIL_{TTL}	Logic Inputs	0		0.8	V
Input High Voltage, HI-8050/51 only (except BPIN)		VIH_{TTL}	Logic Inputs	2		VDD	V
Input Low Voltage, HI-8150/51 only (except BPIN)		VIL_{CMOS}	Logic Inputs	0		0.3 VDD	V
Input High Voltage, HI-8150/51 only (except BPIN)		VIH_{CMOS}	Logic Inputs	0.7 VDD		VDD	V
Input Low Voltage, BPIN		VILX		VEE		0.6 VDD	V
Input High Voltage, BPIN		VIHX		0.8 VDD		VDD	V
Input Current (except T1 & T2)		IIN_1	VIN = 0V to 5V			100	nA
Input Current (T1 & T2)		IIN_2	VIN = 0V to 5V	10			µA
Input Capacitance (Guaranteed, not tested)		CI				10	pF
Segment Output Impedance		RSEG	IL = 10µA		10	15	KΩ
Backplane Output Impedance		RBP	IL = 10µA @ 25°C		450	600	Ω
Data Out Current:	Source Current	IDOH	VOH = 4.5			-3.0	mA
	Sink Current	IDOL	VOL = 0.4	3.2			mA
Voltage Converter:	@ No Load	VEE_c	See Fig. 2	-22	-21.5	-21	V
(VDD - VSS = 5V, TA = 25°C)	@ 0.1mA Load	IDD	See Fig. 2			1.8	mA
	@ 10KΩ Load	VEE_c	See Fig. 2	-20			V
Offset Voltage (Guaranteed, not tested)		VOS	See Fig. 4			25	mV

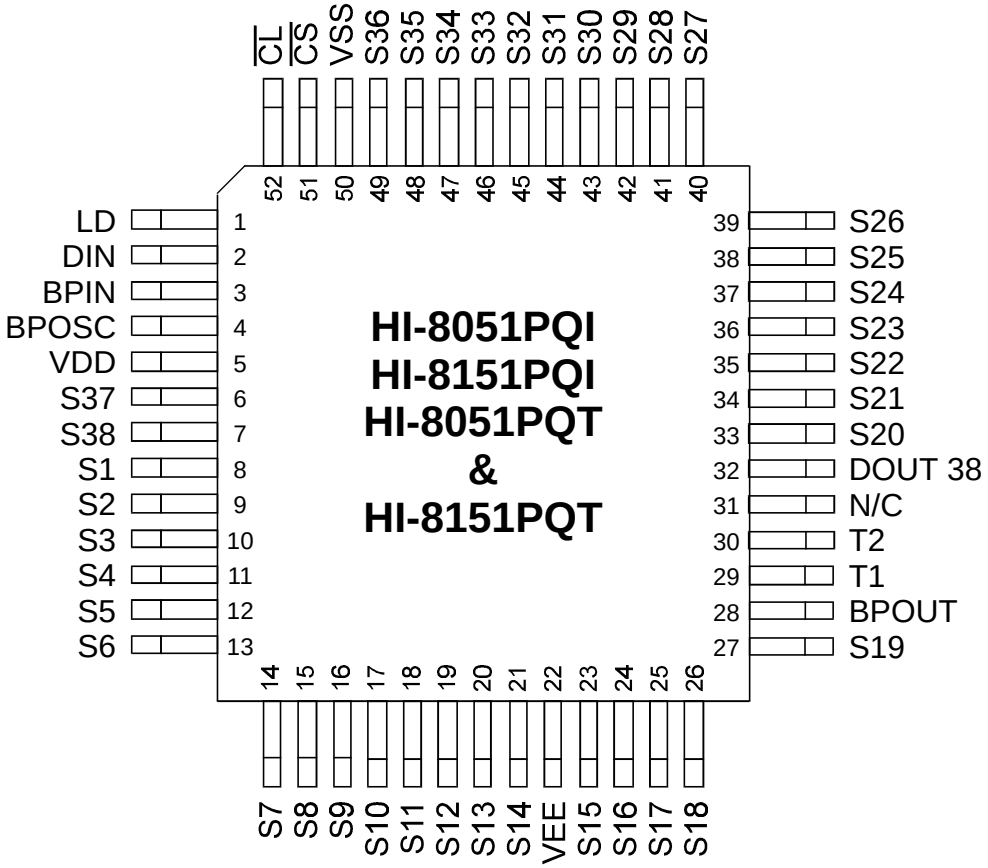
AC ELECTRICAL CHARACTERISTICS (See Figure 7)

VDD = 5V ±5% , VEE = -25V, VSS = 0V, TA = operating temperature range (unless otherwise specified).

PARAMETER		SYMBOL	VDD	MIN	TYP	MAX	UNITS
Clock Period	non-cascaded	t_{CL}	5V	250			ns
	cascaded	t_{CL}	5V	500			ns
Clock Pulse Width	non-cascaded	t_{CW}	5V	125			ns
	cascaded	t_{CW}	5V	250			ns
Data In - Setup		t_{DS}	5V	80			ns
Data In - Hold		t_{DH}	5V	80			ns
Chip Select - Setup to Clock		t_{CSS}	5V	100			ns
Chip Select - Hold to Clock		t_{CSH}	5V	120			ns
Load - Setup to Clock		t_{LS}	5V	120			ns
Chip Select - Setup to Load		t_{CSL}	5V	0			ns
Load Pulse Width		t_{LW}	5V	130			ns
Chip Select - Hold to Load		t_{LCS}	5V	120			ns
Data Out Valid, from Clock		t_{CDO}	5V			170	ns

HI-8051 & HI-8151 PIN CONFIGURATIONS

(See page 3-27 for the HI-8050 & HI-8150 pin configurations)



ORDERING INFORMATION

HI-805xPQx

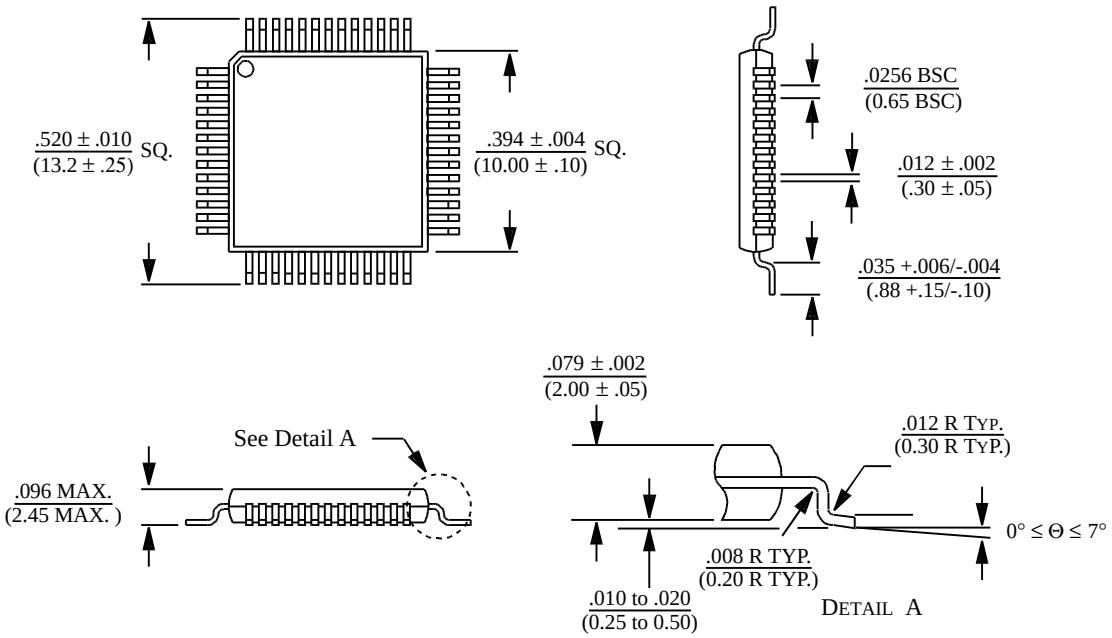
PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN	LEAD FINISH
I	-40°C TO + 85°C	I	NO	SOLDER
T	-55°C TO +125°C	T	NO	SOLDER

PART NUMBER	PACKAGE DESCRIPTION
0	64 PIN PLASTIC THIN FLAT QUAD PACK (TQFP)
1	52 PIN PLASTIC QUAD FLAT PACK (PQFP)

PART NUMBER	LOGIC INPUT LEVELS	# SEGMENTS
HI-805	TTL	38
HI-815	CMOS	38

52 PIN PLASTIC QUAD FLAT PACK (PQFP)

Package Type: 52PQS



64 PIN PLASTIC THIN QUAD FLAT PACK (TQFP)

Package Type: 64PTQS