HEWLETT® PACKARD

100VG-AnyLAN Multimode Fiber Transceivers in Low Cost 1x9 Package Style

Technical Data

HFBR-5106/5106T
1300 nm
HFBR-5107/5107T
820 nm

Features

- **Full Compliance with the Optical Performance Requirements of the IEEE 802.12**
- **Multisourced 1x9 Package Style with Choice of Duplex SC or ST® Receptacles**
- **Wave Solder and Aqueous Wash Process Compatible**
- **Manufactured in an ISO 9002 Certified Facility**
- **820 nm and 1300 nm LED Based Transceivers**

Applications

- **Multimode Fiber Backbone Links**
- **Multimode Fiber Wiring Closet to Desktop Links**

Description

The HFBR-5106 and HFBR-5107 series transceivers from Hewlett-Packard provide system designers with products to implement a range of multimode fiber 100VG-AnyLAN physical layer solutions. The transceivers are all supplied in the new industry standard 1x9 SIP package style with a choice of duplex SC or ST® connector interface.

100VG-AnyLAN Backbone Links

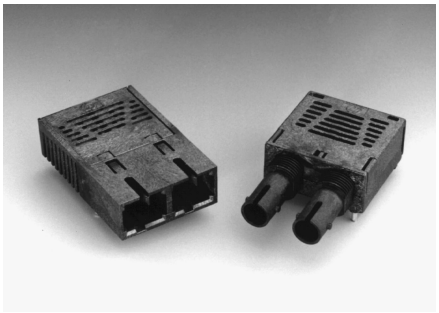
The HFBR-5106/-5106T are 1300 nm products with optical performance compliant with the 100VG-AnyLAN PMD developed by IEEE 802.12. These transceivers are suitable for link lengths up to 2 km.

Alternative 800 nm, Lower Cost 500 m Desktop Links

The HFBR-5107 is a lower cost 800 nm alternative to the HFBR-5106 for 100VG-AnyLAN links from the wiring closet to the desktop. It complies with the performance requirements of 802.12 as implemented by Hewlett-Packard at 800 nm wavelength. This transceiver will transfer the full range of 100VG-AnyLan Signals at the required $1x10^{-8}$ Bit Error Rate over distances up to 500 meters using 62.5/125 µm multimode fiber cables. This product is intended for use in cost sensitive applications where the benefits of fiber optic links are important.

Transmitter Sections

The transmitter sections of the HFBR-5106 utilize 1300 nm



Surface Emitting InGaAsP LEDs and the HFBR-5107 uses a low cost 820 nm AlGaAs LED. These LEDs are packaged in the optical subassembly portion of the transmitter section. They are driven by a custom silicon IC which converts differential PECL logic signals, ECL referenced (shifted) to a +5 Volt supply, into an analog LED drive current.

Receiver Sections

The receiver section of the HFBR-5106 utilizes InGaAs PIN photodiodes coupled to a custom silicon transimpedance preamplifier IC. The HFBR-5107 series uses the same preamplifier IC in conjunction with an inexpensive silicon PIN photodiode. These are packaged in the optical subassembly portion of the receiver.

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These PlN/preamplifier combinations are coupled to a custom quantizer IC which provides the final pulse shaping for the logic output and Signal Detect function. The data output is differential. The signal detect output is single-ended. Both data and signal detect outputs are PECL compatible, ECL referenced (shifted) to a +5 Volt power supply.

Package

The overall package concept for the HP transceivers consists of the following basic elements; two optical subassemblies, an electrical subassembly, and the housing with integral duplex SC connector receptacles. This is illustrated in Figure 1.

The package outline and pinout are shown in Figures 2 and 3. The details of this package outline and pinout are compliant with the multisource definition of the 1x9 SIP. The low profile of the Hewlett- Packard transceiver design complies with the maximum height allowed for the duplex SC connector over the entire length of the package.

The optical subassemblies utilize a high volume process together with low cost lens elements which result in a cost effective transceiver.

The electrical subassembly consists of a high volume multi-layer printed circuit board on which the IC chips and various surface mount passive circuit elements are attached.

The package includes internal shields for the electrical and optical subassemblies to ensure low EMI and high immunity to electromagnetic fields.

The outer housing, including the duplex SC connector receptacle, is molded of filled non-conductive plastic to provide mechanical strength and electrical isolation. The solder posts of the Hewlett-Packard design are isolated from the circuit design of the transceiver and do not require connection to a ground plane on the circuit board.

The transceiver is attached to a printed circuit board with the nine signal pins and the two solder posts which exit the bottom of the housing. The two solder posts provide the primary mechanical strength to withstand the loads imposed on the duplex or simplex SC connectored fiber cables.

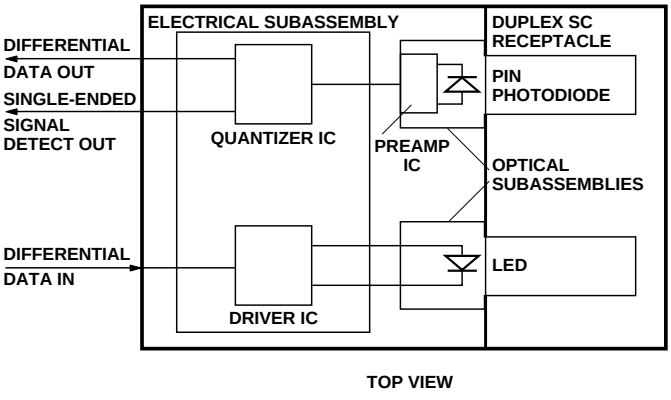


Figure 1. Block Diagram.

Application Information

The Application Engineering group in the Hewlett-Packard Optical Communications Division is available to assist you with the technical understanding and design trade-offs associated with these transceivers. You can contact them through your Hewlett-Packard sales representative.

The following information is provided to answer some of the most common questions about the use of these parts.

Transceiver Optical Power

Budget versus Link Length

Optical Power Budget (OPB) is the available optical power for a fiber optic link to accommodate fiber cable losses plus losses due to inline connectors, splices, optical switches, and to provide margin for link aging and unplanned losses due to cable plant reconfiguration or repair.

Figure 4 illustrates the predicted OPB associated with the two transceivers specified in this data sheet at the Beginning of Life (BOL). These curves represent the attenuation and chromatic plus modal dispersion losses associated with the 62.5/125 µm and 50/125 µm fiber cables only. The area under the curve represents the remaining OPB at any link length, which is available for overcoming non-fiber cable related losses.

Hewlett-Packard LED technology has produced 800 nm LED and 1300 nm LED devices with lower aging characteristics than

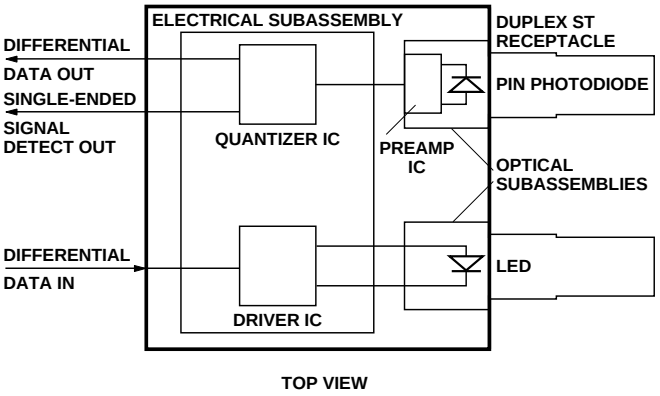
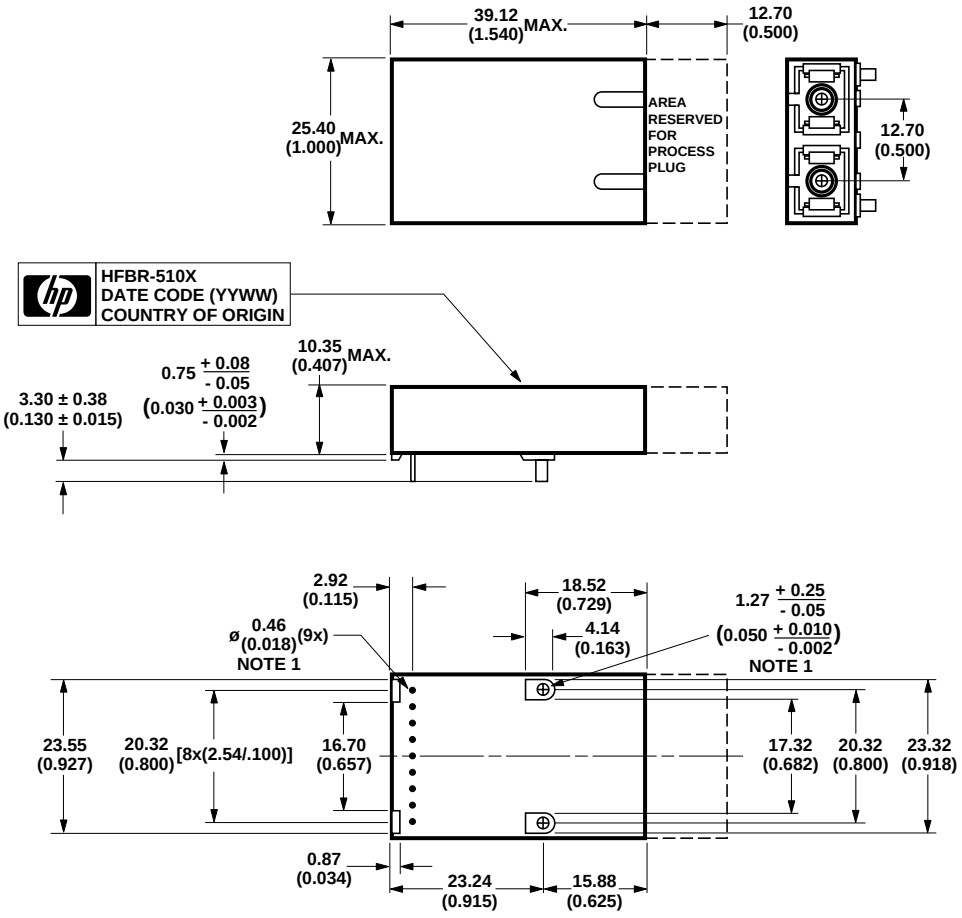


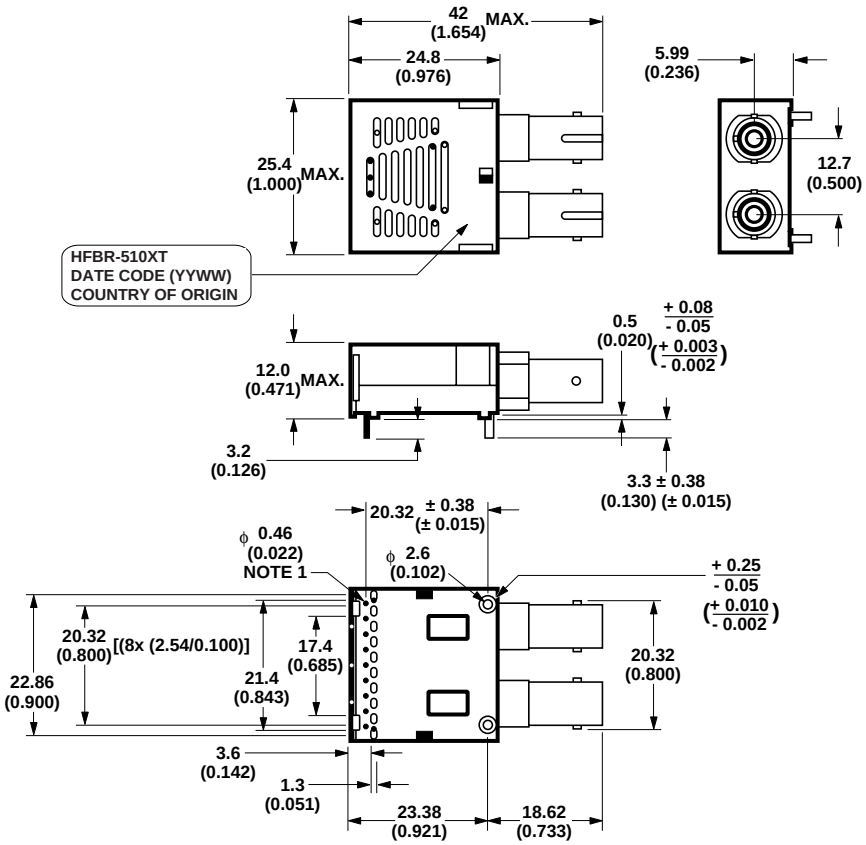
Figure 1a. ST Block Diagram.



NOTE 1: THE SOLDER POSTS AND ELECTRICAL PINS ARE PHOSPHOR BRONZE WITH TIN LEAD OVER NICKEL PLATING.

DIMENSIONS ARE IN MILLIMETERS (INCHES).

Figure 2. Package Outline Drawing.



NOTE 1: PHOSPHOR BRONZE IS THE BASE MATERIAL FOR THE POSTS & PINS WITH TIN LEAD OVER NICKEL PLATING.

DIMENSIONS IN MILLIMETERS (INCHES).

Figure 2a. ST Package Outline Drawing.

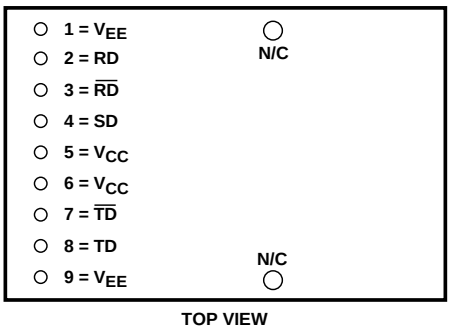


Figure 3. Pin Out Diagram.

normally associated with these technologies in the industry. The Industry convention is 3 dB aging for 800 nm and 1.5 dB for 1300 nm LEDs. The HP LEDs will normally experience less than 1 dB of aging over normal commercial equipment mission life periods. Contact your Hewlett-Packard sales representatives for additional details.

Figure 4 was generated with a Hewlett-Packard fiber optic link module containing the current industry conventions for fiber cable specifications and the 100VG-AnyLAN Optical Parameters. These parameters are reflected in the guaranteed performance of the transceiver specifications in this data sheet. This same model has been used extensively in the ANSI X3T and IEEE committees, including the ANSI X3T12 committee, to establish the optical performance requirements for various fiber optic interface standards. The cable parameters used come from the ISO/IEC JTCI/SC 25/WG3 Generic Cabling for Customer Premises per DIS 11801 document and the EIA/TIA568-A Commercial Building Telecommunications Cabling Standard per SP-2840.

Transceiver Signaling Operating Rate Range and BER Performance

For purposes of definition, the symbol (Baud) rate, also called signaling rate, is the reciprocal of the shortest symbol time. Data rate (bits/sec) is the symbol rate divided by the encoding factor used to encode the data (symbols/bit).

When used in 100VG AnyLAN 100 Mbps applications, the performance of the 1300 nm transceiver is guaranteed over the signaling rate of 10 MBd to 120 MBd to the full conditions listed in the individual product specification tables.

The transceivers may be used for other applications at signaling rates outside of the 10 MBd to 120 MBd range with some penalty in the link optical power budget primarily caused by a reduction of receiver sensitivity. Figure 5 gives an indication of the typical performance of these 1300 nm products at different rates.

These transceivers can also be used for applications which require different Bit Error Rate (BER) performance. Figure 6 illustrates the typical trade-off between link BER and the receivers input optical power level.

Table 1 lists the hub control signals defined in IEEE 802.12, section 18.5.4.1. These signal rates are below 10 MBd but they are transported with adequate accuracy for hub access control.

Transceiver Jitter Performance

The Hewlett-Packard 1300 nm transceivers are designed to operate per the system interface jitter specifications listed in Table 27 of section 18.9. of the IEEE 802.12 (100VG-AnyLAN standards).

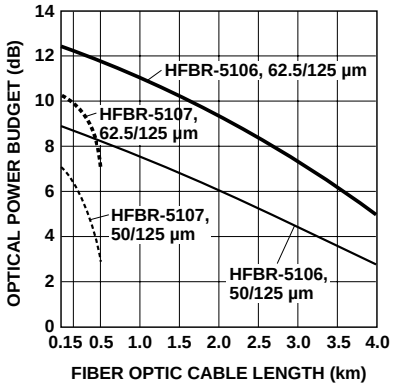
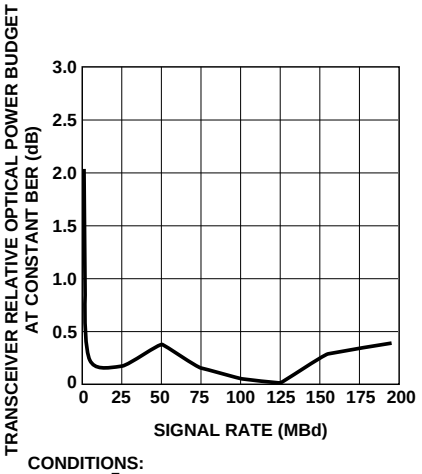
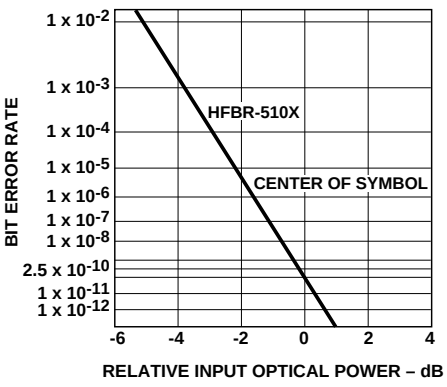


Figure 4. Optical Power Budget at BOL vs. Fiber Optic Cable Length.



CONDITIONS:
1. PRBS 2^7-1
2. DATA SAMPLED AT CENTER OF DATA SYMBOL.
3. BER = 10^{-6}
4. T_A = 25° C
5. V_{CC} = 5 V_{dc}
6. INPUT OPTICAL RISE/FALL TIMES = 1.0/2.1 ns.

Figure 5. Transceiver Relative Optical Power Budget at Constant BER vs. Signaling Rate.



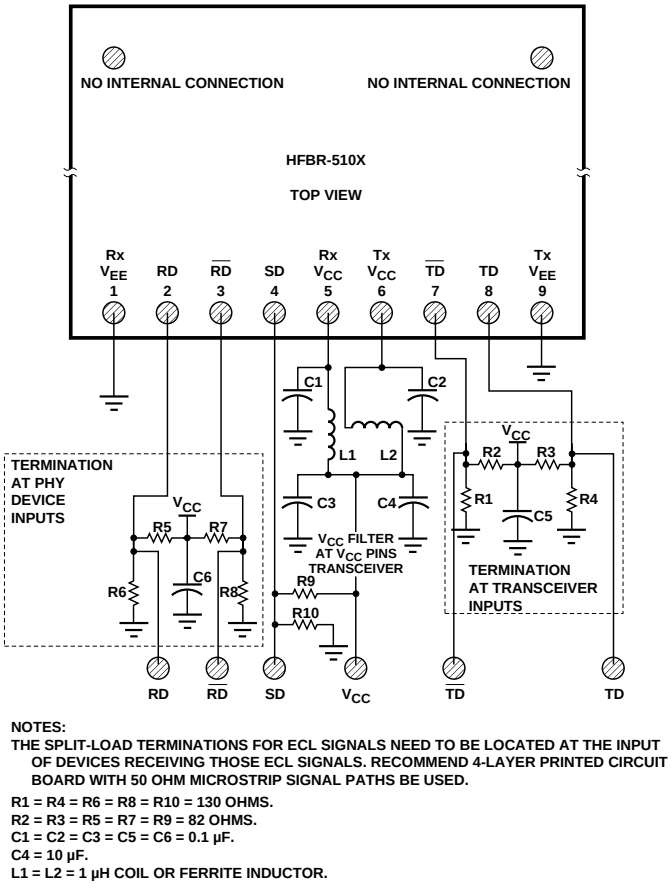
CONDITIONS:
1. 125 MBd
2. PRBS 2^7-1
3. CENTER OF SYMBOL SAMPLING.
4. T_A = 25° C
5. V_{CC} = 5 V_{dc}
6. INPUT OPTICAL RISE/FALL TIMES = 1.0/2.1 ns.

Figure 6. Bit Error Rate vs. Relative Receiver Input Optical Power.

The HP 1300 nm transmitters are allowed to generate the worst case Active Output jitter shown in Table 27 of section 18.9 when driven by circuits optimized for these link applications. The Active Output Specifications of the 100VG-AnyLAN standard are met by the HFBR-5106.

The HP 1300 nm receivers tolerate the worst case input optical response time and systematic jitter shown in Table 27 of Section 18.9. The Active Input Specification of the IEEE 802.12 100VG-AnyLAN standard are met by the HBFR-5106.

The jitter specifications stated in the 1300 nm transceiver specification tables are derived from the values in Table 27 of section 18.9 of the IEEE 802.12 specification. They represent the worst case jitter contributions from the transceiver meeting the overall system jitter in Annex E. In practice the typical jitter contribution of the HP transceivers is well below these maximum allowed values.



NOTES:
THE SPLIT-LOAD TERMINATIONS FOR ECL SIGNALS NEED TO BE LOCATED AT THE INPUT OF DEVICES RECEIVING THOSE ECL SIGNALS. RECOMMEND 4-LAYER PRINTED CIRCUIT BOARD WITH 50 OHM MICROSTRIP SIGNAL PATHS BE USED.
R1 = R4 = R6 = R8 = R10 = 130 OHMS.
R2 = R3 = R5 = R7 = R9 = 82 OHMS.
C1 = C2 = C3 = C5 = C6 = 0.1 µF.
C4 = 10 µF.
L1 = L2 = 1 µH COIL OR FERRITE INDUCTOR.

Figure 7. Recommended Decoupling and Termination Circuits.

Recommended Handling Precautions

It is advised that normal static precautions be taken in the handling and assembly of these transceivers to prevent damage which may be induced by electrostatic discharge (ESD). The HFBR-510X series of transceivers are certified as Mil-Std-883C Method 3015.4 Class 1 products.

Care should be used to avoid shorting the receiver data or signal detect outputs directly to ground without proper current limiting impedance.

Solder and Wash Process Compatibility

The transceivers are delivered with a protective process plug inserted into the duplex SC connector receptacle. This process plug protects the optical subassemblies during wave solder and aqueous wash processing and acts as a dust cover during shipping. These transceivers are compatible with either industry standard wave or hand soldering processes.

Shipping Container

The transceiver is packaged in a shipping container designed to protect it from mechanical and ESD damage during shipment or storage.

Board Layout – Decoupling Circuit and Ground Planes

It is important to take care in the layout of your circuit board to achieve optimum performance from these transceivers. Figure 7 provides a good example of a schematic for a power supply decoupling circuit that works

Regulatory Compliance Table

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883C Method 3015.4	Certified to Class 1 (0 to 1999 Volts) Withstand up to 1800 V applied between electrical pins.
Electrostatic Discharge (ESD) to the Duplex SC Receptacle	Variation of IEC 801-2	Typically withstand at least 25 kV without damage when the Duplex SC Connector Receptacle is contacted by a Human Body Model probe.
Electromagnetic Interference (EMC)	FCC Class B CENELEC CEN55022 Class B (CISPR 22B) VCCI Class 2	Typically provide a 10 dB margin to the noted standard limits when tested at a certified test range with the transceiver mounted to a circuit card without a chassis enclosure.
Immunity	Variation of IEC 801-3	Typically show no measurable effect from a 10 V/m field swept from 10 to 450 MHz applied to the transceiver when mounted to a circuit card without a chassis enclosure.

well. It is further recommended that a contiguous ground plane be provided in the circuit board directly under the transceiver to provide a low inductance ground for signal return current. This recommendation is in keeping with good high frequency board layout practices.

Board Layout – Hole Pattern

This Hewlett-Packard transceiver complies with the circuit board "Common Transceiver Footprint" hole pattern defined in the original multisource announcement which defined the 1x9 package style. This drawing is reproduced in Figure 8 with the addition of ANSI Y14.5N compliant dimensioning to be used as a guide in the mechanical layout of your circuit board.

Board Layout – Art Work

The Applications Engineering group has developed Gerber file artwork for a multilayered printed circuit board layout incorporating the above recommendations. Contact your local Hewlett-Packard sales representative for details.

Board Layout – Mechanical

For applications providing a choice of either a duplex SC or a duplex ST connector interface, while utilizing the same pinout on the printed circuit board, the ST port needs to protrude from the chassis panel a minimum of 9.53 mm for sufficient clearance to install the ST connector.

Please refer to Figure 8a for a mechanical layout detailing the recommended location of the duplex SC and duplex ST transceiver packages in relation to the chassis panel.

Regulatory Compliance

These transceiver products are intended to enable commercial system designers to develop equipment that complies with the various international regulations governing certification of Information Technology Equipment. See the Regulatory Compliance Table for details. Additional information is available from your Hewlett-Packard sales representative.

Electrostatic Discharge (ESD)

There are two design cases in which immunity to ESD damage is important.

The first case is during handling of the transceiver prior to mounting it on the circuit board. It is important to use normal ESD handling precautions for ESD sensitive devices. These precautions include using grounded wrist straps, work benches, and floor mats in ESD controlled areas.

The second case is static discharges to the exterior of the equipment chassis containing the transceiver parts. To the extent that the duplex SC connector is exposed to the outside of the equipment chassis it may be subject to whatever ESD system level test criteria that the equipment is intended to meet.

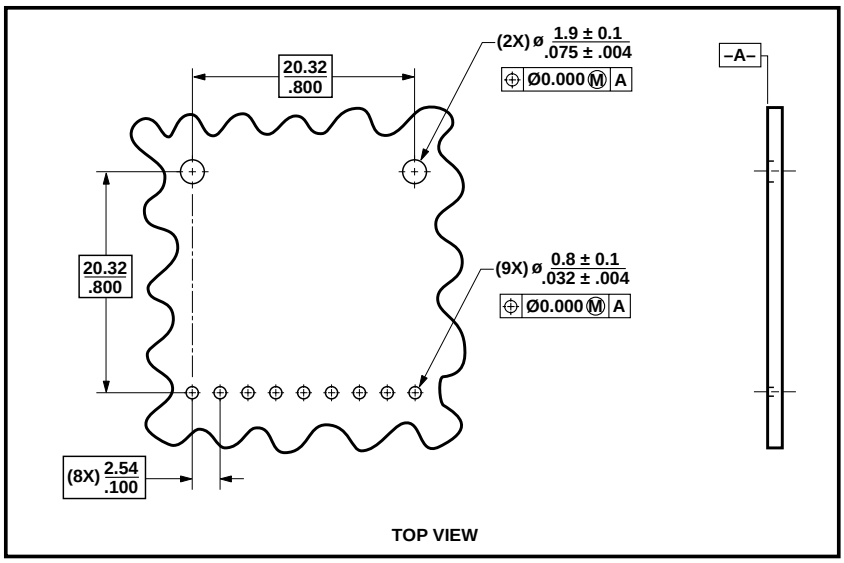


Figure 8. Recommended Board Layout Hole Pattern.

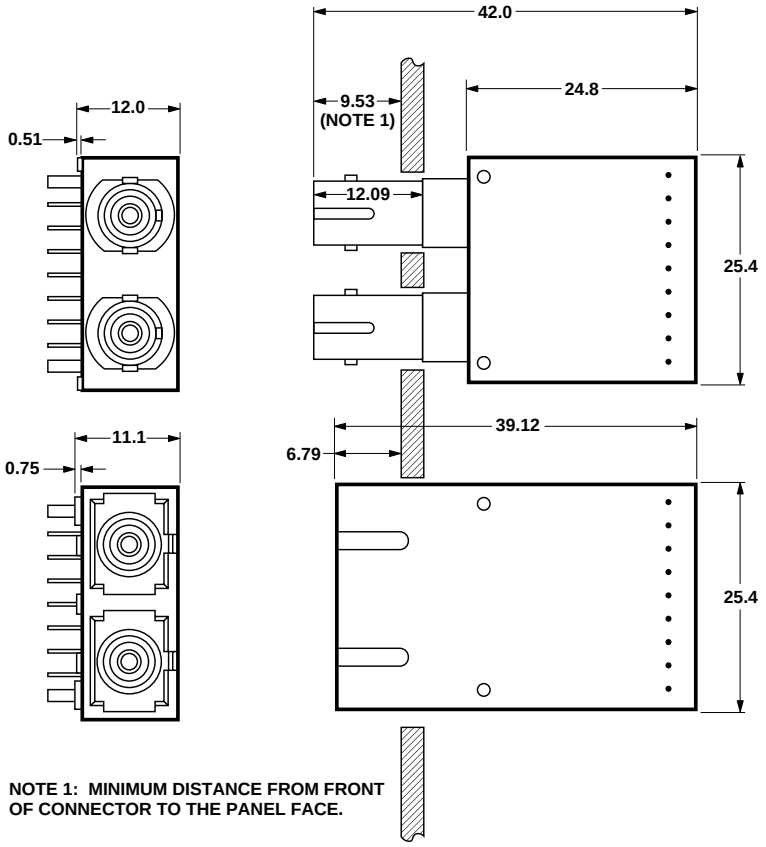


Figure 8a. Recommended Common Mechanical Layout for SC and ST 1x9 Connectored Transceivers.

Electromagnetic Interference (EMI)

Most equipment designs utilizing these high speed transceivers from Hewlett-Packard will be required to meet the requirements of FCC in the United States, CENELEC EN55022 (CISPR 22) in Europe and VCCI in Japan.

These devices are suitable for use in designs ranging from a desktop computer with a single transceiver to a concentrator or switch product with a large number of transceivers.

Immunity

Equipment utilizing these transceivers will be subject to radio frequency electromagnetic fields in some environments. These transceivers have a high immunity to such fields.

Transceiver Reliability and Performance Qualification Data

The 1x9 transceivers have passed Hewlett-Packard reliability and performance qualification testing and are undergoing quality monitoring. Details are available from your Hewlett-Packard sales representative. These transceivers are manufactured at the Hewlett-Packard Singapore location which is an ISO 9002 certified facility.

Ordering Information

The HFBR-5106 and HFBR-5106T 1300 nm products and HFBR-5107 and HFBR-5107T 820 nm devices are available for production orders through the Hewlett-Packard Component Field Sales Offices and Authorized Distributors worldwide.

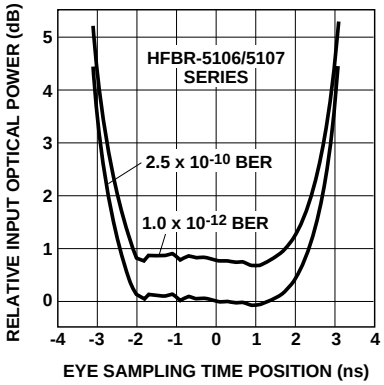
Applications Support Material

Contact your local Hewlett-Packard Component Field Sales Office for information on how to obtain PCB layouts, test boards, and demo boards for the 1x9 transceivers.

Accessory Duplex SC Connectored Cable Assemblies

Hewlett-Packard also offers two compatible Duplex SC connectored jumper cable assemblies to assist you in the evaluation of these transceiver products. These cables may be purchased from HP with the following part numbers. They are available through the Hewlett-Packard Component Field Sales Offices and Authorized Distributors worldwide.

1. HFBR-BKD001 – A duplex cable 1 meter long assembled with 62.5/125 µm fiber and duplex SC connector plugs on either end.
2. HFBR-BKD010 – A duplex cable 10 meters long assembled with 62.5/125 µm fiber and duplex SC connector plugs on either end.



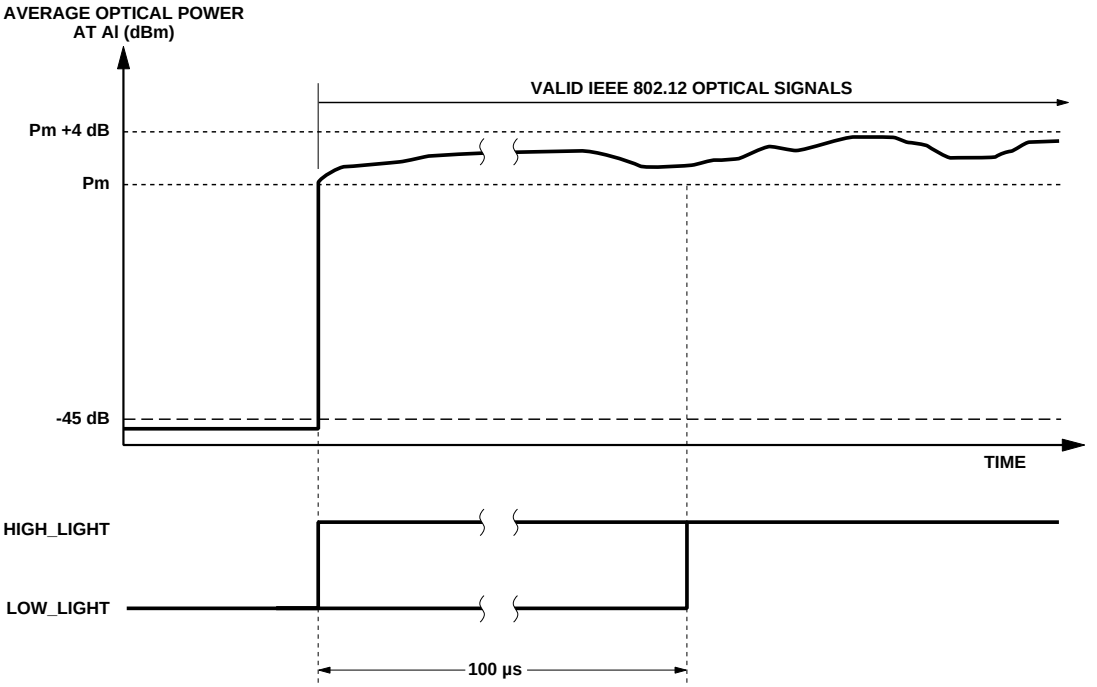
CONDITIONS:
1. T_A = 25° C
2. V_{CC} = 5 Vdc
3. INPUT OPTICAL RISE/FALL TIMES = 1.0/2.1 ns.
4. INPUT OPTICAL POWER IS NORMALIZED TO CENTER OF DATA SYMBOL.
5. NOTE 20 AND 21 APPLY.

Figure 9. Relative Input Optical Power vs. Eye Sampling Time Position.

Table 1. Control Signal Generation

The Hewlett-Packard transceivers are capable of transporting the following five control signals defined in IEEE 802.12, section 18.5.4.1.

Control Signal	NRZ Encoded Pattern	Frequency
Control Signal 1 (CS1)	<HCS1a> and <HCS1b>	1.875 MHz
Control Signal 2 (CS2)	<HCS2a> and <HCS2b>	2.069 MHz
Control Signal 3 (CS3)	<HCS3a> and <HCS3b>	2.308 MHz
Control Signal 4 (CS4)	<HCS4a> and <HCS4b>	2.609 MHz
Control Signal 5 (CS5)	<HCS5a> and <HCS5b>	3.000 MHz


AVERAGE OPTICAL POWER
AT AI (dBm)
VALID IEEE 802.12 OPTICAL SIGNALS
Pm +4 dB
Pm
-45 dB
TIME
HIGH_LIGHT
LOW_LIGHT
100 µs

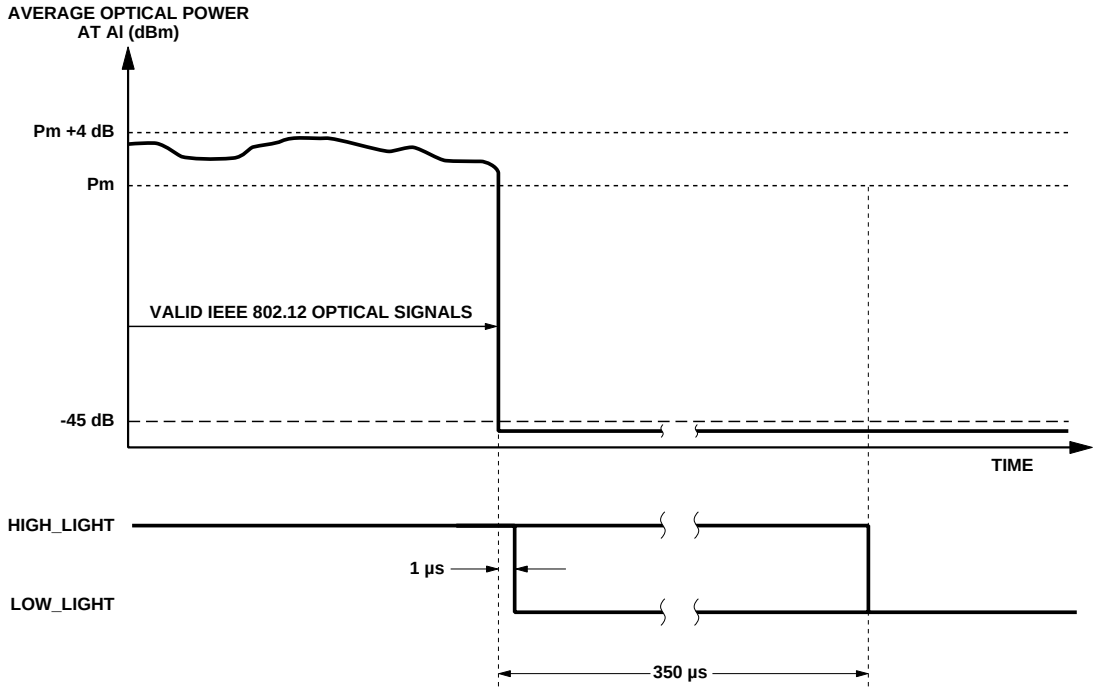

AVERAGE OPTICAL POWER
AT AI (dBm)
Pm +4 dB
Pm
VALID IEEE 802.12 OPTICAL SIGNALS
-45 dB
TIME
HIGH_LIGHT
1 µs
LOW_LIGHT
350 µs

Figure 10.

HFBR-5106, -5107 Series
Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Storage Temperature	T_S	–40		100	°C	
Lead Soldering Temperature	T_{SOLD}			260	°C	
Lead Soldering Time	t_{SOLD}			10	sec.	
Supply Voltage	V_{CC}	–0.5		7.0	V	
Data Input Voltage	V_I	–0.5		V_{CC}	V	
Differential Input Voltage	V_D			1.4	V	Note 1
Output Current	I_O			50	mA	

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Ambient Operating Temperature	T_A	0		70	°C	
Supply Voltage	V_{CC}	4.75		5.25	V	
Data Input Voltage - Low	V_{IL} - V_{CC}	–1.810		–1.475	V	
Data Input Voltage - High	V_{IH} - V_{CC}	–1.165		–0.880	V	
Data and Signal Detect Output Load	R_L		50		Ω	Note 2

Transmitter Electrical Characteristics
(T_A = 0°C to 70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Supply Current	I_{CC}		145	185	mA	Note 3
Power Dissipation	P_{DISS}		0.76	0.97	W	
Data Input Current - Low	I_{IL}	-350	0		µA	
Data Input Current - High	I_{IH}		14	350	µA	

Receiver Electrical Characteristics
(T_A = 0°C to 70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Supply Current	I_{CC}		102	145	mA	Note 4
Power Dissipation	P_{DISS}		0.3	0.5	W	Note 5
Data Output Voltage - Low	V_{OL} - V_{CC}	–1.840		–1.620	V	Note 6
Data Output Voltage - High	V_{OH} - V_{CC}	–1.045		–0.880	V	Note 6
Data Output Rise Time	t_r	0.35		2.2	ns	Note 7
Data Output Fall Time	t_f	0.35		2.2	ns	Note 7
Signal Detect Output Voltage - Low	V_{OL} - V_{CC}	–1.840		–1.620	V	Note 6
Signal Detect Output Voltage - High	V_{OH} - V_{CC}	–1.045		–0.880	V	Note 6
Signal Detect Output Rise Time	t_r	0.35		2.2	ns	Note 7
Signal Detect Output Fall Time	t_f	0.35		2.2	ns	Note 7

HFBR-5106/5106T
Transmitter Optical Characteristics

(T_A = 0°C to 70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Output Optical Power 62.5/125 µm, NA = 0.275 Fiber	P_O	-21.0 BOL		-14	dBm avg.	Note 9
Output Optical Power 50/125 µm, NA = 0.20 Fiber	P_O	-24.8 BOL		-14	dBm avg.	Note 9
Output Optical Power at Logic "0" State	P_O ("0")			-45	dBm avg.	Note 11
Center Wavelength	λ_C	1270		1380	nm	Note 12
Spectral Width - FWHM	$\Delta\lambda$			200	nm	Note 12
Optical Rise Time	t_r			3.0	ns	Note 12, 13
Optical Fall Time	t_f			3.0	ns	Note 12, 13
Systematic Jitter Contributed by the Transmitter	SJ			1.2	ns p-p	Note 23
Random Jitter Contributed by the Transmitter	RJ			0.69	ns p-p	Note 15

HFBR-5106/5106T
Receiver Optical and Electrical Characteristics

(T_A = 0°C to 70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Input Optical Power Minimum at Window Edge	$P_{IN\ Min.}$ (W)			–29	dBm avg.	Note 16 Figure 9
Input Optical Power Minimum at Eye Center	$P_{IN\ Min.}$ (C)		–33.5		dBm avg.	Note 17 Figure 9
Input Optical Power Maximum	$P_{IN\ Max.}$	–14			dBm avg.	Note 16
Operating Wavelength	λ	1270		1380	nm	
Systematic Jitter Contributed by the Receiver	SJ			1.4	ns p-p	Note 23
Random Jitter Contributed by the Receiver	RJ			2.90	ns p-p	Note 24
Signal Detect - Asserted (high_light)	P_A	P_D + 1.5 dB		–31	dBm avg.	Note 18, 19 Figure 10
Signal Detect - Deasserted (lo_light)	P_D	–45			dBm avg.	Note 21, 22 Figure 10
Signal Detect - Hysteresis	$P_A - P_D$	1.5			dB	Figure 10
Signal Detect Assert Time (off to on)	AS_MAX	0		100	µs	Note 8, 19 Figure 10
Signal Detect Deassert Time (off to on)	ANS_MAX	0		350	µs	Note 21, 22 Figure 10
Control Signal Detect	CS1-5	–14		–29	dBm avg.	See Table 1

HFBR-5107/5107T
Transmitter Optical Characteristics

(T_A = 0°C to 70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Output Optical Power 62.5/125 µm, NA = 0.275 Fiber	P_O	–17.0 BOL		–12	dBm avg.	Note 10
Output Optical Power 50/125 µm, NA = 0.20 Fiber	P_O	–20.8 BOL		–12	dBm avg.	Note 10
Output Optical Power at Logic "0" State	P_O ("0")			–45	dBm avg.	Note 11
Center Wavelength	λ_C	800		900	nm	Note 12
Spectral Width - FWHM	$\Delta\lambda$			100	nm	Note 12
Optical Rise Time	t_r			4.5	ns	Note 12, 14
Optical Fall Time	t_f			4.5	ns	Note 12, 14
Systematic Jitter Contributed by the Transmitter	SJ			1.7	ns p-p	Note 23
Random Jitter Contributed by the Transmitter	RJ			0.69	ns p-p	Note 24

HFBR-5107/5107T
Receiver Optical and Electrical Characteristics

(T_A = 0°C to 70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Input Optical Power Minimum at Window Edge	$P_{IN\ Min.}$ (W)			–27.5	dBm avg.	Note 16a
Input Optical Power Minimum at Eye Center	$P_{IN\ Min.}$ (C)		–28		dBm avg.	Note 17a
Input Optical Power Maximum	$P_{IN\ Max.}$	–12			dBm avg.	Note 16a
Operating Wavelength	λ	800		900	nm	
Systematic Jitter Contributed by the Receiver	SJ			1.2	ns p-p	Note 23
Random Jitter Contributed by the Receiver	RJ			2.6	ns p-p	Note 24
Signal Detect - Asserted	P_A	P_D + 1.5 dB		–29.5	dBm avg.	Note 18 Figure 10
Signal Detect - Deasserted	P_D	–45			dBm avg.	Note 21 Figure 10
Signal Detect - Hysteresis	$P_A - P_D$	1.5			dB	Figure 10
Signal Detect Assert Time (off to on)	AS_MAX	0		100	µs	Note 18 Figure 10
Signal Detect Deassert Time (off to on)	ANS_MAX	0		350	µs	Note 21 Figure 10
Control Signal Detect	CS1-5	–14		–27.5	dBm avg.	See Table 1

Notes:

1. This is the maximum voltage that can be applied across the Differential Transmitter Data Inputs to prevent damage to the input ESD protection circuit.
2. The outputs are terminated with 50 Ω connected to V_{CC} –2 V.
3. The power supply current needed to operate the transmitter is supplied to differential ECL circuitry. This circuitry maintains a nearly constant current from the power supply. Constant current operation helps to prevent unwanted electrical noise from being generated and conducted or emitted to neighboring circuitry.
4. This value is measured with the outputs terminated into 50 Ω connected to V_{CC} –2 V and an Input Optical Power Level of –14 dBm average.
5. The power dissipation value is the power dissipated in the receiver itself. Power dissipation is calculated as the sum of the products of supply voltage and currents, minus the sum of the products of the output voltages and currents.
6. This value is measured with respect to V_{CC} with the output terminated into 50 Ω connected to V_{CC} –2 V.
7. The output electrical rise and fall times are measured between 20% and 80% levels with the output connected to V_{CC} –2 V through 50 Ω.
8. Random Jitter contributed by the receiver is specified with a 120 MBd (60 MHz square-wave) input signal. The input optical power level is at maximum "$P_{IN\ MIN}$. (W)".
9. These optical power values are measured with the following conditions:
   - At the Beginning of Life (BOL). The actual FDDI specification is 1.5 dB lower power at the End of Life for the equipment. The definition of Beginning of Life (BOL) to the End of Live (EOL) optical power degradation is assumed to be 1.0 dB per the industry convention for 1300 nm LEDs. The actual degradation observed in normal commercial environments is considerably less than this amount with Hewlett-Packard's 1300 nm LED products.
   - At the end of one meter of noted fiber with cladding modes removed.
   - Over the specified operating voltage and temperature ranges.
   - (12.5 MHz square-wave) input signal. The average power value can be converted to a peak power value by adding 3 dB. Higher output optical power transmitters are available upon special request.
10. The same comments of Note 9 apply except that industry convention for 800 nm LED BOL to EOL aging is 3 dB. This value for Output Optical Power provides a minimum of 7.5 dB optical power budget at the EOL, which provides at least 500 meter link lengths with margin left over for overcoming normal passive losses, such as in-line connectors in the cable plant. The actual degradation observed in normal commercial environments is considerably less than this amount with Hewlett-Packard 800 nm LED products.
11. The transmitter provides compliance with 802.12. An Output Optical Power level of <–45 dBm average in response to a logic "0" input. This specification applies to either 62.5/125 µm or 50/125 µm fiber cables.
12. This parameter complies with 802.12.
13. The optical rise and fall times are measured from 10% to 90% when the transmitter is driven by a 12.5 MHz square-wave input signal.
14. The optical rise and fall times are measured from 10% to 90% when the transmitter is driven by a 12.5 MHz square-wave input signal.
15. Random Jitter contributed by the transmitter is specified with a 60 MBd square-wave input signal.
16. This specification is intended to indicate the performance of the receiver section of the transceiver when Input Optical Power signal characteristics are present per the following definitions. The Input Optical Power dynamic range from the minimum level (with a window time-width) to the maximum level is the range over which the receiver is guaranteed to provide output data with a Bit Error Ratio (BER) better than or equal to 10^{-8}.
    - At the Beginning of Life (BOL).
    - Over the specified operating temperature and voltage ranges.
    - Receiver data window opening time-width is 2.2 ns or greater and centered at mid-symbol. This worst case window opening time-width is the minimum allowed eye-opening presented to the PHY input per 802.12. This minimum window time-width of 2.2 ns is based upon the worst case 802.12 Active Input Interface optical conditions peak-to-peak SJ (1.6 ns) and RJ (0.77 ns) presented to the receiver.
      To test a receiver with the worst case 802.12 Active Input Jitter condition requires exacting control over SJ and RJ jitter components. This is difficult to implement with production test equipment. The receiver can be equivalently tested to the worst case 802.12 input jitter conditions and meet the minimum output data window time-width of 2.2 ns This is accomplished by using a nearly ideal input optical signal (No DCD, insignificant DDJ and RJ) and measuring for a wider window time-width of 4.0 ns. This is possible due to the cumulative addition of jitter components through their superposition. (SJ is directly additive and RJ components are rms additive). Specifically, when a nearly ideal input optical test signal is used and the maximum receiver peak-to-peak jitter contributions of SJ (X.Xns), and RJ (X.Xns) exist, the minimum window time-width becomes 4.4 ns. This wider window time-width of 4.4 ns guarantees the 802.12 time-width of 2.2 ns under worst case input jitter conditions to the Hewlett-Packard receiver.
    - Transmitter operating with a 120 MBd (60 MHz square-wave), input signal to simulate any cross-talk present between the transmitter and receiver sections of the transceiver.

16a. All conditions of Note 16 apply except that the BER requirement is tightened to $1x10^{-8}$ and the minimum window time-width test condition is adjusted to 5.2 ns to reflect the HFBR-5107 transmitter contributed jitter values per the specification table.

17. All conditions of Note 16 apply except that the measurement is made at the center of the symbol with no window time-width.

17a. All conditions of Note 17 apply except that the BER requirement is tightened to $1x10^{-8}$.

18. This value is measured during the transition from low to high levels of input optical power.
19. The high_light (Signal Detect) output shall be asserted within 100 µs after a step increase of the Input Optical Power. The step will be from a low Input Optical Power ≤ –45 dBm, into the range between greater than Pm and (Pm + 4 dB). Pm is the relevant

minimum allowed input average optical power for the PMD at the AI as defined in Figure 10. (The input optical power is averaged over a period of 1 µs or more).

20. The high_light (Signal Detect) output shall be asserted within 100 µs after a step increase of the Input Optical Power. The step will be from a low Input Optical Power ≤ –45 dBm, into the range between greater than Pm and (Pm + 4 dB). Pm is the relevant minimum allowed input average optical power for the PMD at the AI as defined in Figure 10. (The input optical power is averaged over a period of 1 µs or more).
21. This value is measured during the transition from high to low levels of input optical power. The maximum value will occur when the input optical power is –45 dBm average or when the input optical power yields a BER of 10^{-2} or better, whichever power is higher.
22. The low_light (Signal Detect) output shall be deasserted within 350 µs after valid IEEE 802.12 optical signals cease to be present at the AI and the input average optical power at AI has fallen monitonically from a level between (Pm +4 dB) and Pm to a level below –45 dBm and remain below –45 dBm (see Figure 10). (The input optical power is averaged over a period of 1 µs or more.)
22. The low_light (Signal Detect) output shall be deasserted within 350 µs after valid IEEE 802.12 optical signals cease to be present at the AI and the input average optical power at AI, has fallen monitonically from a level between (Pm +4 dB) and Pm to a level below –45 dBm and remain below –45 dBm (see Figure 10). (The input optical power is averaged over a period of 1 µs or more.)
23. Systematic Jitter (SJ) contributed by the 800 and 1300 nm transmitter is a combination of Duty Cycle Distortion (DCD) and Data Dependent Jitter (DDJ).
24. Random Jitter contributed by the 800 and 1300 nm transmitter is specified with an IDLE Line State, 125 MBd (62.5 MHz square-wave), input signal.