Fibre Channel Transceiver Chip

Technical Data

HDMP-1536 Transceiver
HDMP-1546 Transceiver

Features

- **ANSI X3.230-1994 Fibre Channel Compatible (FC-0)**
- **Supports Full Speed (1062.5 MBd) Fibre Channel**
- **Compatible with "Fibre Channel 10-Bit Interface" Specification**
- **Low Power Consumption, 630 mW**
- **Transmitter and Receiver Functions Incorporated onto a Single IC**
- **Auto Frequency Lock**
- **Small Package Profile**
  HDMP-1536, 10x10 mm QFP
  HDMP-1546, 14x14 mm QFP
- **10-Bit Wide Parallel TTL Compatible I/Os**
- **Single +3.3 V Power Supply**

Applications

- **1062.5 MBd Fibre Channel Interface**
- **FC Interface for Disk Drives and Arrays**
- **Mass Storage System I/O Channel**
- **Work Station/Server I/O Channel**
- **High Speed Proprietary Interface**
- **High Speed Backplane Interface**

Description

The HDMP-1536/46 transceiver is a single silicon bipolar integrated circuit packaged in a plastic QFP package. It provides a low-cost, low-power physical layer solution for 1062.5 MBd Fibre Channel or proprietary link interfaces. It provides complete FC-0 functionality for copper transmission, incorporating both the Fibre Channel FC-0 transmit and receive functions into a single device.

This chip is used to build a high-speed interface (as shown in Figure 1) while minimizing board space, power, and cost. It is compatible with both the ANSI X3.230-1994/AM 1 - 1996 document and the "Fibre Channel 10-bit Interface" specification.

The transmitter section accepts 10-bit wide parallel TTL data and multiplexes this data into a high-speed serial data stream. The parallel data is expected to be 8B/10B encoded data, or equivalent. This parallel data is latched into the input register of the transmitter section on the rising edge of the 106.25 MHz reference clock (used as the transmit byte clock).

The transmitter section's PLL locks to this user supplied 106.25 MHz byte clock. This clock is then multiplied by 10, to generate the 1062.5 MHz serial signal clock used to generate the high-speed output. The high-speed outputs are capable of interfacing directly to copper cables for electrical transmission or to a separate fiber-optic module for optical transmission.

The receiver section accepts a serial electrical data stream at 1062.5 MBd and recovers the original 10-bit wide parallel data. The receiver PLL locks onto the incoming serial signal and recovers the high-speed serial clock and data. The serial data is
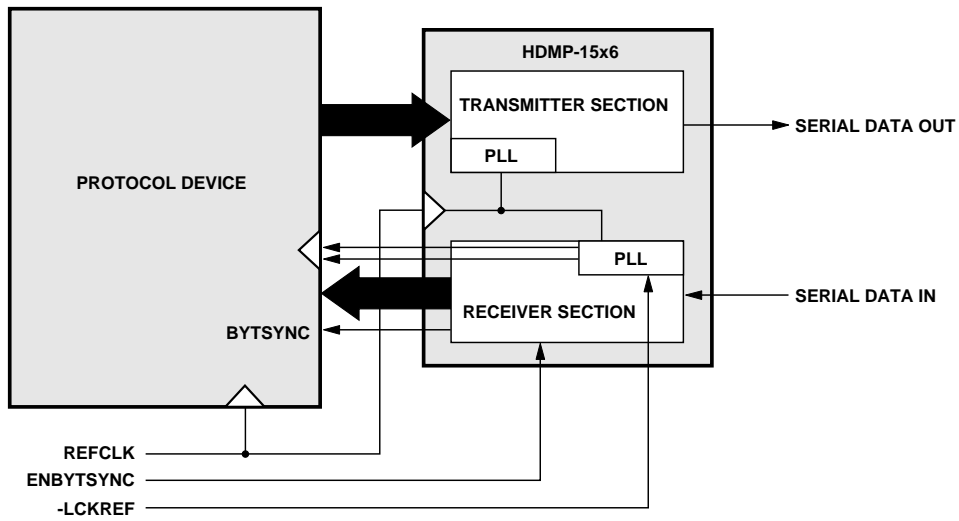
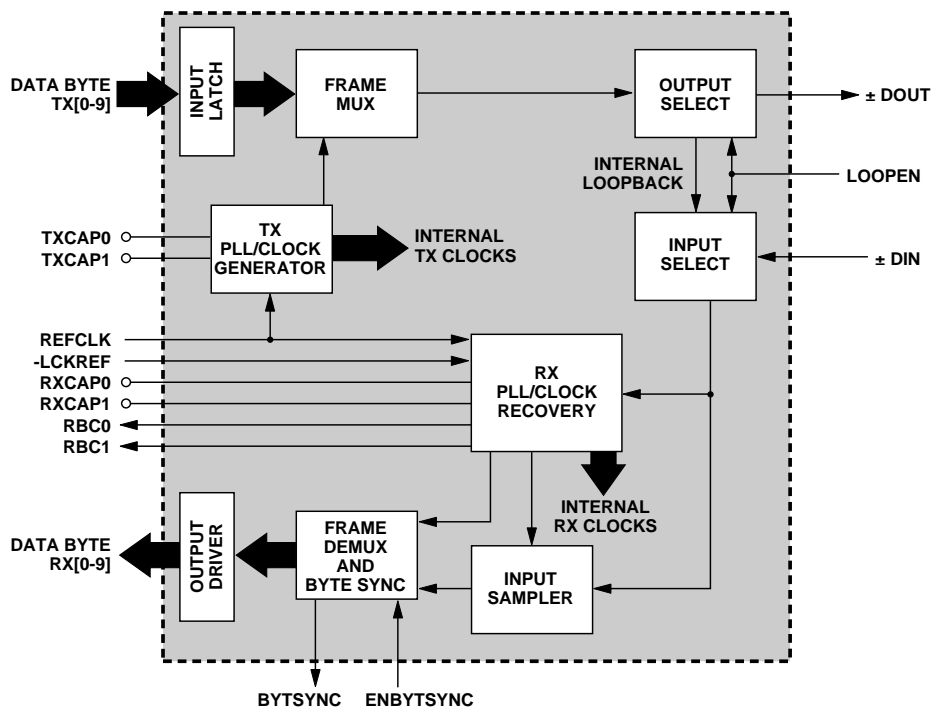Figure 1. Typical Application Using the HDMP-15x6.

Figure 2. HDMP-15x6 Transceiver Block Diagram.

converted back into 10-bit parallel data, recognizing the 8B/10B comma character to establish byte alignment.

The recovered parallel data is presented to the user at TTL compatible outputs. The receiver section also recovers two 53.125 MHz receiver byte clocks that are 180 degrees out of phase with each other. The parallel data is properly aligned with the rising edge of alternating clocks.

The transceiver provides for on-chip local loop-back functionality, controlled through an external input pin. Additionally, the byte synchronization feature may be disabled. This may be useful in proprietary applications which use alternative methods to align the parallel data.

HDMP-1536/46 Block Diagram

The HDMP-1536/46 was designed to transmit and receive 10-bit wide parallel data over a single high-speed line, as specified for the FC-0 layer of the Fibre Channel standard. The parallel data applied to the transmitter is expected to be encoded per the Fibre Channel specification, which uses an 8B/10B encoding scheme with special reserve characters for link management purposes. In order to accomplish this task, the HDMP-1536/46 incorporates the following:

- TTL Parallel I/Os
- High Speed Phase Lock Loops
- Clock Generation/Recovery Circuitry
- Parallel to Serial Converter
- High-Speed Serial Clock and Data Recovery Circuitry
- Comma Character Recognition Circuitry

- Byte Alignment Circuitry
- Serial to Parallel Converter

INPUT LATCH

The transmitter accepts 10-bit wide TTL parallel data at inputs TX[0..9]. The user-provided reference clock signal, REFCLK, is also used as the transmit byte clock. The TX[0..9] and REFCLK signals must be properly aligned, as shown in Figure 3.

TX PLL/CLOCK GENERATOR

The transmitter Phase Lock Loop and Clock Generator (TX PLL/CLOCK GENERATOR) block is responsible for generating all internal clocks needed by the transmitter section to perform its functions. These clocks are based on the supplied reference byte clock (REFCLK). REFCLK is used as both the frequency reference clock for the PLL and the transmit byte clock for the incoming data latches. It is expected to be 106.25 MHz and properly aligned to the incoming parallel data (see Figure 3). This clock is multiplied by 10 to generate the 1062.5 MHz clock necessary for the high speed serial outputs.

FRAME MUX

The FRAME MUX accepts the 10-bit wide parallel data from the INPUT LATCH. Using internally generated high speed clocks, this parallel data is multiplexed into the 1062.5 MBd serial data stream. The data bits are transmitted sequentially, from the least significant bit (TX[0]) to the most significant bit (TX[9]).

OUTPUT SELECT

The OUTPUT SELECT block provides for an optional internal loopback of the high speed serial signal, for testing purposes.

In normal operation, LOOPEN is set low and the serial data stream is placed at ± DOUT. When wrap-mode is activated by setting LOOPEN high, the ± DOUT pins are held static and the serial output signal is internally wrapped to the INPUT SELECT box of the receiver section.

INPUT SELECT

The INPUT SELECT block determines whether the signal at ± DIN or the internal loop-back serial signal is used. In normal operation, LOOPEN is set low and the serial data is accepted at ± DIN. When LOOPEN is set high, the high-speed serial signal is internally looped-back from the transmitter section to the receiver section. This feature allows for loop-back testing exclusive of the transmission medium.

RX PLL/CLOCK RECOVERY

The RX PLL/CLOCK RECOVERY block is responsible for frequency and phase locking onto the incoming serial data stream and recovering the bit and byte clocks. An automatic locking feature allows the Rx PLL to lock onto the input data stream without external controls. It does this by continually frequency locking onto the 106.25 MHz clock, and then phase locking onto the input data stream. An internal signal detection circuit monitors the presence of the input, and invokes the phase detection as the data stream appears. Once bit locked, the receiver generates the high speed sampling clock at 1062.5 MHz for the input sampler, and recovers the two 53.125 MHz receiver byte clocks (RBC1/RBC0). These clocks are 180° out of phase with each other, and are

alternately used to clock the 10-bit parallel output data.

An optional -LCKREF pin is available for users who want to gain full control during the frequency acquisition process. Asserting this pin will force the Rx PLL to fully phase and frequency lock onto the reference clock, disregarding the serial stream completely.

To enable the auto-locking feature, the -LCKREF pin should be tied to V_{CC}. The receiver will detect the absence of high-speed serial data into +DIN (pin 54) and -DIN (pin 52) and lock onto the reference clock (REFCLK). RBC0 and RBC1 will remain frequency locked to 53.125 MHz. The receiver will frequency and phase lock onto the incoming valid data once it is reapplied.

INPUT SAMPLER

The INPUT SAMPLER is responsible for converting the serial input signal into a re-timed serial bit stream. In order to accomplish this, it uses the high speed serial clock recovered from the RX PLL/CLOCK RECOVERY block. This serial bit stream is sent to the FRAME DEMUX and BYTE SYNC block.

FRAME DEMUX AND BYTE SYNC

The FRAME DEMUX AND BYTE SYNC block is responsible for restoring the 10-bit parallel data from the high speed serial bit stream. This block is also responsible for recognizing the comma character (or a K28.5 character) of positive disparity (0011111xxx). When recognized, the FRAME DEMUX AND BYTE SYNC block works with the RX PLL/CLOCK RECOVERY block to properly align the receive byte clocks to the parallel data. When a comma character is detected and realignment of the receiver byte clocks (RBC1/RBC0) is necessary, these clocks are stretched, not slivered, to the next possible correct alignment position. These clocks will be fully aligned by the start of the second 4-byte ordered set. The second comma character received shall be aligned with the rising edge of RBC1. Comma characters should not be transmitted in consecutive bytes to allow the receiver byte clocks to maintain their proper recovered frequencies.

OUTPUT DRIVERS

The OUTPUT DRIVERS present the 10-bit parallel recovered data byte properly aligned to the receiver byte clocks (RBC1/RBC0), as shown in Figure 5. These output data buffers provide TTL compatible signals.

Recommended Handling Precautions

Additional circuitry is built into the various input and output pins on this chip to protect against low level electrostatic discharge; however, they are still ESD sensitive. Standard procedures for static sensitive devices should be used in the handling and assembly of this product.

HDMP-1536/46 (Transmitter Section)

Timing Characteristics

$T_A{}^{[1]} = 0°C$ to $+60°C$, $V_{CC} = 3.15$ V to 3.45 V

Symbol	Parameter	Units	Min.	Typ.	Max.
t_{setup}	Setup Time	nsec	2		
t_{hold}	Hold Time	nsec	1.5		
t_txlat[2]	Transmitter Latency	nsec		7.5	
		bits		8.0	

Notes:

1. Device tested and characterized under T_A conditions specified, with T_C monitored at approximately 20° higher than T_A.

2. The transmitter latency, as shown in Figure 4, is defined as the time between the latching in of the parallel data word (as triggered by the rising edge of the transmit byte clock, REFCLK) and the transmission of the first serial bit of that parallel word (defined by the rising edge of the first bit transmitted).
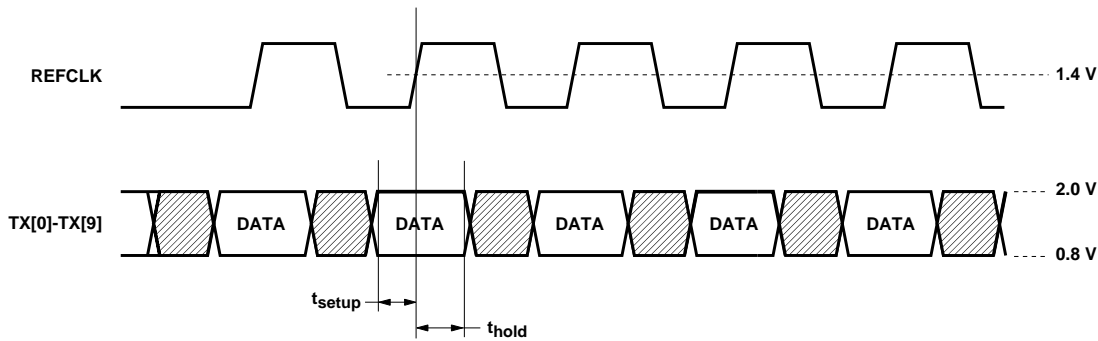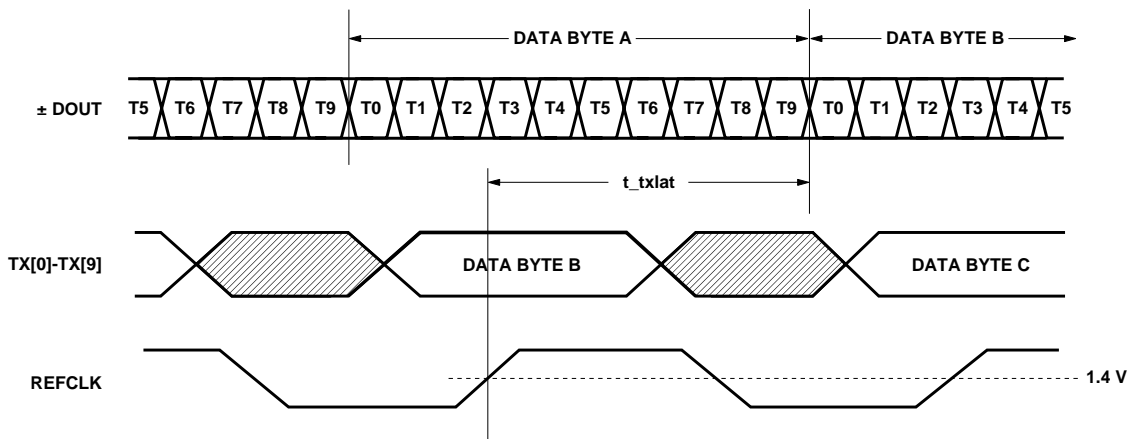

Figure 3. Transmitter Section Timing.

Figure 4. Transmitter Latency.

HDMP-1536/46 (Receiver Section)

Timing Characteristics

T_A[1] = 0°C to +60°C, V_{CC} = 3.15 V to 3.45 V

Symbol	Parameter	Units	Min.	Typ.	Max.
b_sync[2,3]	Bit Sync Time	bits			2500
t_{valid_before}	Time Data Valid Before Rising Edge of RBC	nsec	3	3.8	
t_{valid_after}	Time Data Valid After Rising Edge of RBC	nsec	1.5	3.5	
t_{duty}	RBC Duty Cycle	%	40		60
t_{A-B}[4]	Rising Edge Time Difference	nsec	8.9	9.4	9.9
t_rxlat[5]	Receiver Latency	nsec		24.5	
		bits		26	

Notes:

1. Device tested and characterized under T_A conditions specified, with T_C monitored at approximately 20° higher than T_A.
2. This is the recovery time for input phase jumps, per the FC-PH specification Ref 4.1, Sec 5.3.
3. Tested using C_{PLL} = 0.1 μF.
4. The RBC clock skew is calculated as $t_{A-B(max)}$ - $t_{A-B(min)}$.
5. The receiver latency, as shown in Figure 6, is defined as the time between receiving the first serial bit of a parallel data word (as defined as the first edge of the first serial) and the clocking out of that parallel word (defined by the rising edge of the receive byte clock, either RBC1 or RBC0).
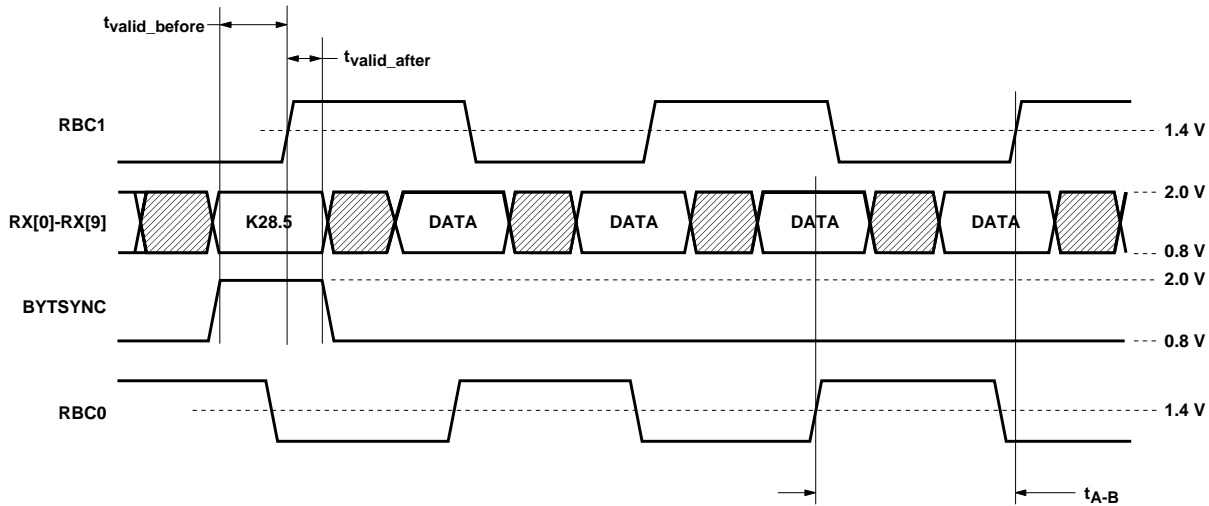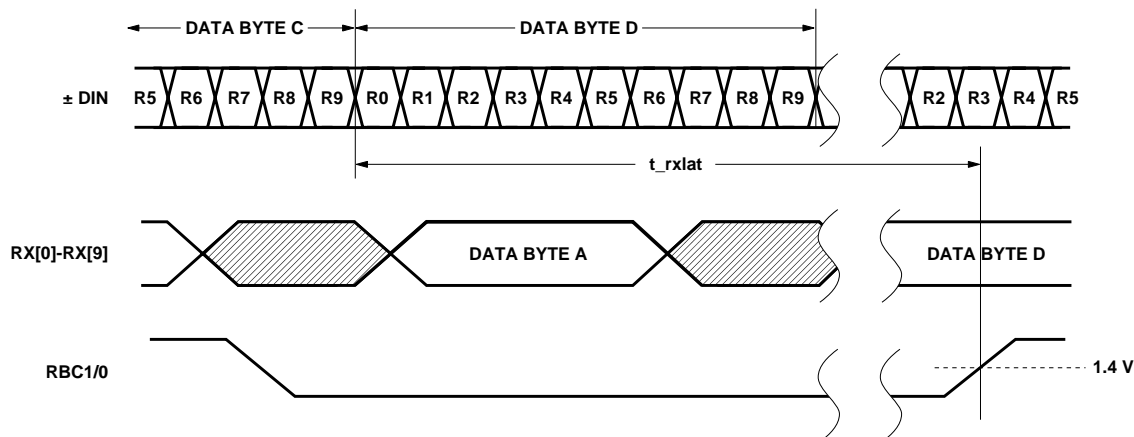

Figure 5. Receiver Section Timing.

Figure 6. Receiver Latency.

Absolute Maximum Ratings

$T_A = 25°C$, except as specified. Operation in excess of any one of these conditions may result in permanent damage to this device.

Symbol	Parameter	Units	Min.	Max.
V_{CC}	Supply Voltage	V	-0.5	5.0
$V_{IN,TTL}$	TTL Input Voltage	V	-0.7	V_{CC} + 0.7
V_{IN,HS_IN}	HS_IN Input Voltage	V	2.0	V_{CC}
$I_{O,TTL}$	TTL Output Source Current	mA		13
T_{stg}	Storage Temperature	°C	-40	+130
T_j	Junction Operating Temperature	°C	0	+130

Guaranteed Operating Rates

$T_A{}^{[1]} = 0°C$ to $+60°C$, $V_{CC} = 3.15$ V to 3.45 V

Parallel Clock Rate (MHz)		Serial Baud Rate (MBaud)	
Min.	Max.	Min.	Max.
106.20	106.30	1062.0	1063.0

Note:

1. Device tested and characterized under T_A conditions specified, with T_C monitored at approximately 20° higher than T_A.

Transceiver Reference Clock Requirements

$T_A{}^{[1]} = 0°C$ to $+60°C$, $V_{CC} = 3.15$ V to 3.45 V

Symbol	Parameter	Unit	Min.	Typ.	Max.
f	Nominal Frequency (for Fibre Channel Compliance)	MHz	106.20	106.25	106.30
F_{tol}	Frequency Tolerance	ppm	-100		+100
Symm	Symmetry (Duty Cycle)	%	40		60

Note:

1. Device tested and characterized under T_A conditions specified, with T_C monitored at approximately 20° higher than T_A.

DC Electrical Specifications

$T_A{}^{[1]} = 0°C$ to $+60°C$, $V_{CC} = 3.15$ V to 3.45 V

Symbol	Parameter	Unit	Min.	Typ.	Max.
$V_{IH,TTL}$	TTL Input High Voltage Level, Guaranteed High Signal for All Inputs	V	2		V_{CC}
$V_{IL,TTL}$	TTL Input Low Voltage Level, Guaranteed Low Signal for All Inputs	V	0		0.8
$V_{OH,TTL}$	TTL Output High Voltage Level, $I_{OH} = -400$ μA	V	2.2		V_{CC}
$V_{OL,TTL}$	TTL Output Low Voltage Level, $I_{OL} = 1$ mA	V	0		0.6
$I_{IH,TTL}$	Input High Current (Magnitude), $V_{IN} = V_{CC}$	μA		0.004	40
I_{IL-TTL}	Input Low Current (Magnitude), $V_{IN} = 0$ Volts	μA		-325	-600
$I_{CC,TRx}{}^{[2,3]}$	Transceiver V_{CC} Supply Current, $T_A = 25°C$	mA		220	

Notes:

1. Device tested and characterized under T_A conditions specified, with T_C monitored at approximately 20° higher than T_A.

2. Measurement Conditions: Tested sending 1062.5 MBd PRBS 2^7-1 sequence from a serial BERT with both DOUT outputs biased with 150 Ω resistors.

3. Typical specified with $V_{CC} = 3.3$ volts, maximum specified with $V_{CC} = 3.45$ volts.

AC Electrical Specifications

$T_A[1] = 0°C$ to $+60°C$, $V_{CC} = 3.15$ V to 3.45 V

Symbol	Parameter	Units	Min.	Typ.	Max.
$t_{r,TTLin}$	Input TTL Rise Time, 0.8 to 2.0 Volts	nsec		2	
$t_{f,TTLin}$	Input TTL Fall Time, 2.0 to 0.8 Volts	nsec		2	
$t_{r,TTLout}$	Output TTL Rise Time, 0.8 to 2.0 Volts, 10 pF Load	nsec		1.5	2.4
$t_{f,TTLout}$	Output TTL Fall Time, 2.0 to 0.8 Volts, 10 pF Load	nsec		1.1	2.4
t_{rs,HS_OUT}	HS_OUT Single-Ended (+DOUT) Rise Time	psec		255	375
t_{fs,HS_OUT}	HS_OUT Single-Ended (+DOUT) Fall Time	psec		185	375
t_{rd,HS_OUT}	HS_OUT Differential Rise Time	psec		255	
t_{fd,HS_OUT}	HS_OUT Differential Fall Time	psec		185	
V_{IP,HS_IN}	HS_IN Input Peak-to-Peak Differential Voltage	mV	200	1200	2000
$V_{OP,HS\_OUT}[2]$	HS_OUT Output Peak-to-Peak Differential Voltage	mV	1200	1600	2200

Notes:

1. Device tested and characterized under T_A conditions specified, with T_C monitored at approximately 20° higher than T_A.
2. Output Peak-to-Peak Differential Voltage specified as DOUT+ minus DOUT-.

200.0 ps/div   22.0680 ns   **Yaxis = 400 mV/DIV**
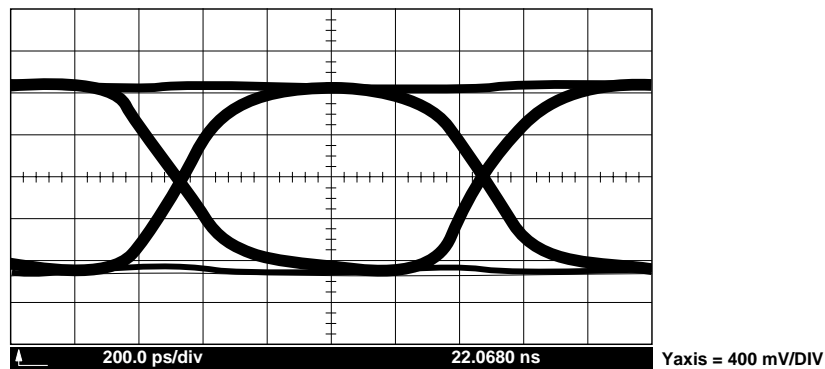
a. Differential HS_OUT Output (Dout+ Minus Dout-).

200.0 ps/div   22.0680 ns   **Yaxis = 200 mV/DIV**
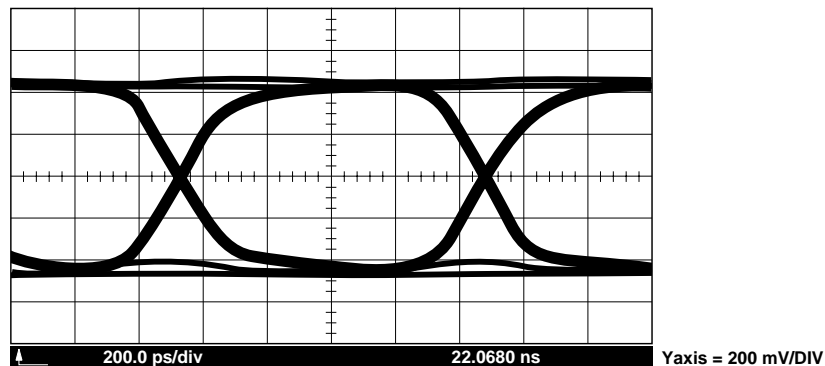
b. Single-Ended HS_OUT Output (Dout+).

Eye Diagrams of the High-Speed Serial Outputs from the HDMP-1536/46 as Captured on the HP 83480A Digital Communications Analyzer. Tested with PRBS = 2^7-1.

**Figure 7. Transmitter DOUT Eye Diagrams.**

Output Jitter Characteristics

$T_A = 25°C$, $V_{CC} = 3.3$ V

Symbol	Parameter	Units	Typ.
RJ[1]	Random Jitter at DOUT, the High Speed Electrical Data Port, specified as 1 sigma deviation of the 50% crossing point (RMS)	ps	8
DJ[1]	Deterministic Jitter at DOUT, the High Speed Electrical Data Port (pk-pk)	ps	15

Note:

1. Defined by Fibre Channel Specification Rev 4.1, Annex A, Section A.4 and tested using measurement method shown in Figure 8.
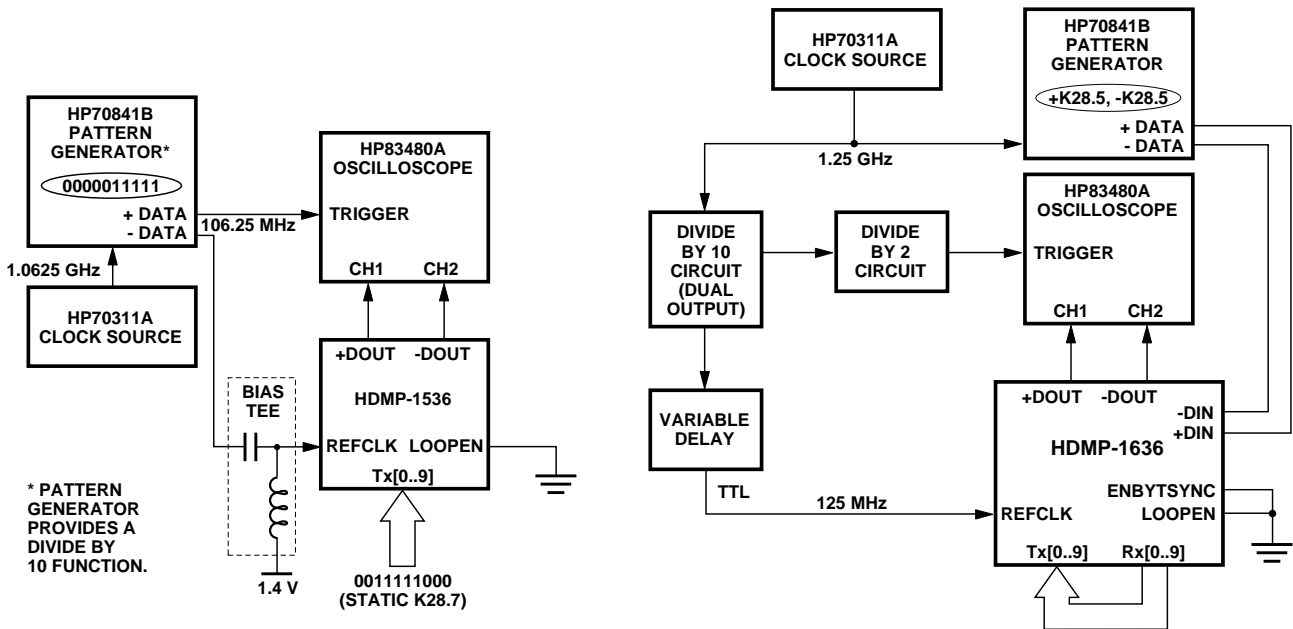
a. Block Diagram of RJ Measurement Method.   b. Block Diagram of DJ Measurement Method.

Figure 8. Transmitter Jitter Measurement Method.

Thermal and Power Temperature Characteristics,

$T_A[1] = 0°C$ to $+60°C$, $V_{CC} = 3.15$ V to 3.45 V

Symbol	Parameter	Units	Typ.	Max.
$P_{D,TRx}$[2,3]	Transceiver Power Dissipation, Outputs Open, Parallel Data has 5 Ones and 5 Zeroes	mW	630	850
$P_{D,TRx}$[2,3,4]	Transceiver Power Dissipation, Outputs Connected per Recommended Bias Terminations with Idle Pattern	mW	685	900
Θ_{jc}[5]	Thermal Resistance, Junction to Case HDMP-1536 HDMP-1546	°C/Watt	10 7	

Notes:

1. Device tested and characterized under T_A conditions specified, with T_C monitored at approximately 20° higher than T_A.

2. P_D is multiplying the max V_{CC} by the max I_{CC} and subtracting the power dissipated outside the chip at the high speed bias resistors.

3. Typical specified with $V_{CC} = 3.3$ volts, maximum specified with $V_{CC} = 3.45$ volts.

4. Specified with high speed outputs biased with 150 Ω resistors and receiver TTL outputs driving 10 pF loads.

5. Based on independant package testing by HP. Θ_{ja} for these devices is 48°C/Watt for the HDMP-1536 and 44°C/Watt for the HDMP-1546. Θ_{ja} is measured on a standard 3x3" FR4 PCB in a still air environment. To determine the actual junction temperature in a given application, use the value as described as follows: $Tj = T_C + (\Theta_{jc} \times Pd)$, where T_C is the case temperature measured on the top center of the package and P_D is the power being dissipated.

I/O Type Definitions

I/O Type	Definition
I-TTL	Input TTL, Floats High When Left Open
O-TTL	Output TTL
HS_OUT	High Speed Output, ECL Compatible
HS_IN	High Speed Input
C	External Circuit Node
S	Power Supply or Ground

Pin Input Capacitance

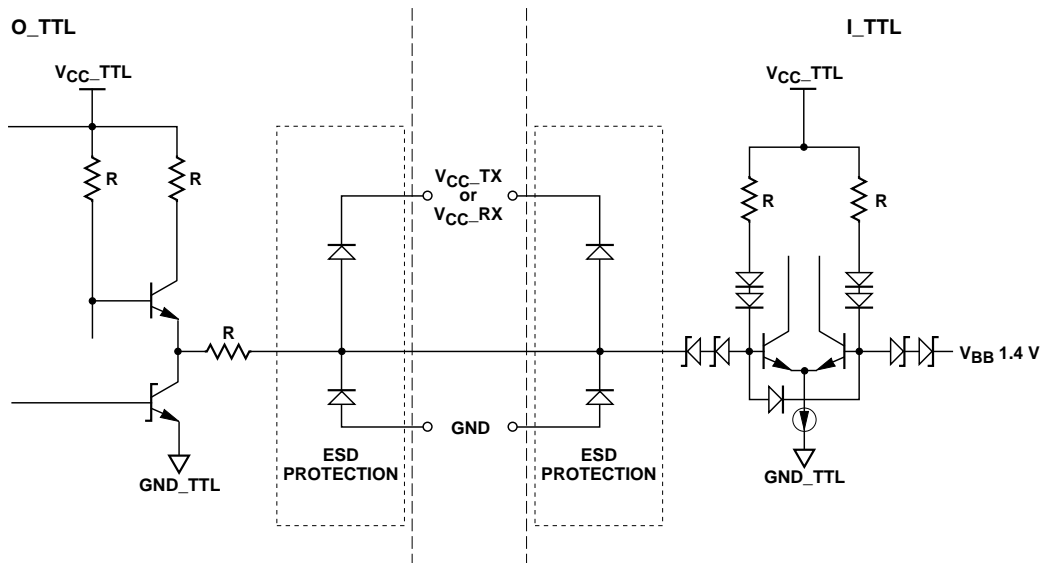| Symbol	Parameter	Units	Typ.	Max.
C_{INPUT}	Input Capacitance on TTL Input Pins	pF	1.6	

Figure 9. O-TTL and I-TTL Simplified Circuit Schematic.
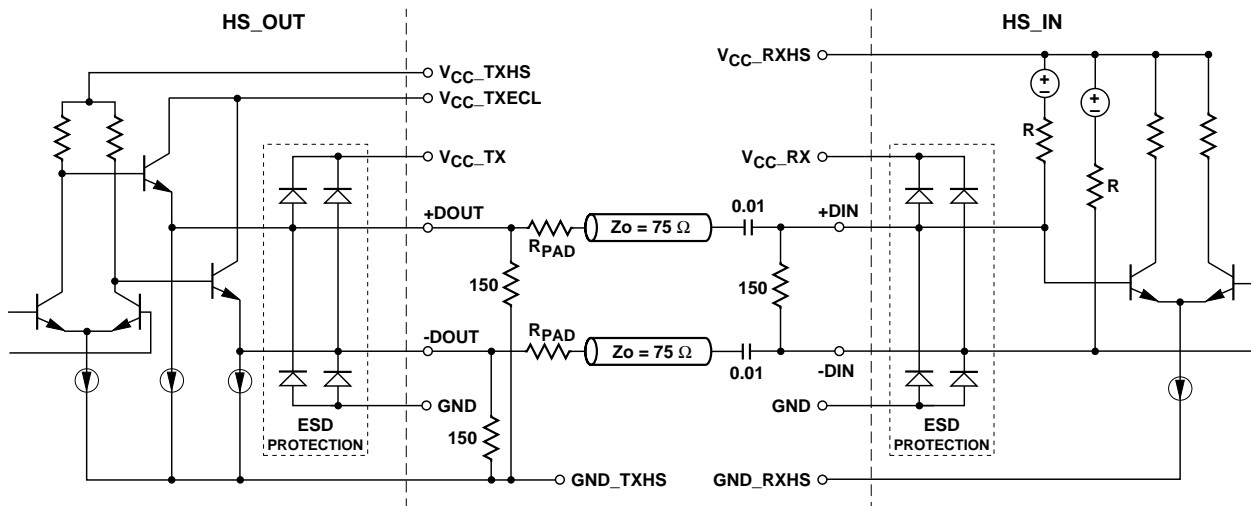
Figure 10. HS_OUT and HS_IN Simplified Circuit Schematic.

Notes:

1. HS_IN inputs should never be connected to ground as permanent damage to the device may result.

2. The optional series padding resistors (Rpad) help dampen load reflections. Typical Rpad values for mismatched loads range between 25-75 Ω.
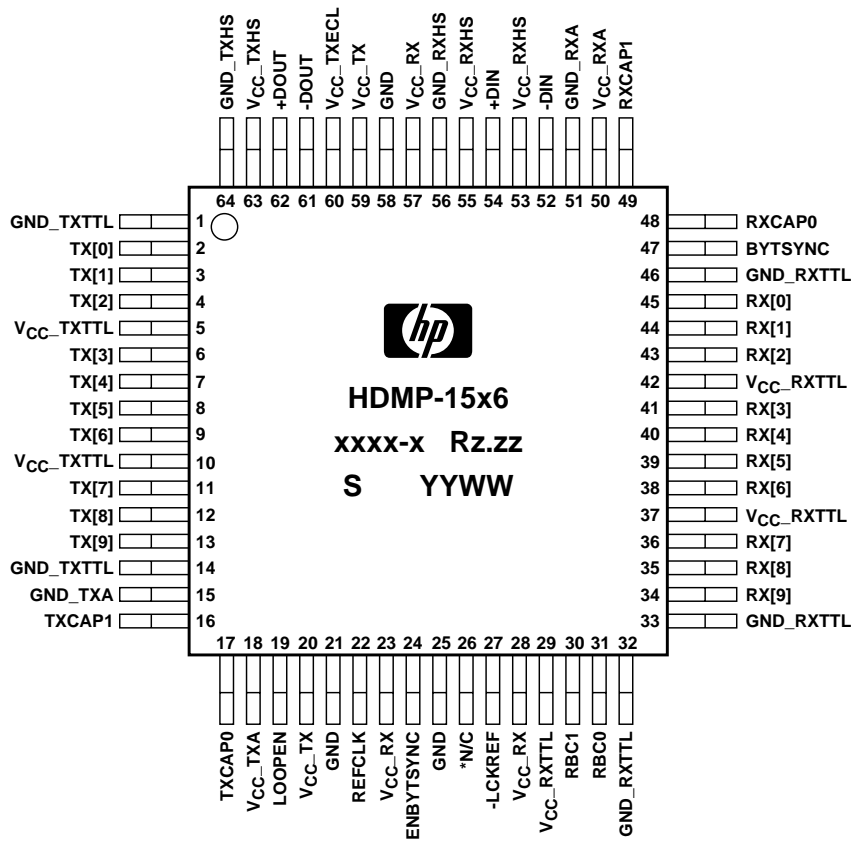
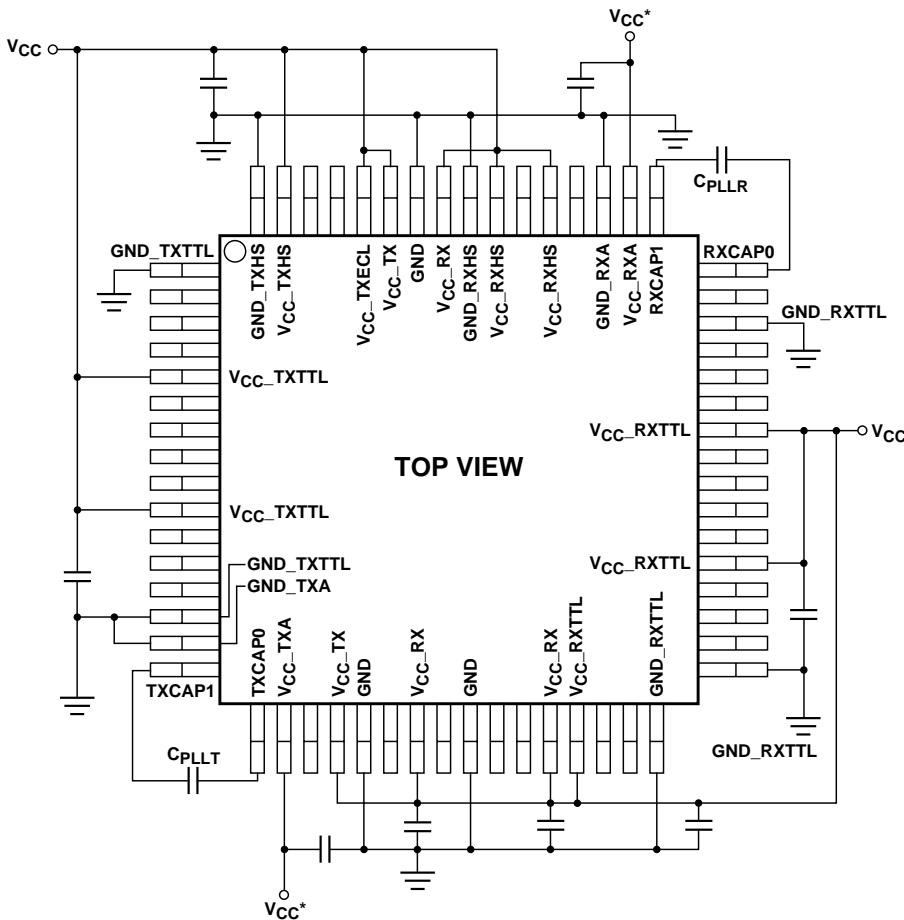**Figure 11. HDMP-1536/46 (TRx) Package Layout and Marking, Top View.**

*Note: Pin 26 is designated as a "no connect" pin and should be left unconnected.

TRx I/O Definition

Name	Pin	Type	Signal
BYTSYNC	47	O-TTL	**Byte Sync Output:** An active high output. Used to indicate detection of either a comma character or a K28.5 special character (0011111XXX). It is only active when ENBYTSYNC is enabled.
-DIN +DIN	52 54	HS_IN	**Serial Data Inputs:** High-speed inputs. Serial data is accepted from the ± DIN inputs when LOOPEN is low.
-DOUT +DOUT	61 62	HS_OUT	**Serial Data Outputs:** High-speed outputs. These lines are active when LOOPEN is set low. When LOOPEN is set high, these outputs are held static.
ENBYTSYNC	24	I-TTL	**Enable Byte Sync Input:** When high, turns on the internal byte sync function to allow clock synchronization to a comma character, or a K28.5 character (0011111XXX). When the line is low, the function is disabled and will not reset registers and clocks, or strobe the BYTSYNC line.
GND	21 25 58	S	**Logic Ground:** Normally 0 volts. This ground is used for internal PECL logic. It should be isolated from the noisy TTL ground as well as possible.
GND_RXA	51	S	**Analog Ground:** Normally 0 volts. Used to provide a clean ground plane for the receiver PLL and high-speed analog cells.
GND_RXHS	56	S	**Ground:** Normally 0 volts.
GND_RXTTL	32 33 46	S	**TTL Receiver Ground:** Normally 0 volts. Used for the TTL output cells of the receiver section.
GND_TXA	15	S	**Analog Ground:** Normally 0 volts. Used to provide a clean ground plane for the PLL and high-speed analog cells.
GND_TXHS	64	S	**Ground:** Normally 0 volts.
GND_TXTTL	1 14	S	**TTL Transmitter Ground:** Normally 0 volts. Used for the TTL input cells of the transmitter section.
-LCKREF	27	I-TTL	**Lock to Reference:** When low, causes the PLL to acquire frequency and phase lock on the external reference, supplied at REFCLK. When high, the Rx PLL will automatically frequency lock to REFCLK and phase lock to the high speed data stream.
LOOPEN	19	I-TTL	**Loopback Enable Input:** When set high, the high-speed serial signal is internally wrapped from the transmitter's serial loopback outputs back to the receiver's loopback inputs. Also, when in loopback mode, the ± DOUT outputs are held static. When set low, ± DOUT outputs and ± DIN inputs are active.
RBC1 RBC0	30 31	O-TTL	**Receiver Byte Clocks:** The receiver section recovers two 53.125 MHz receive byte clocks. These two clocks are 180 degrees out of phase. The receiver parallel data outputs are alternatively clocked on the rising edge of these clocks. The rising edge of RBC1 aligns with the output of the comma character (for byte alignment) when detected.
REFCLK	22	I-TTL	**Reference Clock and Transmit Byte Clock:** A 106.25 MHz clock supplied by the host system. The transmitter section accepts this signal as the frequency reference clock. It is multiplied by 10 to generate the serial bit clock and other internal clocks. The transmit side also uses this clock as the transmit byte clock for the incoming parallel data TX[0]..TX[9]. It also serves as the reference clock for the receive portion of the transceiver.

TRx I/O Definition (cont'd.)

Name	Pin	Type	Signal
RX[0] RX[1] RX[2] RX[3] RX[4] RX[5] RX[6] RX[7] RX[8] RX[9]	45 44 43 41 40 39 38 36 35 34	O-TTL	**Data Outputs:** One 10 bit data byte. RX[0] is the first bit received. RX[0] is the least significant bit.
RXCAP0 RXCAP1	48 49	C	**Loop Filter Capacitor:** A loop filter capacitor for the internal PLL must be connected across the RXCAP0 and RXCAP1 pins. (typical value = 0.1 μF).
TX[0] TX[1] TX[2] TX[3] TX[4] TX[5] TX[6] TX[7] TX[8] TX[9]	2 3 4 6 7 8 9 11 12 13	I-TTL	**Data Inputs:** One, 10 bit, pre-encoded data byte. TX[0] is the first bit transmitted. TX[0] is the least significant bit.
TXCAP1 TXCAP0	16 17	C	**Loop Filter Capacitor:** A loop filter capacitor must be connected across the TXCAP1 and TXCAP0 pins (typical value = 0.1 μF).
V_{CC}_RX	23 28 57	S	**Logic Power Supply:** Normally 3.3 volts. Used for internal receiver PECL logic. It should be isolated from the noisy TTL supply as well as possible.
V_{CC}_RXA	50	S	**Analog Power Supply:** Normally 3.3 volts. Used to provide a clean supply line for the PLL and high-speed analog cells.
V_{CC}_RXHS	53 55	S	**High-Speed Supply:** Normally 3.3 volts. Used only for the high-speed receiver cell (HS_IN). Noise on this line should be minimized for best operation.
V_{CC}_RXTTL	29 37 42	S	**TTL Power Supply:** Normally 3.3 volts. Used for all TTL receiver output buffer cells.
V_{CC}_TX	20 59	S	**Logic Power Supply:** Normally 3.3 volts. Used for internal transmitter PECL logic. It should be isolated from the noisy TTL supply as well as possible.
V_{CC}_TXA	18	S	**Analog Power Supply:** Normally 3.3 volts. Used to provide a clean supply line for the PLL and high-speed analog cells.
V_{CC}_TXECL	60	S	**High-Speed ECL Supply:** Normally 3.3 volts. Used only for the last stage of the high-speed transmitter output cell (HS_OUT) as shown in Figure 10. Due to high current transitions, this V_{CC} should be well bypassed to a ground plane.
V_{CC}_TXHS	63	S	**High-Speed Supply:** Normally 3.3 volts. Used by the transmitter side for the high-speed circuitry. Noise on this line should be minimized for best operation.
V_{CC}_TXTTL	5 10	S	**TTL Power Supply:** Normally 3.3 volts. Used for all TTL transmitter input buffer cells.

V_{CC}

V_{CC}*

C_{PLLR}

GND_TXTTL

GND_TXHS V_{CC}_TXHS V_{CC}_TXECL V_{CC}_TX GND V_{CC}_RX GND_RXHS V_{CC}_RXHS V_{CC}_RXHS GND_RXA V_{CC}_RXA RXCAP1 RXCAP0

GND_RXTTL

V_{CC}_TXTTL

TOP VIEW

V_{CC}_RXTTL

V_{CC}_TXTTL

V_{CC}_RXTTL

GND_TXTTL
GND_TXA

V_{CC}

TXCAP1 TXCAP0 V_{CC}_TXA V_{CC}_TX GND V_{CC}_RX GND V_{CC}_RX V_{CC}_RXTTL GND_RXTTL

GND_RXTTL

C_{PLLT}

V_{CC}*

* SUPPLY VOLTAGE INTO V_{CC}_RXA AND V_{CC}_TXA SHOULD
BE FROM A LOW NOISE SOURCE. ALL BYPASS CAPACITORS
AND PLL FILTER CAPACITORS ARE 0.1 µF.

Figure 12. Power Supply Bypass.

Start-up Procedure:

The transceiver start-up procedure(s) use the following conditions: V_{CC} = +3.3 V ± 5% and REFCLK = 106.25 MHz ± 100 ppm.

Auto-Lock Used Exclusively

Set -LCKREF = 1 and apply valid data using a balanced code such as 8B/10B. Frequency lock occurs within 500 µs. After frequency lock, phase lock occurs within 2500 bit times.

User Controlled

Set -LCKREF = 0 for at least 500 µs (frequency lock will occur within 500 µs). After valid 8B/10B data is applied to the Rx input, set -LCKREF=1. Phase lock will occur within 2500 bit times. In this case, asserting -LCKREF = 0 forces the Rx PLL to fully phase and frequency lock onto the reference clock (REFCLK) disregarding the serial data stream completely. Asserting -LCKREF = 0 is an option for

users that want full control during the frequency acquisition process.

Transceiver Power Supply Bypass and Loop Filter Capacitors

Bypass capacitors should be used and placed as close as possible to the appropriate power supply pins of the HDMP-1536/46 as shown on the schematic of Figure 12. All bypass chip capacitors are 0.1 µF. The V_{CC}_RXA and V_{CC}_TXA pins are the analog power supply pins for the PLL sections. The voltage into these pins should be clean with minimum noise. The PLL loop filter capacitors and their pin locations are also shown on Figure 12. Notice that only two capacitors are required: C_{PLLT} for the transmitter and C_{PLLR} for the receiver. Nominal capacitance is 0.1 µF. The voltage across the capacitors is on the order of 1 volt, so the capacitor can be a low voltage type and physically small. The PLL capacitors are placed physically close to the appropriate pins on the HDMP-1536/46. Keeping the lines short will prevent them from picking up stray noise from surrounding lines or components.

Package Information

Item	Details	
Package Material	Plastic	
Lead Finish Material	85% Tin, 15% Lead	
Lead Finish Thickness	300-800 μm	
Lead Coplanarity	HDMP-1536 0.08 mm max.	HDMP-1546 0.10 mm max.

Mechanical Dimensions
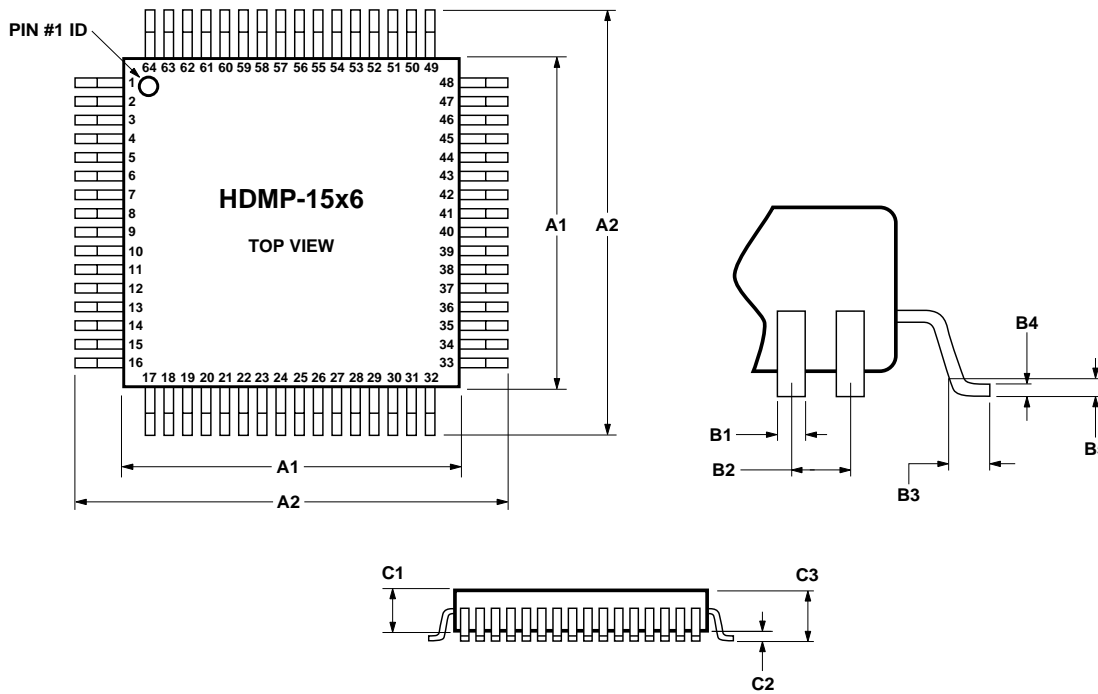
Part Number	A1	A2	B1	B2	B3	B4	B5	C1	C2	C3
HDMP-1536	10.00	13.20	0.22	0.50	0.88	0.17	0.25	2.00	0.25 min.	2.45
HDMP-1546	14.00	17.20	0.35	0.80	0.88	0.17	0.25	2.00	0.25 max.	2.35
Tolerance	± 0.10	± 0.25	± 0.05	Basic	+0.15 -0.10	max.		+0.10/-0.05		max.

Figure 13. Mechanical Dimensions of HDMP-1536/46.