Silicon Bipolar MMIC 3.5 and 5.5 GHz Divide-by-4 Static Prescalers

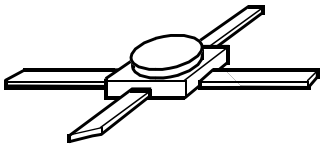
Technical Data

IFD-53010
IFD-53110

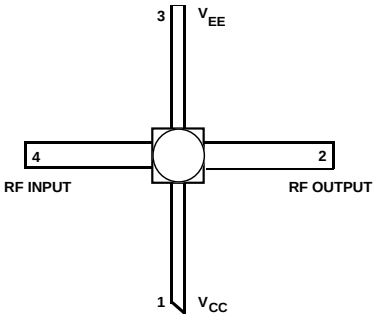
Features

- **Wide Operating Frequency Range:**
  IFD-53010: 0.15 to 5.5 GHz
  IFD-53110: 0.15 to 3.5 GHz
- **Low Phase Noise:**
  -143 dBc/Hz @ 1 kHz Offset
- **Output Power:** -5 dBm Typ.
- **Single Supply Voltage**
  V_{cc} = 5 V or V_{ee} = -5 V
- **On-Chip Terminations Provide Good Input and Output VSWRs**
- **Hermetic Gold-Ceramic Surface Mount Package**

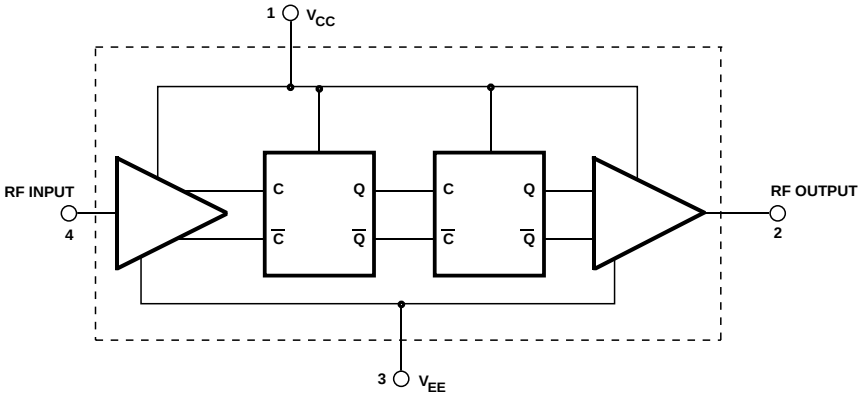
100 mil Stripline Package



Pin Configuration



Functional Block Diagram



Description

Hewlett-Packard's IFD-53010 and IFD-53110 are low phase noise silicon bipolar static digital frequency dividers using two scaled Emitter-Coupled-Logic (ECL) master-slave D flip-flops and buffer amplifiers. They are housed in hermetic high reliability surface mount packages suitable for commercial, industrial, and military applications. Typical applications include stabilized or digitally controlled local oscillators for GPS, SATCOM or military receivers, and frequency synthesizers and counters in instrumentation systems. The IFD-53110 is a lower cost selected version of the IFD-53010, and is distinguished by a reduced operating frequency range.

The IFD series of frequency dividers is fabricated using Hewlett-Packard's 18 GHz, f_t, ISOSAT™-2 silicon bipolar process which uses nitride self-alignment, submicrometer lithography, trench isolation, ion-implantation, gold metallization and polyimide intermetal dielectric and scratch protection to achieve excellent device uniformity, performance, and reliability.

Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{cc} - V_{ee}	Device Voltage	V	8
P_{diss}	Power Dissipation[2,3]	mW	650
P_{in}	RF Input Power	dBm	+15
T_j	Junction Temperature	°C	200
T_{STG}	Storage Temperature	°C	-65 to +200

Thermal Resistance[2]: θ_{jc} = 107°C/W

Notes:
1, Operation of this device above any one of these parameters may cause permanent damage.
2. T_{case} = 25°C.
3. Derate at 9.3 mW/°C for $T_C \geq$ 130°C.

Guaranteed Electrical Specifications, IFD-53010 and IFD-53110

T_A = 25°C, Z_O = 50 Ω, V_{cc} - V_{ee} = 5.0 V

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
F_{MAX}	IFD-53010: Maximum Clock Frequency P_{in} = -10 dBm (200 mVpp)	GHz	5.5	6.0	
F_{MAX}	IFD-53110: Maximum Clock Frequency P_{in} = -10 dBm (200 mVpp)	GHz	3.5	5.0	
I_{CC}	IFD-53010 and IFD-53110: Supply Current	mA	35	43	50

Typical Design Information, T_A = 25°C, Z_0 = 50 Ω, V_{cc} - V_{ee} = 5.0 V, P_{in} = -10 dBm.

All values apply to both IFD-53010 and IFD-53110. f_{test} is 5 GHz for IFD-53010 and 3 GHz for IFD-53110 (unless otherwise noted).

Symbol	Parameters and Test Conditions	Units	Value
F_{MIN}	Minimum Clock Frequency[1]	MHz	150
P_{in}	Input Sensitivity $f = f_{test}$	dBm mVpp	-22 50
P_{out}	Output Power f = 0.15 to f_{test}	dBm mVpp	-5 355
VSWR	Input VSWR f = 0.15 to f_{test} Output VSWR f = 0.15 to f_{test}		2.0:1 2.5:1
PN	SSB Phase Noise f = 3 GHz, 1 kHz offset f = 5 GHz, 1 kHz offset (IFD-53010 only)	dBc/Hz	-143 -138
T_r	Output Rise Time, 20% - 80% $f = f_{test}$	psec	145
T_f	Output Fall Time, 20% - 80% $f = f_{test}$	psec	85

Note:
1. Minimum clock frequency when driven from a sinusoidal input. Operation to lower frequencies is possible when using input signals with faster rise times, such as occurs in the case of a cascade of two or more IFDs.

Typical Performance, $T_A = 25°C, Z_O = 50\,\Omega, V_{cc} - V_{ee} = 5.0\,V$

Graphs apply to both IFD-53010 and IFD-53110 (unless otherwise noted).

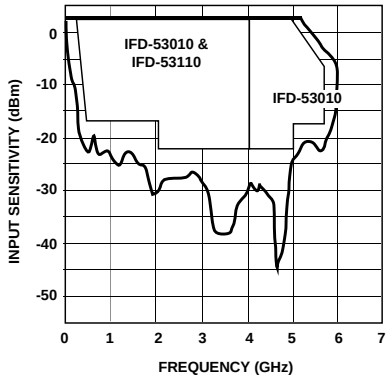


Figure 1. Input Sensitivity vs. Input Frequency and Recommended Operating Ranges for Nominal Operating Conditions (T = 25°C , V_{cc} - V_{ee} = 5 V).

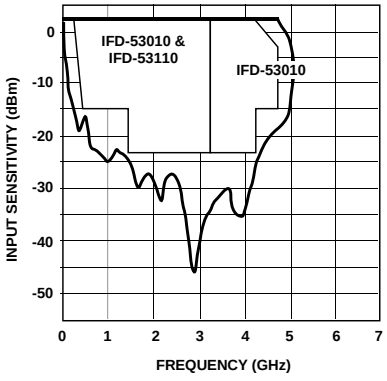


Figure 2. Input Sensitivity vs. Input Frequency and Recommended Operating Ranges for Worst Case Operating Conditions (-55°C < T < 125°C and 4.5 V < V_{cc} - V_{ee} < 5.5 V.

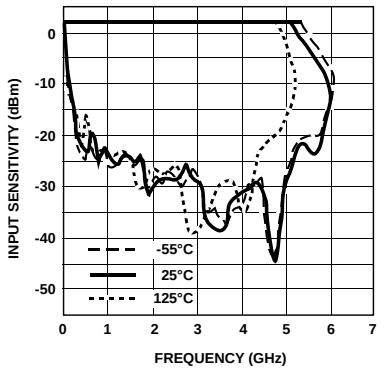


Figure 3. Input Sensitivity vs. Input Frequency and Temperature (V_{cc} - V_{ee} = 5 V).

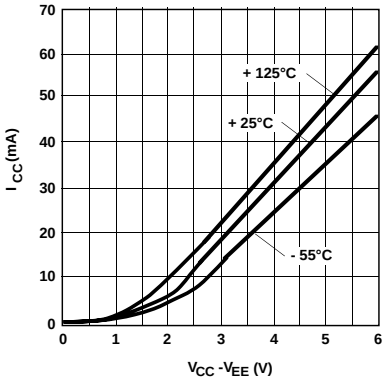


Figure 4. Device Current vs. Voltage and Temperature.

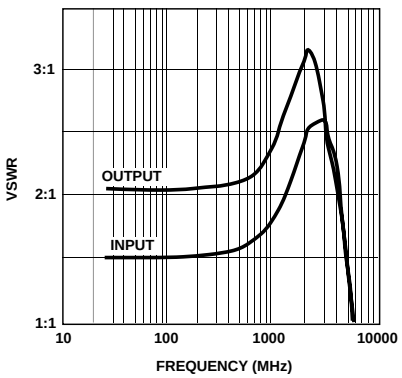


Figure 5. Input and Output VSWR vs. Frequency.

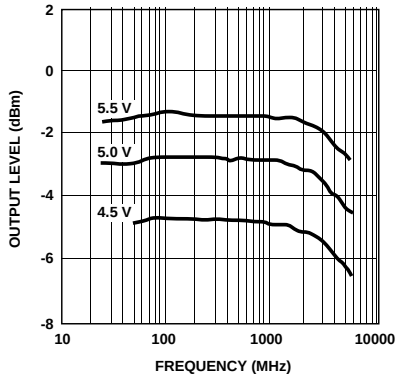


Figure 6. Output Power Level vs. Input Frequency and V_{cc} - V_{ee}.

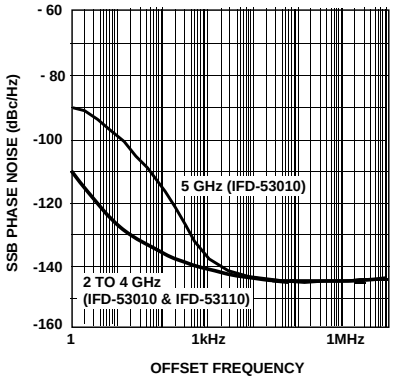


Figure 7. SSB Phase Noise vs. Offset Frequency, and Input Frequency.

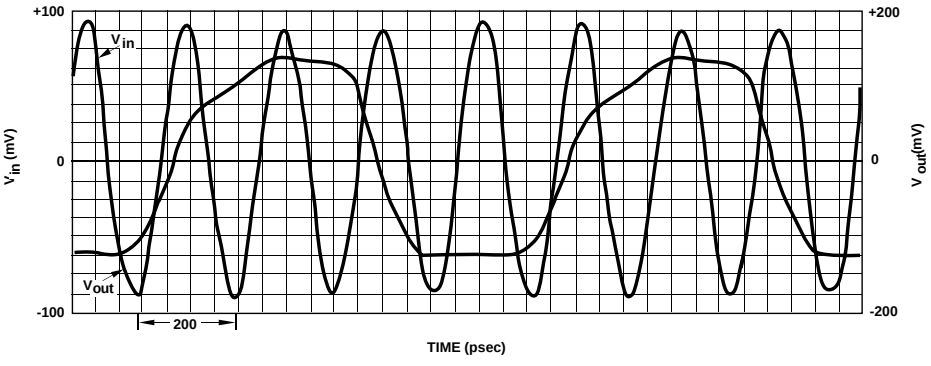


Figure 8. IFD-53010 Typical Output Response with 5 GHz Input.

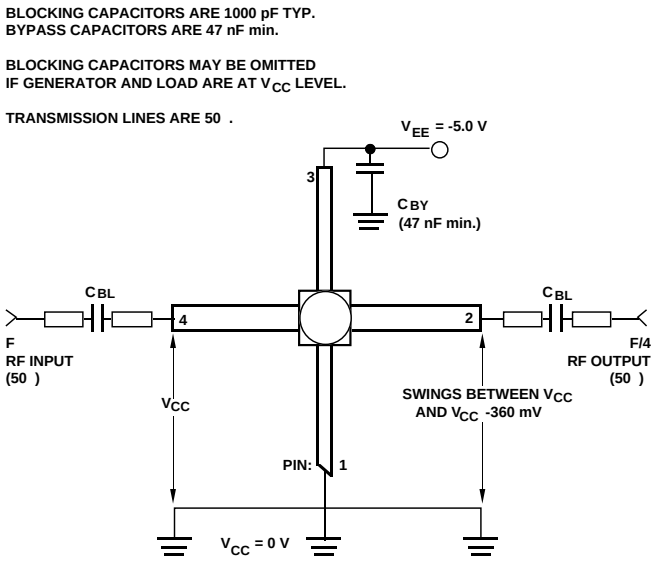


Figure 9. Typical ECL Biasing Configuration, IFD-53010 and IFD-53110.

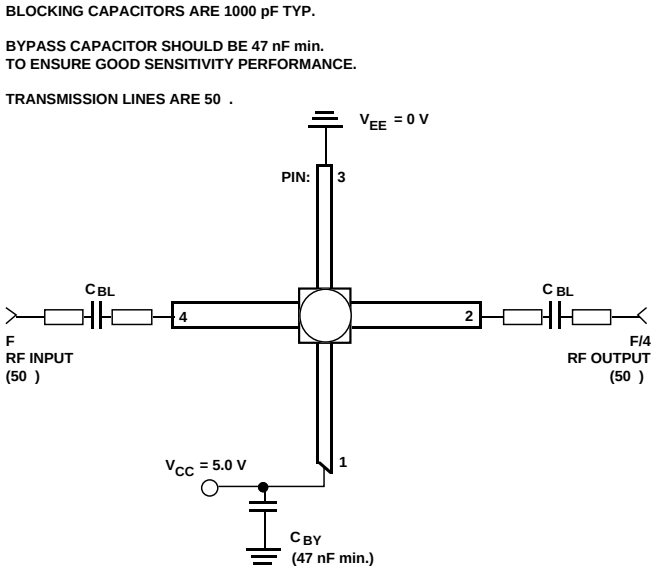


Figure 10. Typical RF Biasing Configuration, IFD-53010 and IFD-53110.

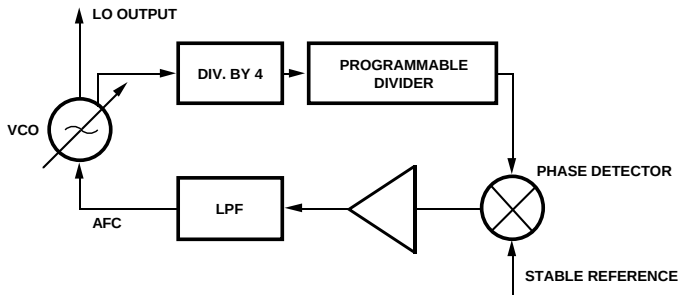


Figure 11. Typical Stabilized LO Configuration, IFD-53010 and IFD-53110.

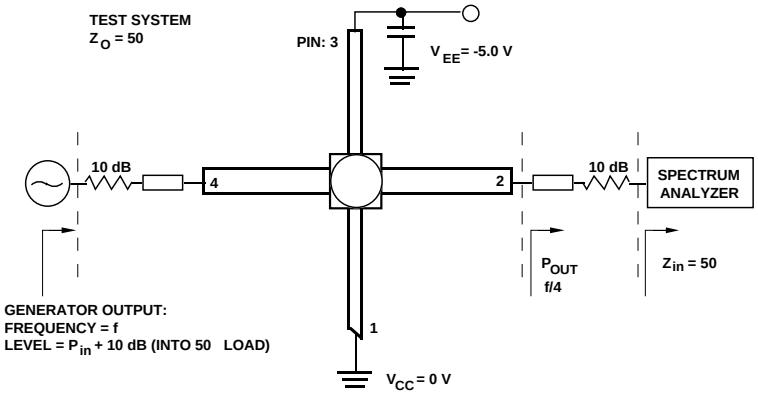


Figure 12. Sensitivity Test Configuration, IFD-53010 and IFD-53110.

Package Dimensions

100 mil Stripline Package