High CMR, High Speed Optocouplers

Technical Data

HCPL-4504
HCPL-0454
HCNW4504

Features

- **Short Propagation Delays for TTL and IPM Applications**
- **15 kV/µs Minimum Common Mode Transient Immunity at V_{CM} = 1500 V for TTL/Load Drive**
- **High CTR at T_A = 25°C**
  >25% for HCPL-4504/0454
  >23% for HCNW4504
- **Electrical Specifications for Common IPM Applications**
- **TTL Compatible**
- **Guaranteed Performance from 0°C to 70°C**
- **Open Collector Output**
- **Safety Approval**
  UL Recognized - 2500 V rms for 1 minute (5000 V rms for 1 minute for HCPL-4504#020 and HCNW4504)per UL1577
  CSA Approved
  VDE 0884 Approved
  -V_{IORM} = 630 V peak for HCPL-4504#060
  -V_{IORM} = 1414 V peak for HCNW4504
  BSI Certified (HCNW4504)
- **Available in 8-Pin DIP, SO-8, Widebody Packages**

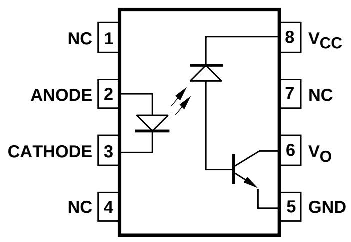
Applications

- **Inverter Circuits and Intelligent Power Module (IPM) interfacing -**
  High Common Mode Transient Immunity (> 10 kV/µs for an IPM load/drive) and (t_{PLH} - t_{PHL}) Specified (See Power Inverter Dead Time section)
- **Line Receivers -**
  Short Propagation Delays and Low Input-Output Capacitance
- **High Speed Logic Ground Isolation - TTL/TTL, TTL/CMOS, TTL/LSTTL**
- **Replaces Pulse Transformers -**
  Save Board Space and Weight
- **Analog Signal Ground Isolation -**
  Integrated Photodetector Provides Improved Linearity over Phototransistors

Description

These optocouplers are similar to HP's other high speed transistor optocouplers but with shorter propagation delays and higher CTR. The HCPL-4504/0454 and HCNW4504 also have a guaranteed propagation delay difference (t_{PLH} - t_{PHL}). These features make these optocouplers an excellent solution to IPM inverter dead time and other switching problems.

Functional Diagram



TRUTH TABLE

LED	V_O
ON	LOW
OFF	HIGH

A 0.1 µF bypass capacitor between pins 5 and 8 is recommended.

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

The HCPL-4504/0454 and HCNW4504 CTR, propagation delay, and CMR are specified for both TTL and IPM load/drive conditions. Specifications and typical performance plots for both TTL and IPM conditions are provided for ease of application.

These single channel, diode-transistor optocouplers are available in 8-Pin DIP, SO-8, and Widebody package configurations. An insulating layer between a LED and an integrated photodetector provide electrical insulation between input and output. Separate connections for the photodiode bias and output-transistor collector increase the speed up to a hundred times that of a conventional phototransistor coupler by reducing the base collector capacitance.

Selection Guide

Single Channel Packages		
8-Pin DIP (300 Mil)	**Small Outline SO-8**	**Widebody (400 Mil)**
HCPL-4504	HCPL-0454	HCNW4504

Ordering Information

Specify Part Number followed by Option Number (if desired).

Example:

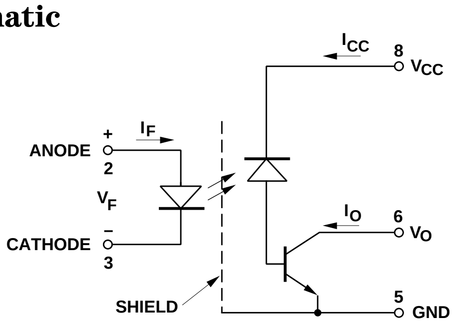
HCPL-4504#XXX

- 020 = UL 5000 V rms/1 Minute Option*
- 060 = VDE 0884 V_{IORM} = 630 V $_{peak}$ Option*
- 300 = Gull Wing Surface Mount Option†
- 500 = Tape and Reel Packaging Option

Option data sheets available. Contact your Hewlett-Packard sales representative or authorized distributor for information.

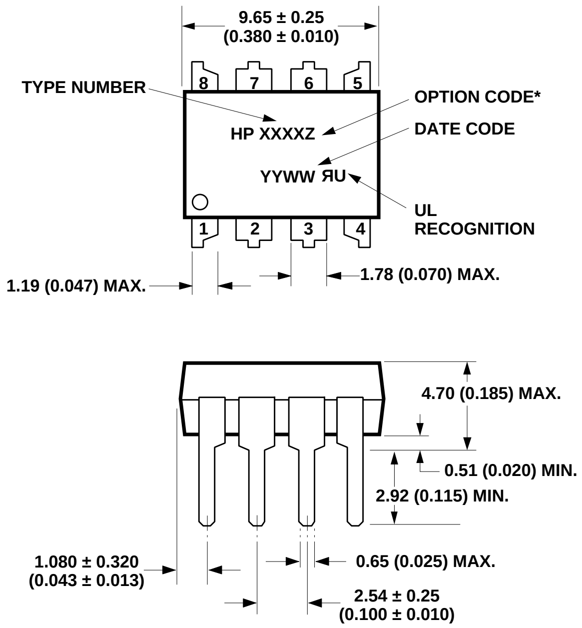
*For HCPL-4504 only. Combination of Option 020 and Option 060 is not available.
†Gull wing surface mount option applies to through hole parts only.

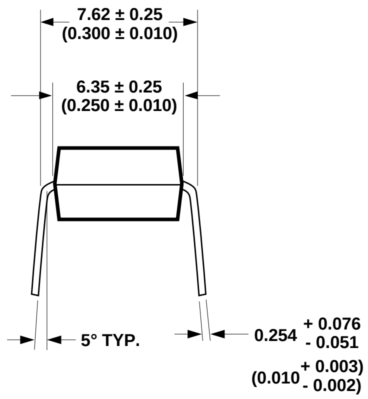
Schematic



Package Outline Drawings

8-Pin DIP Package (HCPL-4504)

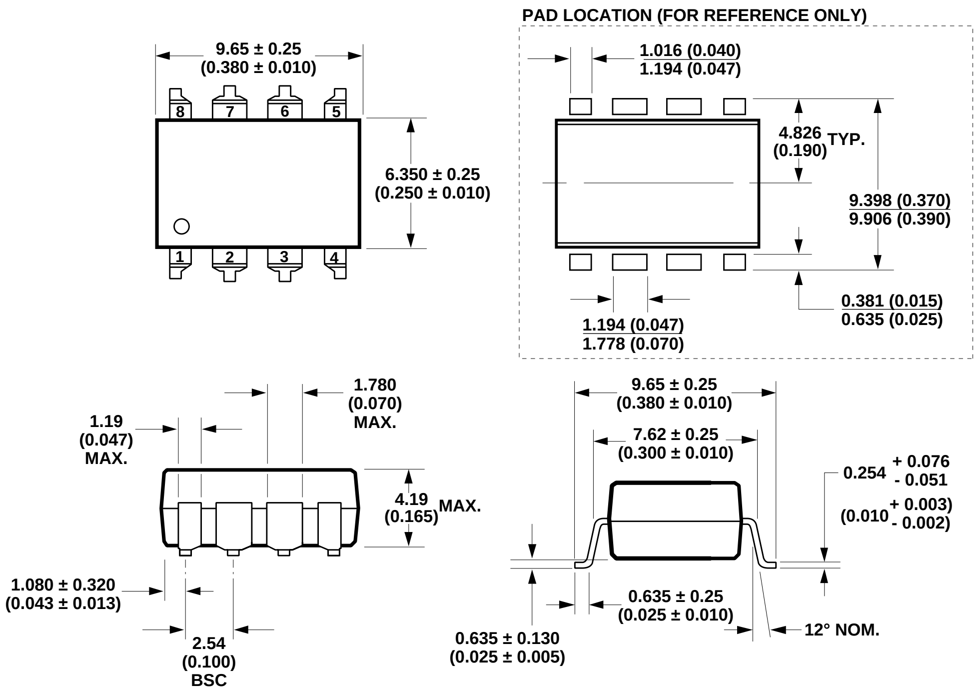




DIMENSIONS IN MILLIMETERS AND (INCHES).

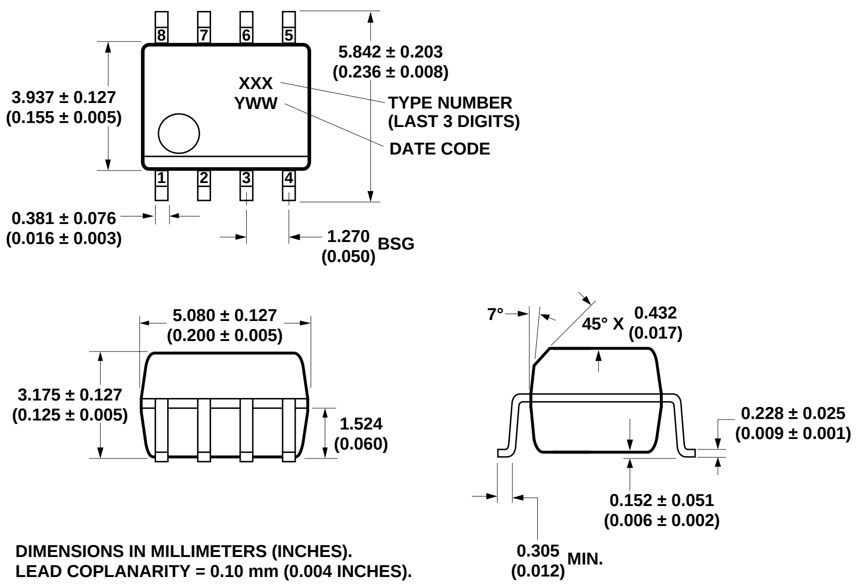
* MARKING CODE LETTER FOR OPTION NUMBERS.
"L" = OPTION 020
"V" = OPTION 060
OPTION NUMBERS 300 AND 500 NOT MARKED.

8-Pin DIP Package with Gull Wing Surface Mount Option 300 (HCPL-4504)

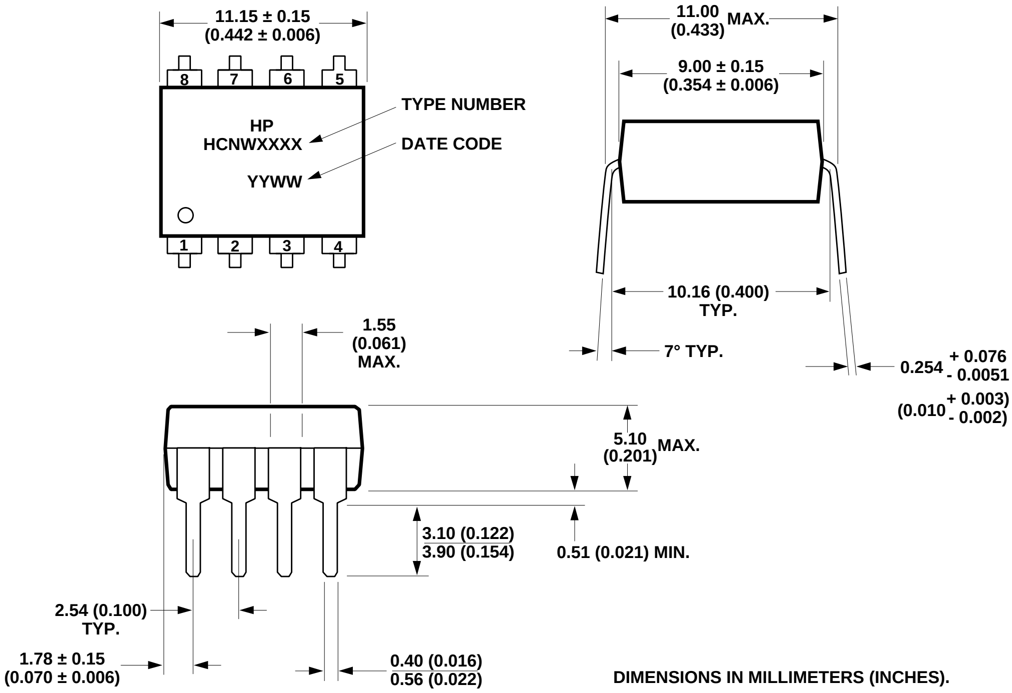


DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

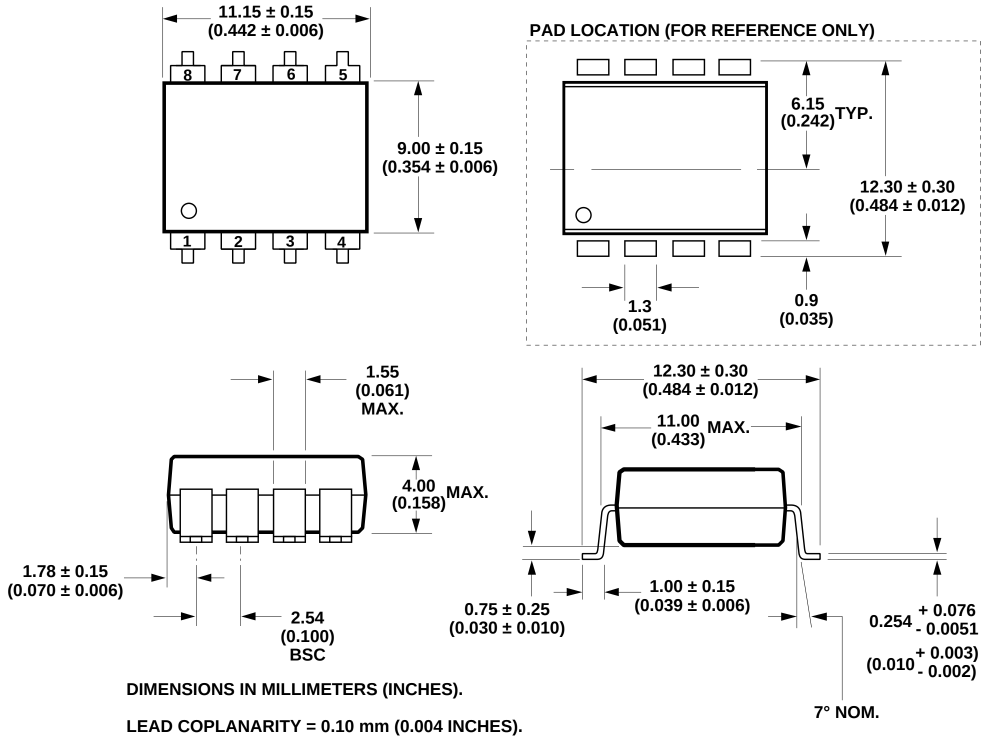
Small Outline SO-8 Package (HCPL-0454)



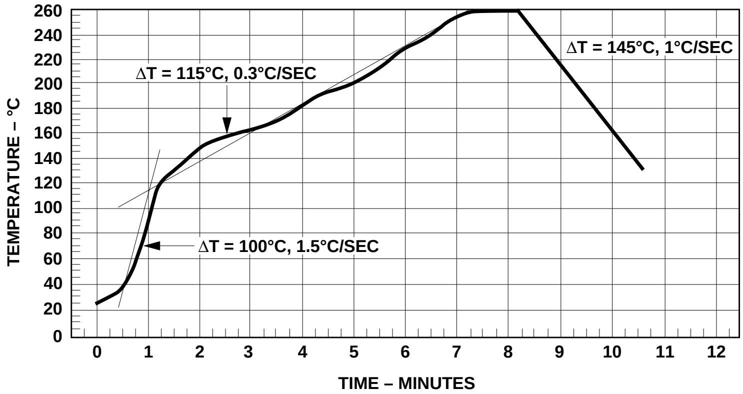
8-Pin Widebody DIP Package (HCNW4504)



8-Pin Widebody DIP Package with Gull Wing Surface Mount Option 300 (HCNW4504)



Solder Reflow Temperature Profile (HCPL-0454 and Gull Wing Surface Mount Option Parts)



Note: Use of nonchlorine activated fluxes is highly recommended.

Regulatory Information

The devices contained in this data sheet have been approved by the following organizations:

UL

Recognized under UL 1577, Component Recognition Program, File E55361.

CSA

Approved under CSA Component Acceptance Notice #5, File CA 88324.

VDE

Approved according to VDE 0884/06.92 (HCNW4504 and HCPL-4504#060 only).

BSI

Certification according to BS451:1994, (BS EN60065:1994); BS EN60950:1992 (BS7002:1992) and EN41003:1993 for Class II applications (HCNW4504 only).

Insulation and Safety Related Specifications

Parameter	Symbol	8-Pin DIP (300 Mil) Value	SO-8 Value	Widebody (400 Mil) Value	Units	Conditions
Minimum External Air Gap (External Clearance)	L(101)	7.1	4.9	9.6	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	7.4	4.8	10.0	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	0.08	1.0	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity.
Minimum Internal Tracking (Internal Creepage)		NA	NA	4.0	mm	Measured from input terminals to output terminals, along internal cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	200	200	200	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa	IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Option 300 - surface mount classification is Class A in accordance with CECC 00802.

VDE 0884 Insulation Related Characteristics (HCPL-4504 OPTION 060 ONLY)

Description	Symbol	Characteristic	Units
Installation classification per DIN VDE 0110/1.89, Table 1 for rated mains voltage ≤ 300 V rms		I-IV	
for rated mains voltage ≤ 450 V rms		I-III	
Climatic Classification		55/100/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	630	V peak
Input to Output Test Voltage, Method b* V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	1181	V peak
Input to Output Test Voltage, Method a* V_{IORM} x 1.5 = V_{PR}, Type and sample test, t_m = 60 sec, Partial Discharge < 5 pC	V_{PR}	945	V peak
Highest Allowable Overvoltage* (Transient Overvoltage, t_{ini} = 10 sec)	V_{IOTM}	6000	V peak
Safety Limiting Values (Maximum values allowed in the event of a failure, also see Figure 15, Thermal Derating curve.) Case Temperature Input Current Output Power	 T_S $I_{S,INPUT}$ $P_{S,OUTPUT}$	 175 230 600	 °C mA mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	≥ 10^9	Ω

VDE 0884 Insulation Related Characteristics (HCNW4504 ONLY)

Description	Symbol	Characteristic	Units
Installation classification per DIN VDE 0110/1.89, Table 1 for rated mains voltage ≤ 600 V rms		I-IV	
for rated mains voltage ≤ 1000 V rms		I-III	
Climatic Classification		55/85/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	1414	V peak
Input to Output Test Voltage, Method b* V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	2652	V peak
Input to Output Test Voltage, Method a* V_{IORM} x 1.5 = V_{PR}, Type and sample test, t_m = 60 sec, Partial Discharge < 5 pC	V_{PR}	2121	V peak
Highest Allowable Overvoltage* (Transient Overvoltage, t_{ini} = 10 sec)	V_{IOTM}	8000	V peak
Safety Limiting Values (Maximum values allowed in the event of a failure, also see Figure 15, Thermal Derating curve.) Case Temperature Input Current Output Power	 T_S $I_{S,INPUT}$ $P_{S,OUTPUT}$	 150 400 700	 °C mA mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	≥ 10^9	Ω

*Refer to the front of the optocoupler section of the current catalog under Product Safety Regulations section (VDE 0884), for a detailed description.
Note: Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application.

Absolute Maximum Ratings

Parameter	Symbol	Device	Min.	Max.	Units	Note
Storage Temperature	T_S		-55	125	°C	
Operating Temperature	T_A	HCPL-4504 HCPL-0454	-55	100	°C	
		HCNW4504	-55	85		
Average Forward Input Current	$I_{F(AVG)}$			25	mA	1
Peak Forward Input Current (50% duty cycle, 1 ms pulse width)	$I_{F(PEAK)}$	HCPL-4504 HCPL-0454		50	mA	2
(50% duty cycle, 1 ms pulse width)		HCNW4504		40		
Peak Transient Input Current (≤ 1 µs pulse width, 300 pps)	$I_{F(TRANS)}$	HCPL-4504 HCPL-0454		1	A	
		HCNW4504		0.1		
Reverse LED Input Voltage (Pin 3-2)	V_R	HCPL-4504 HCPL-0454		5	V	
		HCNW4504		3		
Input Power Dissipation	P_{IN}	HCPL-4504 HCPL-0454		45	mW	3
		HCNW4504		40		
Average Output Current (Pin 6)	$I_{O(AVG)}$			8	mA	
Peak Output Current	$I_{O(PEAK)}$			16	mA	
Supply Voltage (Pin 8-5)	V_{CC}		-0.5	30	V	
Output Voltage (Pin 6-5)	V_O		-0.5	20	V	
Output Power Dissipation	P_O			100	mW	4
Lead Solder Temperature (Through-Hole Parts Only) 1.6 mm below seating plane, 10 seconds up to seating plane, 10 seconds	T_{LS}	HCPL-4504		260	°C	
		HCNW4504		260	°C	
Reflow Temperature Profile	T_{RP}	HCPL-0454 and Option 300	See **Package Outline Drawings** section			

Electrical Specifications (DC)

Over recommended temperature (T_A = 0°C to 70°C) unless otherwise specified. See note 12.

Parameter	Symbol	Device	Min.	Typ.*	Max.	Units	Test Conditions			Fig.	Note
Current Transfer Ratio	CTR	HCPL-4504	25	32	60	%	T_A = 25°C	V_O = 0.4 V	I_F = 16 mA, V_{CC} = 4.5 V	1, 2, 4	5
		HCPL-0454	21	34				V_O = 0.5 V			
		HCNW4504	23	29	60		T_A = 25°C	V_O = 0.4 V			
			19	31	63			V_O = 0.5 V			
Current Transfer Ratio	CTR	HCPL-4504	26	35	65	%	T_A = 25°C	V_O = 0.4 V	I_F = 12 mA, V_{CC} = 4.5 V	1, 2, 4	5
		HCPL-0454	22	37				V_O = 0.5 V			
		HCNW4504	25	33	65		T_A = 25°C	V_O = 0.4 V			
			21	35	68			V_O = 0.5 V			
Logic Low Output Voltage	V_{OL}	HCPL-4504 HCPL-0454		0.2	0.4	V	T_A = 25°C	I_O = 4.0 mA	I_F = 16 mA, V_{CC} = 4.5 V		
					0.5			I_O = 3.3 mA			
		HCNW4504		0.2	0.4		T_A = 25°C	I_O = 3.6 mA			
					0.5			I_O = 3.0 mA			
Logic High Output Current	I_{OH}			0.003	0.5	µA	T_A = 25°C	V_O = V_{CC} = 5.5 V	I_F = 0 mA	5	
				0.01	1		T_A = 25°C	V_O = V_{CC} = 15 V			
					50						
Logic Low Supply Current	I_{CCL}			50	200	µA	I_F = 16 mA, V_O = Open, V_{CC} = 15 V				12
Logic High Supply Current	I_{CCH}			0.02	1	µA	T_A = 25°C	I_F = 0 mA, V_O = Open, V_{CC} = 15 V			12
					2						
Input Forward Voltage	V_F	HCPL-4504 HCPL-0454		1.5	1.7	V	T_A = 25°C	I_F = 16 mA		3	
					1.8						
		HCNW4504	1.45	1.59	1.85		T_A = 25°C	I_F = 16 mA			
			1.35		1.95						
Input Reverse Breakdown Voltage	BV_R	HCPL-4504 HCPL-0454	5			V	I_R = 10 µA				
		HCNW4504	3				I_R = 100 µA, T_A = 25°C				
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$	HCPL-4504 HCPL-0454		-1.6		mV/°C	I_F = 16 mA				
		HCNW4504		-1.4							
Input Capacitance	C_{IN}	HCPL-4504 HCPL-0454		60		pF	f = 1 MHz, V_F = 0 V				
		HCNW4504		70							

*All typicals at T_A = 25°C.

AC Switching Specifications

Over recommended temperature (T_A = 0°C to 70°C) unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions		Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}		0.2	0.3	µs	T_A = 25°C	Pulse: f = 20 kHz, Duty Cycle = 10%, I_F = 16 mA, V_{CC} = 5.0 V, R_L = 1.9 kΩ, C_L = 15 pF, V_{THHL} = 1.5 V	6, 8, 9	9
			0.2	0.5					
		0.2	0.5	0.7		T_A = 25°C	Pulse: f = 10 kHz, Duty Cycle = 50%, I_F = 12 mA, V_{CC} = 15.0 V, R_L = 20 kΩ, C_L = 100 pF, V_{THHL} = 1.5 V	6, 10-14	10
		0.1	0.5	1.0					
Propagation Delay Time to Logic High at Output	t_{PLH}		0.3	0.5	µs	T_A = 25°C	Pulse: f = 20 kHz, Duty Cycle = 10%, I_F = 16 mA, V_{CC} = 5.0 V, R_L = 1.9 kΩ, C_L = 15 pF, V_{THLH} = 1.5 V	6, 8, 9	9
			0.3	0.7					
		0.3	0.8	1.1		T_A = 25°C	Pulse: f = 10 kHz, Duty Cycle = 50%, I_F = 12 mA, V_{CC} = 15.0 V, R_L = 20 kΩ, C_L = 100 pF, V_{THLH} = 2.0 V	6, 10-14	10
		0.2	0.8	1.4					
Propagation Delay Difference Between Any 2 Parts	t_{PLH}-t_{PHL}	-0.4	0.3	0.9	µs	T_A = 25°C	Pulse: f = 10 kHz, Duty Cycle = 50%, I_F = 12 mA, V_{CC} = 15.0 V, R_L = 20 kΩ, C_L = 100 pF, V_{THHL} = 1.5 V, V_{THLH} = 2.0 V	6, 10-14	15
		-0.7	0.3	1.3					
Common Mode Transient Immunity at Logic High Level Output	$\|CM_H\|$	15	30		kV/µs	T_A = 25°C, V_{CM} = 1500 V_{P-P}	V_{CC} = 5.0 V, R_L = 1.9 kΩ, C_L = 15 pF, I_F = 0 mA	7	7, 9
		15	30				V_{CC} = 15.0 V, R_L = 20 kΩ, C_L = 100 pF, I_F = 0 mA	7	8, 10
Common Mode Transient Immunity at Logic Low Level Output	$\|CM_L\|$	15	30		kV/µs	T_A = 25°C, V_{CM} = 1500 V_{P-P}	V_{CC} = 5.0 V, R_L = 1.9 kΩ, C_L = 15 pF, I_F = 16 mA	7	7, 9
		10	30				V_{CC} = 15.0 V, R_L = 20 kΩ, C_L = 100 pF, I_F = 12 mA	7	8, 10
		15	30				V_{CC} = 15.0 V, R_L = 20 kΩ, C_L = 100 pF, I_F = 16 mA	7	8, 10

*All typicals at T_A = 25°C.

Package Characteristics

Over recommended temperature (T_A = 0°C to 25°C) unless otherwise specified.

Parameter	Sym.	Device	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage†	V_{ISO}	HCPL-4504 HCPL-0454	2500			V rms	RH ≤ 50%, t = 1 min., T_A = 25°C		6, 13
		HCNW4504	5000						6, 14
		HCPL-4504 (Option 020)	5000						6, 11, 14
Input-Output Resistance	R_{I-O}	HCPL-4504 HCPL-0454		10^{12}		Ω	V_{I-O} = 500 Vdc		6
		HCNW4504	10^{12}	10^{13}			T_A = 25°C		
			10^{11}				T_A = 100°C		
Input-Output Capacitance	C_{I-O}	HCPL-4504 HCPL-0454		0.6		pF	f = 1 MHz		6
		HCNW4504		0.5	0.6				

*All typicals at T_A = 25°C..

†The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the VDE 0884 Insulation Related Characteristics Table (if applicable), your equipment level safety specification or HP Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage."

Notes:

1. Derate linearly above 70°C free-air temperature at a rate of 0.8 mA/°C (8-Pin DIP).
   Derate linearly above 85°C free-air temperature at a rate of 0.5 mA/°C (SO-8).
2. Derate linearly above 70°C free-air temperature at a rate of 1.6 mA/°C (8-Pin DIP).
   Derate linearly above 85°C free-air temperature at a rate of 1.0 mA/°C (SO-8).
3. Derate linearly above 70°C free-air temperature at a rate of 0.9 mW/°C (8-Pin DIP).
   Derate linearly above 85°C free-air temperature at a rate of 1.1 mW/°C (SO-8).
4. Derate linearly above 70°C free-air temperature at a rate of 2.0 mW/°C (8-Pin DIP).
   Derate linearly above 85°C free-air temperature at a rate of 2.3 mW/°C (SO-8).
5. CURRENT TRANSFER RATIO in percent is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100.
6. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
7. Under TTL load and drive conditions: Common mode transient immunity in a Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O > 2.0 V). Common mode transient immunity in a Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O < 0.8 V).
8. Under IPM (Intelligent Power Module) load and LED drive conditions: Common mode transient immunity in a Logic High level is the maximum tolerable dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O > 3.0 V). Common mode transient immunity in a Logic Low level is the maximum tolerable dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O < 1.0 V).
9. The 1.9 kΩ load represents 1 TTL unit load of 1.6 mA and the 5.6 kΩ pull-up resistor.
10. The R_L = 20 kΩ, C_L = 100 pF load represents an IPM (Intelligent Power Module) load.
11. See Option 020 data sheet for more information.
12. Use of a 0.1 µF bypass capacitor connected between pins 5 and 8 is recommended.
13. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 3000 V rms for 1 second (leakage detection current limit, I_{i-o} ≤ 5 µA). This test is performed before the 100% Production test shown in the VDE 0884 Insulation Related Characteristics Table, if applicable.
14. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 second (leakage detection current limit, I_{i-o} ≤ 5 µA). This test is performed before the 100% Production test shown in the VDE 0884 Insulation Related Characteristics Table, if applicable.
15. The difference between t_{PLH} and t_{PHL} between any two devices (same part number) under the same test condition. (See Power Inverter Dead Time and Propagation Delay Specifications section.)

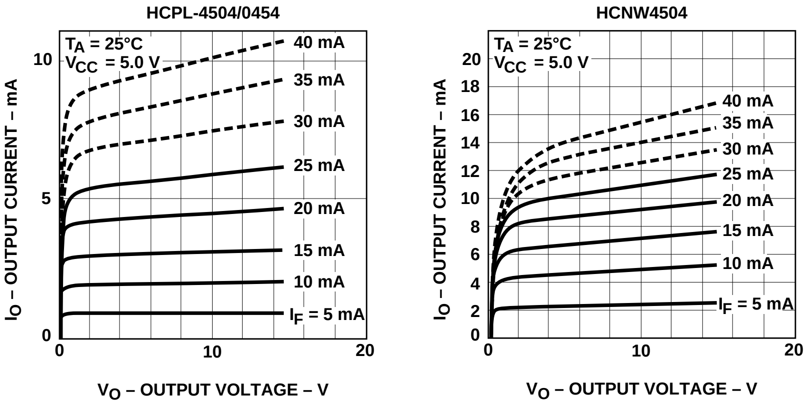


Figure 1. DC and Pulsed Transfer Characteristics.

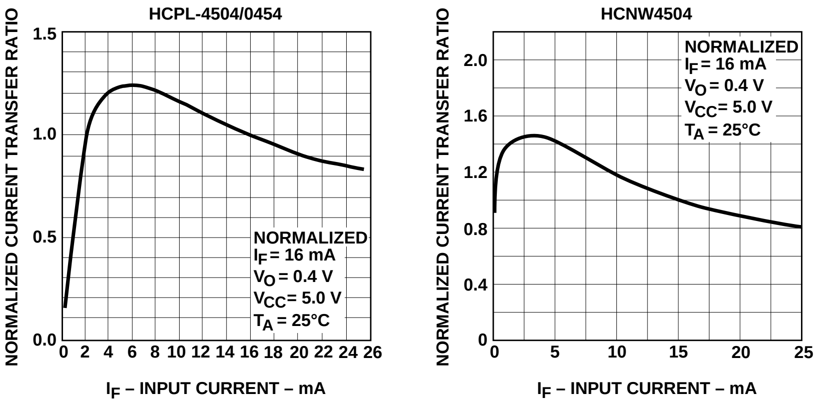


Figure 2. Current Transfer Ratio vs. Input Current.

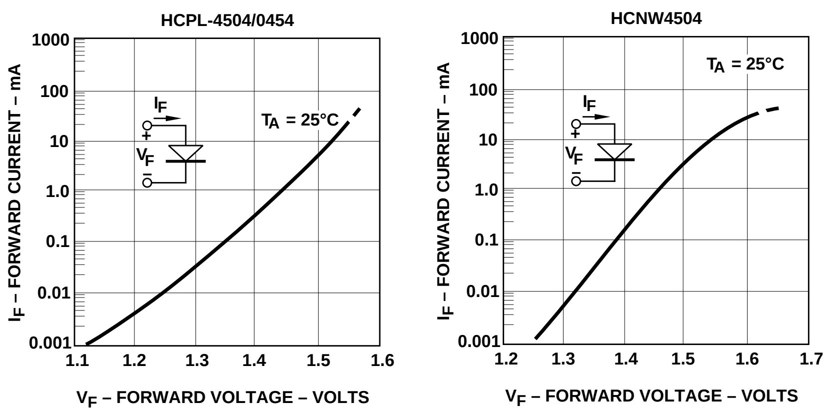
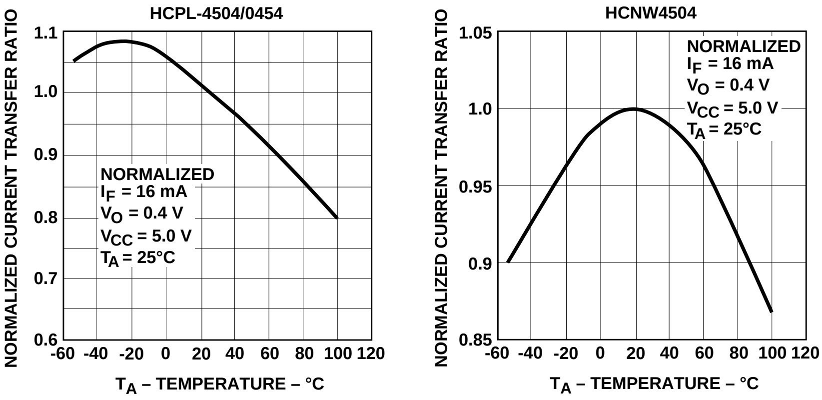


Figure 3. Input Current vs. Forward Voltage.



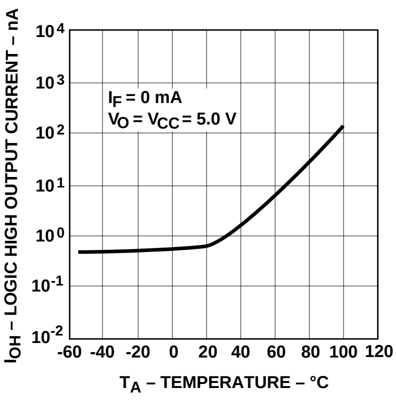


Figure 4. Current Transfer Ratio vs. Temperature.

Figure 5. Logic High Output Current vs. Temperature.

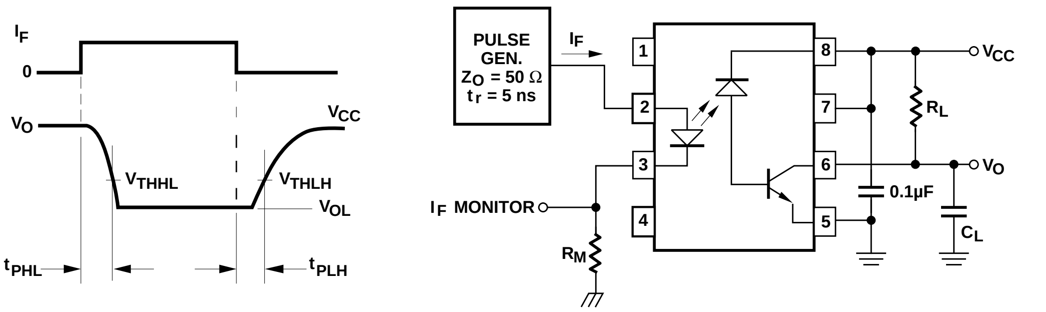


Figure 6. Switching Test Circuit.

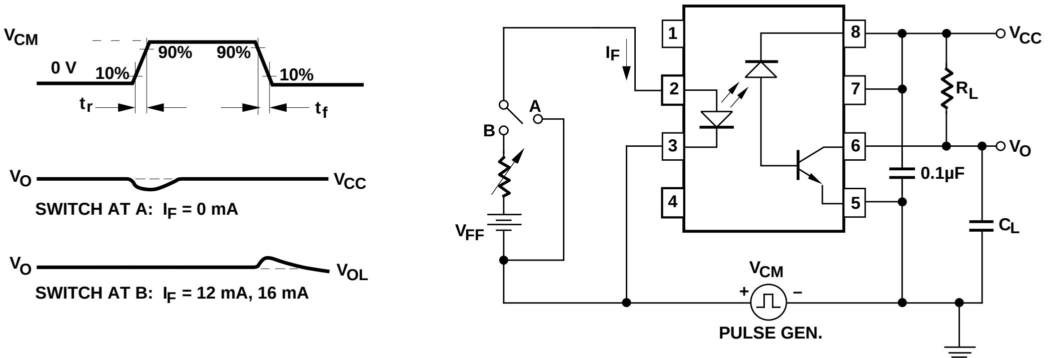


Figure 7. Test Circuit for Transient Immunity and Typical Waveforms.

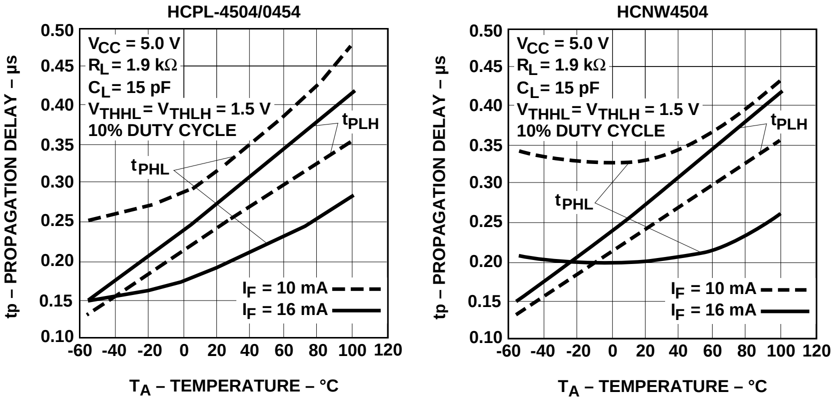


Figure 8. Propagation Delay Time vs. Temperature.

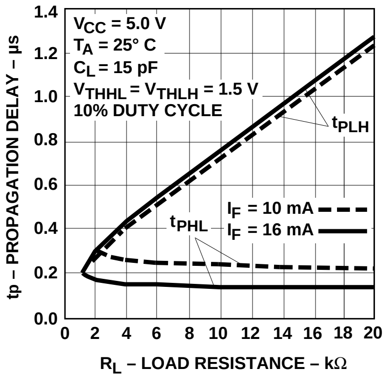


Figure 9. Propagation Delay Time vs. Load Resistance.

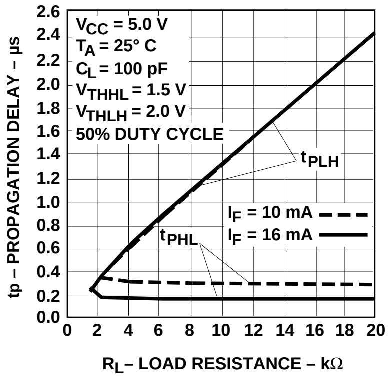


Figure 10. Propagation Delay Time vs. Load Resistance.

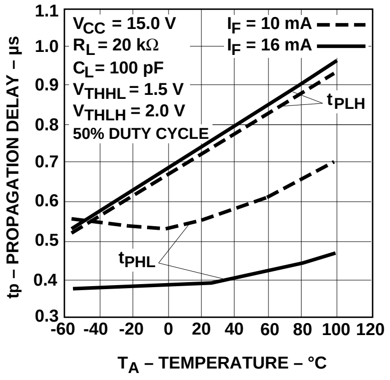


Figure 11. Propagation Delay Time vs. Temperature.

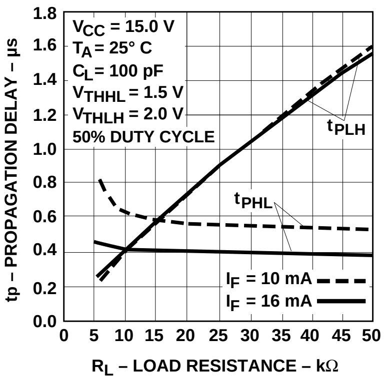


Figure 12. Propagation Delay Time vs. Load Resistance.

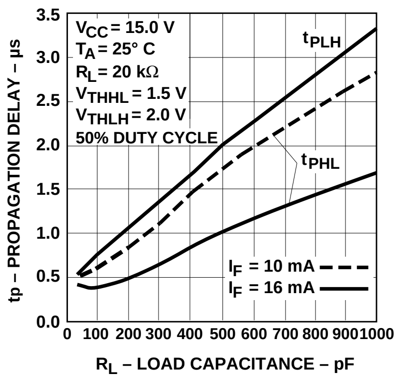


Figure 13. Propagation Delay Time vs. Load Capacitance.

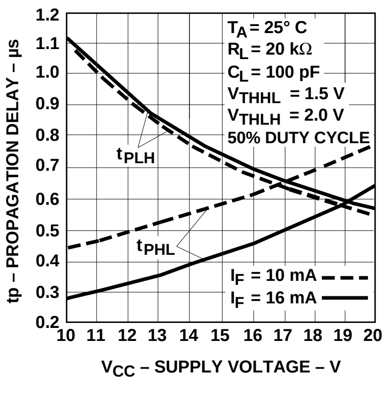


Figure 14. Propagation Delay Time vs. Supply Voltage.

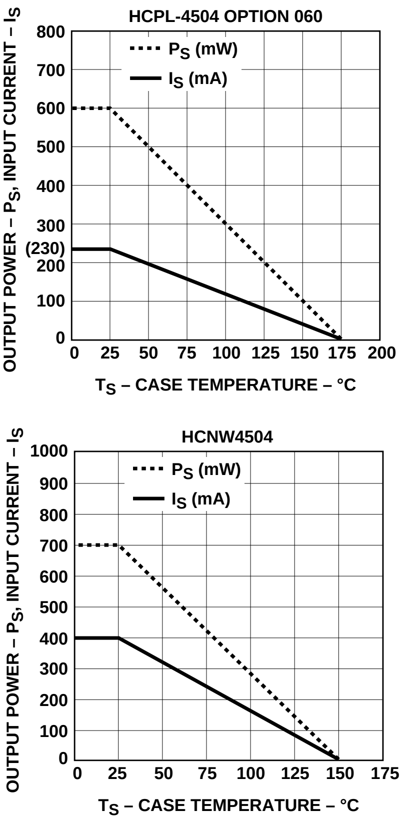


Figure 15. Thermal Derating Curve, Dependence of Safety Limiting Valve with Case Temperature per VDE 0884.

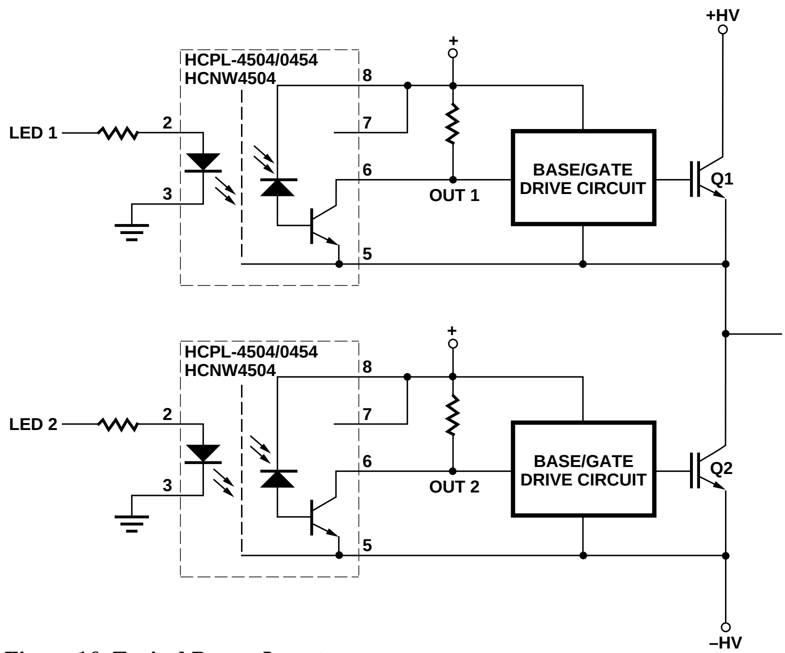


Figure 16. Typical Power Inverter.

Power Inverter Dead Time and Propagation Delay Specifications

The HCPL-4504/0454 and HCNW4504 include a specification intended to help designers minimize “dead time” in their power inverter designs. The new “propagation delay difference” specification (t_{PLH} - t_{PHL}) is useful for determining not only how much optocoupler switching delay is needed to prevent “shoot-through” current, but also for determining the best achievable worst-case dead time for a given design.

When inverter power transistors switch (Q1 and Q2 in Figure 17), it is essential that they never

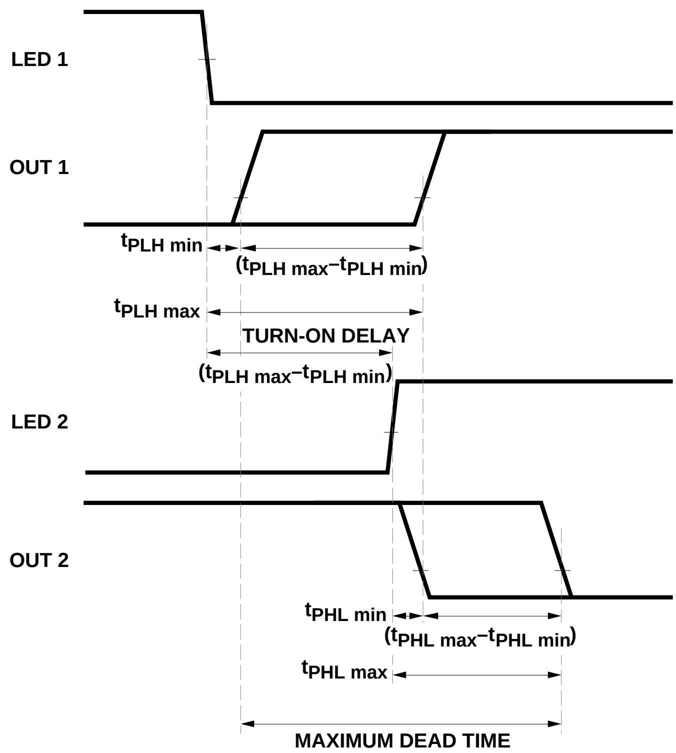


Figure 17. LED Delay and Dead Time Diagram.

conduct at the same time. Extremely large currents will flow if there is any overlap in their conduction during switching transitions, potentially damaging the transistors and even the surrounding circuitry. This "shoot-through" current is eliminated by delaying the turn-on of one transistor (Q2) long enough to ensure that the opposing transistor (Q1) has completely turned off. This delay introduces a small amount of "dead time" at the output of the inverter during which both transistors are off during switching transitions. Minimizing this dead time is an important design goal for an inverter designer.

The amount of turn-on delay needed depends on the propagation delay characteristics of the optocoupler, as well as the characteristics of the transistor base/gate drive circuit. Considering only the delay characteristics of the optocoupler (the characteristics of the base/gate drive circuit can be analyzed in the same way), it is important to know the minimum and maximum turn-on (t_{PHL}) and turn-off (t_{PLH}) propagation delay specifications, preferably over the desired operating temperature range. The importance of these specifications is illustrated in Figure 17. The waveforms labeled "LED1", "LED2", "OUT1", and "OUT2" are the input and output voltages of the optocoupler circuits driving Q1 and Q2 respectively. Most inverters are designed such that the power transistor turns on when the optocoupler LED turns on; this ensures that both power transistors will be off in the event of a power loss in the control circuit. Inverters can also be designed such that the power transistor turns off when the optocoupler LED turns on; this type of design, however, requires additional fail-safe circuitry to turn off the power transistor if an over-current condition is detected. The timing illustrated in Figure 17 assumes that the power transistor turns on when the optocoupler LED turns on.

The LED signal to turn on Q2 should be delayed enough so that an optocoupler with the very fastest turn-on propagation delay (t_{PHLmin}) will never turn on before an optocoupler with the very slowest turn-off propagation delay (t_{PLHmax}) turns off. To ensure this, the turn-on of the optocoupler should be delayed by an amount no less than (t_{PLHmax} - t_{PHLmin}), which also happens to be the maximum data sheet value for the propagation delay difference specification, (t_{PLH} - t_{PHL}). The HCPL-4504/0454 and HCNW4504 specify a maximum (t_{PLH} - t_{PHL}) of 1.3 µs over an operating temperature range of 0-70°C.

Although $(t_{PLH}-t_{PHL})_{max}$ tells the designer how much delay is needed to prevent shoot-through current, it is insufficient to tell the designer how much dead time a design will have. Assuming that the optocoupler turn-on delay is exactly equal to $(t_{PLH} - t_{PHL})_{max}$, the minimum dead time is zero (i.e., there is zero time between the turn-off of the very slowest optocoupler and the turn-on of the very fastest optocoupler).

Calculating the maximum dead time is slightly more complicated. Assuming that the LED turn-on delay is still exactly equal to $(t_{PLH} - t_{PHL})_{max}$, it can be seen in Figure 17 that the maximum dead time is the sum of the maximum difference in turn-on delay plus the maximum difference in turn-off delay,

$$[(t_{PLHmax}-t_{PLHmin})+(t_{PHLmax}-t_{PHLmin})].$$

This expression can be rearranged to obtain

$$[(t_{PLHmax}-t_{PHLmin})-(t_{PHLmin}-t_{PHLmax})],$$

and further rearranged to obtain

$$[(t_{PLH}-t_{PHL})_{max}-(t_{PLH}-t_{PHL})_{min}],$$

which is the maximum minus the minimum data sheet values of (t_{PLH}-t_{PHL}). The difference between the maximum and minimum values depends directly on the total spread in propagation delays and sets the limit on how good the worst-case dead time can be for a given design. Therefore, optocouplers with tight propagation delay specifications (and not just shorter delays or lower pulse-width distortion) can achieve short dead times in power inverters. The HCPL-4504/0454 and HCNW4504 specify a minimum (t_{PLH} - t_{PHL}) of -0.7 µs over an operating temperature range of 0-70°C, resulting in a maximum dead time of 2.0 µs when the LED turn-on delay is equal to $(t_{PLH}-t_{PHL})_{max}$, or 1.3 µs.

It is important to maintain accurate LED turn-on delays because delays shorter than $(t_{PLH} - t_{PHL})_{max}$ may allow shoot-through currents, while longer delays will increase the worst-case dead time.