



# HY51V(S)18163HG/HGL 1M x 16Bit EDO DRAM

PRELIMINARY

## DESCRIPTION

The HY51V(S)18163HG/HGL is the new generation dynamic RAM organized 1,048,576 words x 16bit. HY51V(S)18163HG/HGL has realized higher density, higher performance and various functions by utilizing advanced CMOS process technology. The HY51V(S)18163HG/HGL offers Extended Data Out Page-Mode as a high speed access mode. Multiplexed address inputs permit the HY51V(S)18163HG/HGL to be packaged in standard 400mil 42pin SOJ and 44(50) pin TSOP-II. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment.

## FEATURES

- Extended Data Out Mode capability
- Read-modify-write capability
- Multi-bit parallel test capability
- TTL(3.3V) compatible inputs and outputs
- /RAS only, CAS-before-/RAS, Hidden and self refresh(L-version) capability
- Fast access time and cycle time**
- JEDEC standard pinout
- 42pin plastic SOJ / 44(50)pin TSOP-II (400mil)
- Single power supply of 3.3V +/- 0.3V
- Battery back up operation(L-version)
- 2CAS byte control

Part No	tRAC	tCAC	tRC	tHPC
HY51V(S)18163HG/HGL-5	50ns	13ns	84ns	20ns
HY51V(S)18163HG/HGL-6	60ns	15ns	104ns	25ns
HY51V(S)18163HG/HGL-7	70ns	18ns	124ns	30ns

### Power dissipation

	50ns	60ns	70ns
Active	684mW	612mW	540mW
Standby	7.2mW(CMOS level Max) 0.83mW (L-version : Max)		

### Refresh cycle

Part No	Ref	Normal	L-part
HY51V18163HG	1K	16ms	
HY51V18163HGL	1K		128ms

## ORDERING INFORMATION

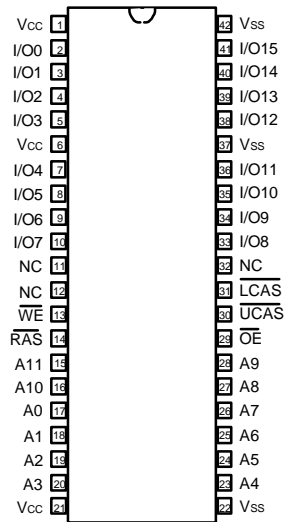
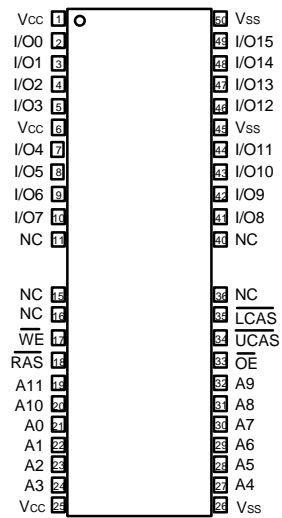
Part Number	Access Time	Package
HY51V(S)18163HGJ/HG(L)J-5 HY51V(S)18163HGJ/HG(L)J-6 HY51V(S)18163HGJ/HG(L)J-7	50ns 60ns 70ns	400mil 42pin SOJ
HY51V(S)18163HGT/HG(L)T-5 HY51V(S)18163HGT/HG(L)T-6 HY51V(S)18163HGT/HG(L)T-7	50ns 60ns 70ns	400mil 44(50)pin TSOP-II

(S) : Self refresh,

(L) : Low power

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**PIN CONFIGURATION**

**42 Pin Plastic SOJ**

**44(50) Pin Plastic TSOP-II**
**PIN DESCRIPTION**

Pin	Function
/RAS	Row Address Strobe
/UCAS, /LCAS	Column Address Strobe
/WE	Write Enable
/OE	Output Enable
A0-A9	Address Inputs
A0-A9	Refresh Address Inputs
I/O 0- I/O 15	Data Input / Output
Vcc	Power (3.3V)
Vss	Ground
NC	No connection

**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Rating	Unit
Ambient Temperature	TA	0 ~ 70	°C
Storage Temperature	TSTG	-55 ~ 125	°C
Voltage on Any Pin relative to Vss	VT	-0.5 ~ Vcc + 0.5 (Max 4.6V)	V
Voltage on Vcc relative to Vss	Vcc	-0.5 ~ 4.6	V
Short Circuit Output Current	IOUT	50	mA
Power Dissipation	PT	1	W

Note : Operation at or above absolute Maximum Ratings can adversely affect device reliability

**Recommended DC OPERATING CONDITIONS** (TA=0 to 70 °C)

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Power Supply Voltage	Vcc	3.0	3.3	3.6	V	
Input High Voltage	VIH	2.0	-	Vcc + 0.3	V	
Input Low Voltage	VIL	-0.3	-	0.8	V	

**Note : All voltages are referenced to Vss**

The supply voltage with all Vcc pins must be on the same level. The supply voltage with all Vss pins must be on the same level

**Truth Table**

/RAS	/LCAS	/UCAS	/WE	/OE	Output	Operation		Notes
H	D	D	D	D	Open	Standby		1,3
L	L	H	H	L	Valid	Lower byte	Read cycle	1, 3
L	H	L	H	L	Valid	Upper byte		
L	L	L	H	L	Valid	Word		
L	L	H	L	D	Open	Lower byte	Early write cycle	1, 2, 3
L	H	L	L	D	Open	Upper byte		
L	L	L	L	D	Open	Word		
L	L	H	L	H	Undefined	Lower byte	Delayed write cycle	1, 2, 3
L	H	L	L	H	Undefined	Upper byte		
L	L	L	L	H	Undefined	Word		
L	L	H	H to L	L to H	Valid	Lower byte	Read-modify-write Cycle	1, 3
L	H	L	H to L	L to H	Valid	Upper byte		
L	L	L	H to L	L to H	Valid	Word		
H to L	H	L	D	D	Open	Word	CBR refresh or Self refresh (L-series)	1, 3
H to L	L	H	D	D	Open	Word		
H to L	L	L	D	D	Open	Word		
L	H	H	D	D	Open	Word	/RAS only refresh cycle	1, 3
L	L	L	H	H	Open	Read cycle (Output disabled)		1, 3

**Notes :**

1. H : High ( inactive) L : Low ( active) D : H or L
2.  $twcs \geq 0ns$  Early write cycle  
 $twcs < 0ns$  Delayed write cycle
3. Mode is determined by the OR function of the /UCAS and /LCAS (mode is set by earliest of /UCAS and /LCAS active edge and reset by the latest of /UCAS and /LCAS inactive edge), However write operation and output High-Z control are done independently by each /UCAS, /LCAS  
 ex) if /RAS = H to L, /UCAS = H, /LCAS = L, then /CAS-before-/RAS refresh cycle is selected

**DC CHARACTERISTICS** ( $V_{CC} = 3.3V \pm 10\%$ ,  $T_A = 0$  to  $70^\circ C$ )

Symbol	Parameter	Min	Max	Unit	Note	
VOH	Output Level Output Level voltage( $I_{out} = -2mA$ )	2.4	$V_{CC}$	V		
VOL	Output Level Output Level voltage( $I_{out} = 2mA$ )	0	0.4	V		
ICC1	Operating current Average power supply operating current ( $/RAS, /CAS$ Cycling : $t_{RC} = t_{RC \min}$ )	50ns	-	190	mA	1, 2
		60ns	-	170		
		70ns	-	150		
ICC2	Standby current (TTL interface) Power supply standby current ( $/RAS, /CAS = V_{IH}$ , $D_{out} = High-Z$ )	-	2	mA		
ICC3	$/RAS$ only refresh current Average power supply current $/RAS$ only refresh mode ( $t_{RC} = t_{RC \min}$ )	50ns	-	190	mA	2
		60ns	-	170		
		70ns	-	150		
ICC4	EDO page mode current Average power supply current EDO page mode ( $t_{PC} = t_{PC \min}$ )	50ns	-	185	mA	1, 3
		60ns	-	165		
		70ns	-	145		
ICC5	CMOS interface ( $/RAS, /CAS \geq V_{CC} - 0.2V$ , $D_{out} = High-Z$ )	-	1	mA		
	Standby current (L-version)	-	150	$\mu A$	5	
ICC6	$/CAS$ -before- $/RAS$ refresh current ( $t_{RC} = t_{RC \min}$ )	50ns	-	190	mA	
		60ns	-	170		
		70ns	-	150		
ICC7	Battery back up operating current (standby with CBR ref.) (CBR refresh, $t_{RC} = 31.3\mu s$ , $t_{RAS} \leq 0.3\mu s$ , $D_{out} = High-Z$ , CMOS interface)	-	400	$\mu A$	4, 5	
ICC8	Standby current ( $RAS = V_{IH}$ , $/CAS = V_{IL}$ , $D_{out} = Enable$ )	-	5	mA	1	
ICC9	Self refresh current ( $/RAS, /CAS \leq 0.2V$ , $D_{out} = High-Z$ )	-	250	$\mu A$	5	
II(L)	Input leakage current, Any input ( $0V \leq V_{in} \leq 4.6V$ )	-10	10	$\mu A$		
IO(L)	Output leakage current, ( $D_{out}$ is disabled, $0V \leq V_{out} \leq 4.6V$ )	-10	10	$\mu A$		

**Note :**

1.  $I_{CC}$  depends on output load condition when the device is selected,  $I_{CC(max)}$  is specified at the output open condition
2. Address can be changed once or less while  $/RAS = V_{IL}$
3. Address can be changed once or less while  $/CAS = V_{IH}$
4.  $/CAS = L$  ( $\leq 0.2$ ) while  $/RAS = L$  ( $\leq 0.2$ )
5. L-Version

**CAPACITANCE** ( $V_{CC}=3.3V \pm 10\%$ ,  $T_A=25^\circ C$ )

Parameter	Symbol	Min.	Max	Unit	Note
Input capacitance (Address)	CI1	-	5	pF	1
Input capacitance (Clocks)	CI2	-	7	pF	1
Output capacitance (Data-in, Data-out)	CI/O	-	7	pF	1, 2

Note : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.  
 2. /CAS =  $V_{IH}$  to disable  $D_{out}$

**AC CHARACTERISTICS** ( $V_{CC}=3.3V \pm 10\%$ ,  $T_A=0\sim 70^\circ C$ , Note 1, 2, 18,19,20)

**Test Condition**

- Input rise and fall times = 2ns
- Input timing reference levels :  $V_{IL}=0V$ ,  $V_{IH}=3.0V$
- Input timing reference level :  $V_{IL}/V_{IH} = 0.8/2.0V$
- Output timing reference level :  $V_{OL}/V_{OH}=0.8/0.2V$
- Output load : 1 TTL gate + CL (100pF)  
( including scope and jig )

**Read, Write, Read-modify-Write and Refresh Cycle**

Parameter	Symbol	-50		-60		-70		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	84	-	104	-	124	-	ns	
/RAS precharge time	tRP	30	-	40	-	50	-	ns	
/CAS precharge time	tCP	8	-	10	-	13	-	ns	
/RAS pulse width	tRAS	50	10,000	60	10,000	70	10,000	ns	
/CAS pulse width	tCAS	8	10,000	10	10,000	13	10,000	ns	
Row address set-up time	tASR	0	-	0	-	0	-	ns	
Row address hold time	tRAH	8	-	10	-	10	-	ns	
Column address set-up time	tASC	0	-	0	-	0	-	ns	21
Column address hold time	tCAH	8	-	10	-	13	-	ns	21
/RAS to /CAS delay time	tRCD	12	37	14	45	14	52	ns	3
/RAS to Column address delay time	tRAD	10	25	12	30	12	35	ns	4
/RAS hold time	tRSH	10	-	13	-	13	-	ns	
/CAS hold time	tCSH	35	-	40	-	45	-	ns	23
/CAS to /RAS precharge time	tCRP	5	-	5	-	5	-	ns	22

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Parameter	Symbol	-50		-60		-70		Unit	Note
		Min	Max	Min	Max	Min	Max		
/OE to Din delay time	tOED	13	-	15	-	18	-	ns	5
/OE delay time from Din	tDZO	0	-	0	-	0	-	ns	6
/CAS delay time from Din	tDZC	0	-	0	-	0	-	ns	6
Transition time ( Rise and Fall)	tT	2	50	2	50	2	50	ns	7
Refresh period	tREF	-	16	-	16	-	16	ms	1K Ref.
Refresh period (L-version)		-	128	-	128	-	128	ms	1K Ref.

**Read Cycle**

Parameter	Symbol	-50		-60		-70		Unit	Note
		Min	Max	Min	Max	Min	Max		
Access time from /RAS	tRAC	-	50	-	60	-	70	ns	8,9
Access time from /CAS	tCAC	-	13	-	15	-	18	ns	9,10,17
Access time from column address	tAA	-	25	-	30	-	35	ns	9,11,17
Access time from /OE	tOEA	-	13	-	15	-	18	ns	9
Read command set-up time	tRCS	0	-	0	-	0	-	ns	21
Read command hold time to /CAS	tRCH	0	-	0	-	0	-	ns	12,22
Read command hold time to /RAS	tRRH	5	-	5	-	5	-	ns	12
Column address to /RAS lead time	tRAL	25	-	30	-	35	-	ns	
Column address to /CAS lead time	tCAL	15	-	18	-	23	-	ns	
/CAS to output in low-Z	tCLZ	0	-	0	-	0	-	ns	
Output data hold time	tOH	3	-	3	-	3	-	ns	27
Output data hold time from /OE	tOHO	3	-	3	-	3	-	ns	
Output buffer turn off time	tOFF	-	13	-	15	-	15	ns	13,27
Output buffer turn off time to /OE	tOEZ	-	13	-	15	-	15	ns	13
/CAS to Din delay time	tCDD	13	-	15	-	18	-	ns	5
Read command hold time from /RAS	tRCHR	50	-	60	-	70	-	ns	
Output data hold time from /RAS	tOHR	3	-	3	-	3	-	ns	27
Output buffer turn-off time to /RAS	tOFR	-	13	-	15	-	15	ns	27
Output buffer turn off time to /WE	tWEZ	-	13	-	15	-	15	ns	
/WE to DIN delay time	tWDD	13	-	15	-	18	-	ns	
/RAS to DIN delay time	tRDD	13	-	15	-	18	-	ns	

**Write Cycle**

Parameter	Symbol	-50		-60		-70		Unit	Note
		Min	Max	Min	Max	Min	Max		
Write command set-up time	tWCS	0	-	0	-	0	-	ns	14,21
Write command hold time	tWCH	8	-	10	-	13	-	ns	21
Write command pulse width	tWP	8	-	10	-	10	-	ns	
Write command to /RAS lead time	tRWL	8	-	10	-	13	-	ns	
Write command to /CAS lead time	tCWL	8	-	10	-	13	-	ns	23
Data-in set-up time	tDS	0	-	0	-	0	-	ns	15,23
Data-in hold time	tDH	8	-	10	-	13	-	ns	15,23

**Read-Modify-Write Cycle**

Parameter	Symbol	-50		-60		-70		Unit	Note
		Min	Max	Min	Max	Min	Max		
Read-modify-write cycle time	tRWC	111	-	136	-	161	-	ns	
/RAS to /WE delay time	tRWD	67	-	79	-	92	-	ns	14
/CAS to /WE delay time	tCWD	30	-	34	-	40	-	ns	14
Column address to /WE delay time	tAWD	42	-	49	-	57	-	ns	14
/OE hold time from /WE	tOEH	13	-	15	-	18	-	ns	

**Refresh cycle**

Parameter	Symbol	-50		-60		-70		Unit	Note
		Min	Max	Min	Max	Min	Max		
/CAS set-up time ( /CAS-before-/RAS Refresh Cycle)	tCSR	5	-	5	-	5	-	ns	21
/CAS hold time ( /CAS-before-/RAS Refresh Cycle)	tCHR	8	-	10	-	10	-	ns	22
/RAS precharge to /CAS hold time ( /CAS-before-/RAS Refresh Cycle)	tRPC	5	-	5	-	5	-	ns	21



**EDO Page Mode Cycle**

Parameter	Symbol	-50		-60		-70		Unit	Note
		Min	Max	Min	Max	Min	Max		
EDO mode cycle time	tHPC	20	-	25	-	30	-	ns	25
EDO mode /RAS pulse width	tRASP	-	100K	-	100K	-	100K	ns	16
Access time from /CAS precharge	tACP	-	30	-	35	-	40	ns	9,17,22
/RAS hold time from /CAS precharge	tRHCP	30	-	35	-	40	-	ns	
Output data hold time from /CAS low	tDOH	3	-	3	-	3	-	ns	9
/CAS hold time referred /OE	tCOL	8	-	10	-	13	-	ns	
/CAS to /OE setup time	tCOP	5	-	5	-	5	-	ns	
Read command hold time from /CAS precharge	tRHCP	30	-	35	-	40	-	ns	

**EDO Page Mode Read-Modify-Write Cycle**

Parameter	Symbol	-50		-60		-70		Unit	Note
		Min	Max	Min	Max	Min	Max		
EDO Page read-modify-write cycle time	tHPRWC	57	-	68	-	79	-	ns	
EDO mode read-modify-write cycle /CAS precharge to /WE delay time	tCPW	45	-	54	-	62	-	ns	14,22

**Self Refresh Mode(L-version)**

Parameter	Symbol	-50		-60		-70		Unit	Note
		Min	Max	Min	Max	Min	Max		
/RAS pulse width (self refresh)	tRASS	100	-	100	-	100	-	us	29
/RAS precharge time(self refresh)	tRPS	90	-	110	-	130	-	ns	
/CAS hold time(self refresh)	tCHS	-50	-	-50	-	-50	-	ns	

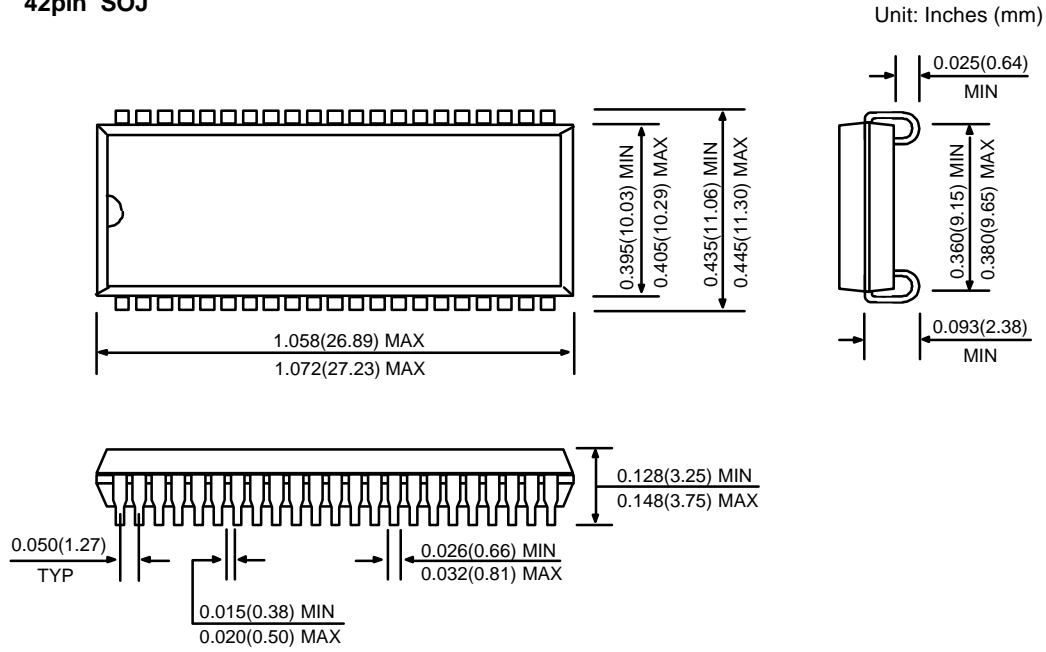
**Notes :**

1. AC measurements assume  $t_T = 2\text{ns}$
2. AC initial pause of 200us is required after power up followed by a minimum of eight initialization cycles ( any combination of cycles containing /RAS-only refresh or /CAS-before-/RAS refresh)  
If the internal refresh counter is used, a minimum of eight /CAS-before-/RAS refresh cycle are required.
3. Operation with the  $t_{RCD}(\text{max})$  limit insures that  $t_{RAC}(\text{max})$  can be met,  $t_{RCD}(\text{max})$  is specified as a reference point only : if  $t_{RCD}$  is greater than the specified  $t_{RCD}(\text{max})$  limit, then access time is controlled exclusively by  $t_{CAC}$ .
4. Operation with the  $t_{RAD}(\text{max})$  limit insures that  $t_{RAC}(\text{max})$  can be met,  $t_{RAD}(\text{max})$  is specified as a reference point only : if  $t_{RAD}$  is greater than the specified  $t_{RAD}(\text{max})$  limit, then access time is controlled exclusively by  $t_{AA}$ .
5. Either  $t_{ODD}$  or  $t_{CDD}$  must be satisfied.
6. Either  $t_{DZO}$  or  $t_{DZC}$  must be satisfied.
7.  $V_{IH}(\text{min})$  and  $V_{IL}(\text{max})$  are reference levels for measuring timing of input signals, also transition times are measured between  $V_{IH}(\text{min})$  and  $V_{IL}(\text{max})$
8. Assumes that  $t_{RCD} \leq t_{RCD}(\text{max})$  and  $t_{RAD} \leq t_{RAD}(\text{max})$ . If  $t_{RCD}$  or  $t_{RAD}$  is greater than the maximum recommended value shown in this table,  $t_{RAC}$  exceeds the value shown
9. Measured with a load circuit equivalent to 1 TTL loads and 100pF.(  $V_{OH}=2.0\text{V}$ ,  $V_{OL}=0.8\text{V}$ )
10. Assumes that  $t_{RCD} \geq t_{RCD}(\text{max})$  and  $t_{RCD} + t_{CAC}(\text{max}) \geq t_{RAD} + t_{AA}(\text{max})$
11. Assumes that  $t_{RAD} \geq t_{RAD}(\text{max})$  and  $t_{RCD} + t_{CAC}(\text{max}) \leq t_{RAD} + t_{AA}(\text{max})$
12. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycles
13.  $t_{OFF}(\text{max})$ ,  $t_{OEZ}(\text{max})$ ,  $t_{OFR}(\text{max})$  and  $t_{WEZ}(\text{max})$  define the time at which the outputs achieve the open circuit condition and is not referenced to output voltage levels
14.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$ ,  $t_{AWD}$  and  $t_{CPW}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only : If  $t_{WCS} \geq t_{WCS}(\text{min})$ , the cycle is an early write cycle and the data out pin will remain open circuit(high impedance) throughout the entire cycle :  
If  $t_{RWD} \geq t_{RWD}(\text{min})$ ,  $t_{CWD} \geq t_{CWD}(\text{min})$ ,  $t_{AWD} \geq t_{AWD}(\text{min})$ , the cycle is a read-modify-write and the data output will contain data read from the selected cell : if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. These parameters are referenced to /CAS leading edge in early write cycles and to /WE leading edge in delayed write or read-modify-write cycles
16.  $t_{RASP}$  defines /RAS pulse width in EDO page mode cycles

17. Access time is determined by the longest among  $t_{AA}$  or  $t_{CAC}$  or  $t_{ACP}$
18. In delayed write or read-modify-write cycles, OE must disable output buffer prior to applying data to the device, After /RAS is reset, if  $t_{OE} \geq t_{CWL}$ , the I/O pin will remain open circuit (high impedance)  
If  $t_{OE} < t_{CWL}$ , invalid data will be out at each I/O
19. When both /UCAS and /LCAS go low at the same time, all 16 bit data are written into the device  
/UCAS and /LCAS cannot be staggered within the same write / read cycles.
20. All the Vcc and Vss pins shall be supplied with the same voltages
21.  $t_{ASC}$ ,  $t_{CAH}$ ,  $t_{RCS}$ ,  $t_{WCS}$ ,  $t_{WCH}$ ,  $t_{CSR}$  and  $t_{RPC}$  are determined by the earlier falling edge of /UCAS or /LCAS.
22.  $t_{CRP}$ ,  $t_{CHR}$ ,  $t_{RCH}$ ,  $t_{ACP}$  and  $t_{CPW}$  are determined by the later rising edge of /UCAS or /LCAS.
23.  $t_{CWL}$ ,  $t_{DH}$ ,  $t_{DS}$  and  $t_{CSH}$  should be satisfied by both /UCAS and /LCAS
24.  $t_{CP}$  is determined by that time the both /UCAS and /LCAS are high.
25.  $t_{HPC}(\min)$  can be achieved during a series of EDO page mode write cycles or EDO mode write cycles  
It both write and read operation are mixed in a EDO mode /RAS cycle(EDO mode mix cycle(1,2))  
minimum value of /CAS cycle( $t_{CAS} + t_{CP} + 2t_T$ ) becomes greater than the specified  $t_{HPC}(\min)$  value.  
The value of /CAS cycle time of mixed EDO mode is shown in EDO mode mix cycle (1) and (2)
26. When output buffers are enabled once, sustain the low impedance state until valid data is obtained  
When output buffer is turned on and off within a very short time, generally it causes large Vcc/Vss line noise, which causes to degrade  $V_{IH \min}$  /  $V_{IL \max}$  level
27. Data output turns off and becomes high impedance from later rising edge of /RAS and /CAS.  
Hold time and turn off time are specified by the timing specification of later rising edge of /RAS and /CAS between  $t_{OHR}$  and  $t_{OH}$ , and between  $t_{OFR}$  and  $t_{OFF}$
28. EDO High-Z control by /OE or /WE. /OE rising edge disables data outputs. When /OE goes high during /CAS high, the data will not come out until next /CAS access. When /WE goes low during /CAS high, the data will not come out until next /CAS access
29. Please do not use  $t_{RASS}$  timing,  $10\mu s \leq t_{RASS} \leq 100\mu s$ . During this period, The device is in transition state from normal operation mode to self refresh mode. If  $t_{RASS} \geq 100\mu s$ , then RAS
30. H or L ( H :  $V_{IH}(\min) \leq V_{IN} \leq V_{IH}(\max)$ , L :  $V_{IL}(\min) \leq V_{IN} \leq V_{IL}(\max)$ )

## PACKAGE INFORMATION

### 42pin SOJ



### 44(50)pin TSOP II

