IS62LV12816L
IS62LV12816LL

128K x 16 LOW VOLTAGE, ULTRA LOW POWER CMOS STATIC RAM

FEATURES

- High-speed access times: 55, 70, 100 ns
- CMOS low power operation
  - -- 120 mW (typical) operating
  - -- 6 μW (typical) CMOS standby
- TTL compatible interface levels
- Single 2.7V-3.6V Vcc power supply
- Fully static operation: no clock or refresh required
- Three state outputs
- Data control for upper and lower bytes
- Industrial temperature available
- Available in the 44-pin TSOP-2 and 48-pin 6*8mm TF-BGA

DESCRIPTION

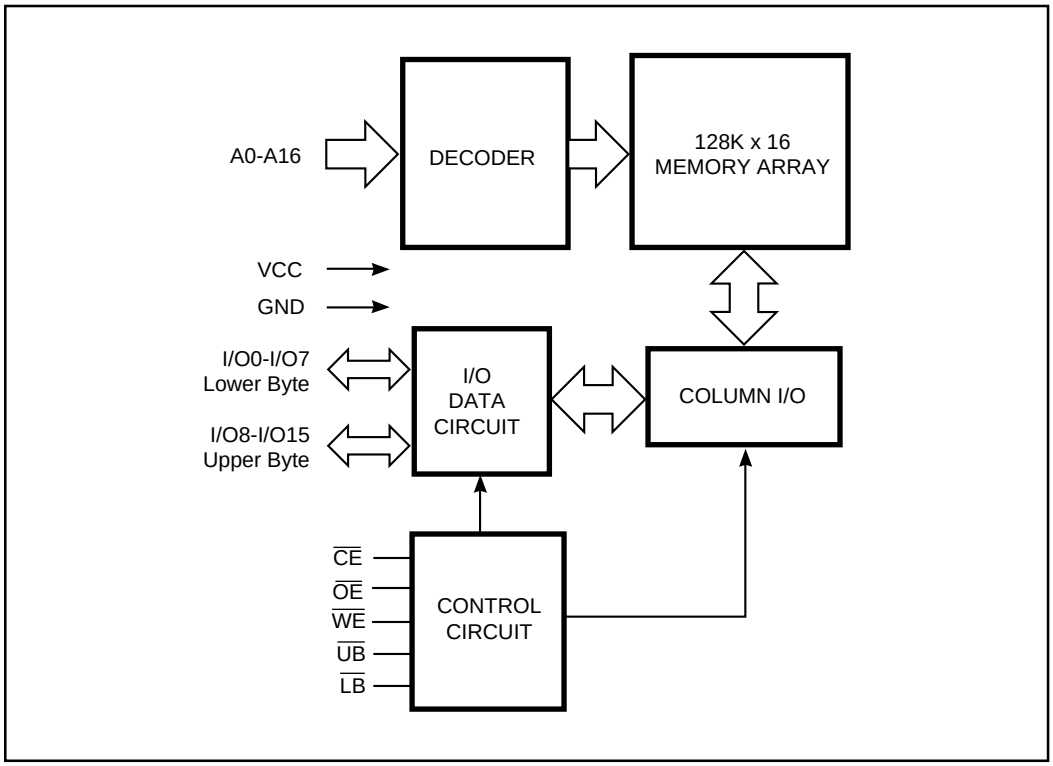
The *ICSI* IS62LV12816L and IS62LV12816LL are high-speed, 2.097,152-bit static RAMs organized as 131,072 words by 16 bits. They are fabricated using *ICSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When $\overline{CE}$ is HIGH (deselected) or when $\overline{CE}$ is low and both $\overline{LB}$ and $\overline{UB}$ are HIGH, the device assumes a standby mode at which the power dissipation can be reduced by using CMOS input levels.

Easy memory expansion is provided by using Chip Enable Output and Enable inputs, $\overline{CE}$ and $\overline{OE}$. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory. A data byte allows Upper Byte ($\overline{UB}$) and Lower Byte ($\overline{LB}$) access.

The IS62LV12816L and IS62LV12816LL are packaged in the JEDEC standare 44-pin 400mil TSOP-2 and 48-pin 6*8mm TF-BGA.

FUNCTIONAL BLOCK DIAGRAM



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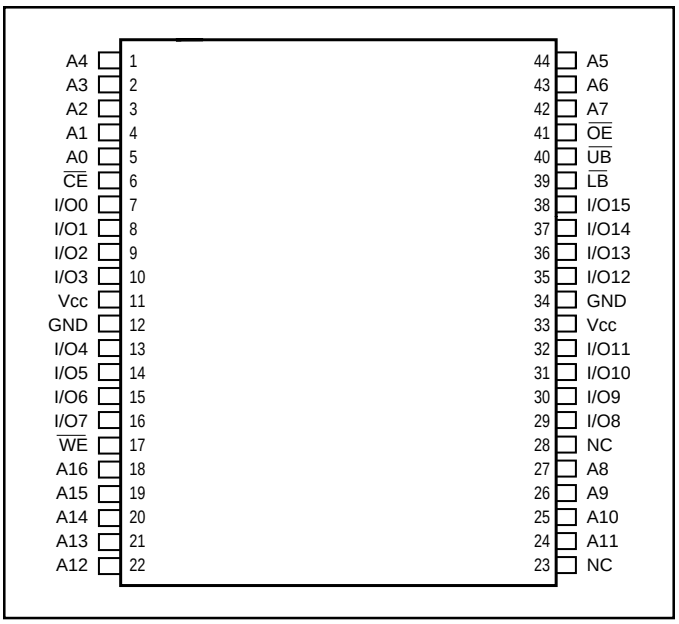
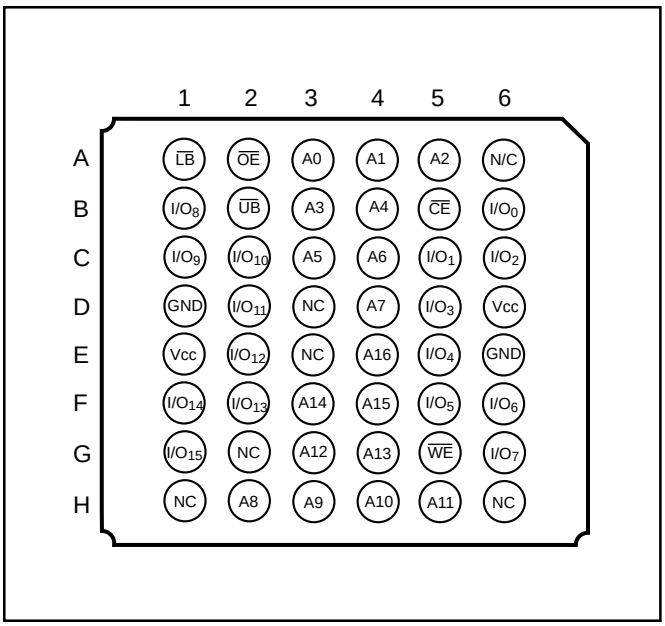
PIN CONFIGURATIONS

44-Pin TSOP-2



48-Pin TF-BGA



PIN DESCRIPTIONS

A0-A16	Address Inputs
I/O0-I/O15	Data Input/Output
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input

$\overline{LB}$	Lower-byte Control (I/O0-I/O7)
$\overline{UB}$	Upper-byte Control (I/O8-I/O15)
NC	No Connection
Vcc	Power
GND	Ground

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O PIN I/O0/-I/O7	I/O PIN I/O8-I/O15	Vcc Current
Not Selected	X	H	X	X	X	High-Z	High-Z	I_{SB1}, I_{SB2}
	X	L	X	H	H	High-Z	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	X	X	High-Z	High-Z	I_{CC}
	X	L	X	H	H	High-Z	High-Z	I_{SB}
Read	H	L	L	L	H	D_{OUT}	High-Z	I_{CC}
	H	L	L	H	L	High-Z	D_{OUT}	
	H	L	L	L	L	D_{OUT}	D_{OUT}	
Write	L	L	X	L	H	D_{IN}	High-Z	I_{CC}
	L	L	X	H	L	High-Z	D_{IN}	
	L	L	X	L	L	D_{IN}	D_{IN}	

OPERATING RANGE

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	2.7V - 3.6V
Industrial	–40°C to +85°C	2.7V - 3.6V

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to Vcc + 0.5	V
T_{BIAS}	Temperature Under Bias	–40 to +85	°C
V_{CC}	Vcc related to GND	–0.3 to +4.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.0	W

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –1 mA	2.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 2.1 mA	—	0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC} + 0.2	V
V_{IL}(1)	Input LOW Voltage(1)		–0.2	0.4	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{CC}	–1	1	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{CC}, Outputs Disabled	–1	1	µA

Notes:
1. V_{IL}(min.) = –2.0V for pulse width less than 10 ns.

CAPACITANCE(1)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0.4V to 2.2V
Input Rise and Fall Times	5 ns
Input and Output Timing and Reference Level	1.3V
Output Load	See Figures 1 and 2

AC TEST LOADS

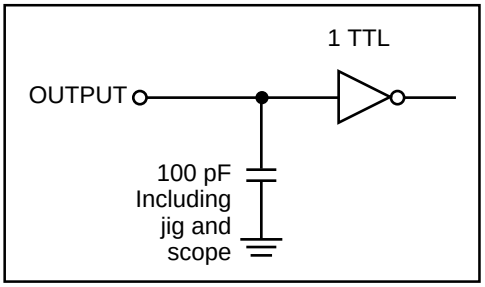


Figure 1

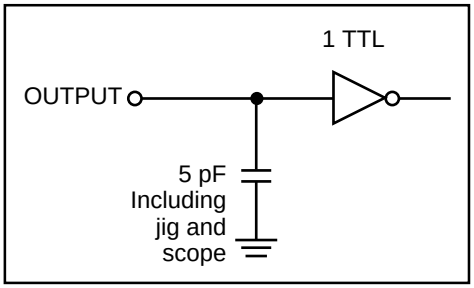


Figure 2

IS62LV12816L POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		-55 Min.	-55 Max.	-70 Min.	-70 Max.	-100 Min.	-100 Max.	Unit
I_{CC}	Vcc Dynamic Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX}	Com.	—	40	—	30	—	20	mA
			Ind.	—	45	—	35	—	25	
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{CC} = Max., V_{IN} = V_{IH} or V_{IL}, $\overline{CE} \geq V_{IH}$, f = 0	Com.	—	0.4	—	0.4	—	0.4	mA
			Ind.	—	1.0	—	1.0	—	1.0	
	OR									
	ULB Control	V_{CC} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CE}$ = V_{IL}, f = 0, $\overline{UB}$ = V_{IH}, $\overline{LB}$ = V_{IH}								
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{CC} = Max., $\overline{CE} \geq V_{CC}$ – 0.2V, $V_{IN} \geq V_{CC}$ – 0.2V, or $V_{IN} \leq$ 0.2V, f = 0	Com.	—	35	—	35	—	35	µA
			Ind.	—	50	—	50	—	50	
	OR									
	ULB Control	V_{CC} = Max., $\overline{CE}$ = V_{IL} $V_{IN} \leq$ 0.2V, f = 0, $\overline{UB}$ / $\overline{LB}$ = V_{CC} – 0.2V								

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

IS62LV12816LL POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		-55 Min.	-55 Max.	-70 Min.	-70 Max.	-100 Min.	-100 Max.	Unit
I_{CC}	Vcc Dynamic Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX}	Com.	—	40	—	30	—	20	mA
			Ind.	—	45	—	35	—	25	
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{CC} = Max., $V_{IN} = V_{IH}$ or V_{IL}, $\overline{CE} \geq V_{IH}$, f = 0	Com.	—	0.4	—	0.4	—	0.4	mA
			Ind.	—	1.0	—	1.0	—	1.0	
	OR									
	ULB Control	V_{CC} = Max., $V_{IN} = V_{IH}$ or V_{IL}, $\overline{CE} = V_{IL}$, f = 0, $\overline{UB} = V_{IH}$, $\overline{LB} = V_{IH}$								
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{CC} = Max., f = 0, $\overline{CE} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$, or $V_{IN} \leq 0.2V$, f = 0	Com.	—	10	—	10	—	10	µA
			Ind.	—	15	—	15	—	15	
	OR									
	ULB Control	V_{CC} = Max., $\overline{CE} = V_{IL}$, $V_{IN} \leq 0.2V$, f = 0, $\overline{UB}$ / $\overline{LB} = V_{CC} - 0.2V$								

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

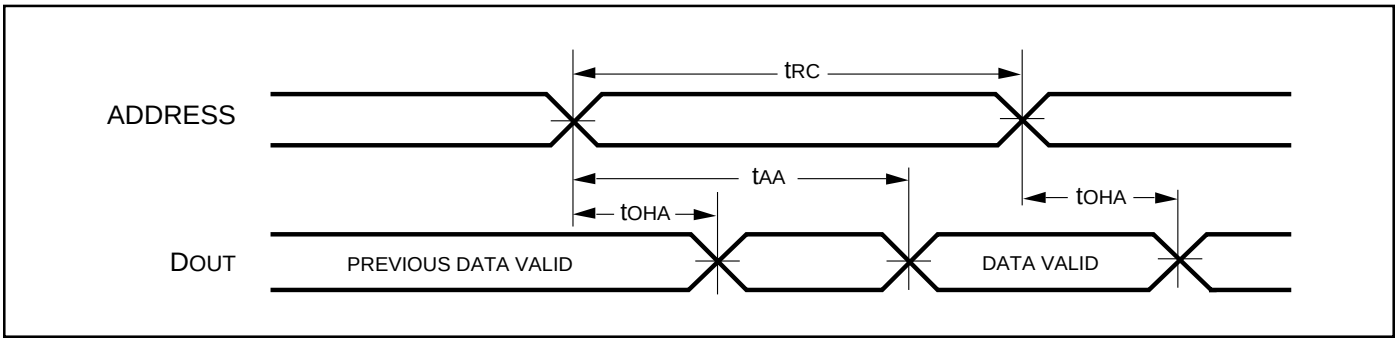
READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	-55 Min.	-55 Max.	-70 Min.	-70 Max.	-100 Min.	-100 Max.	Unit
t_{RC}	Read Cycle Time	55	—	70	—	100	—	ns
t_{AA}	Address Access Time	—	55	—	70	—	100	ns
t_{OHA}	Output Hold Time	10	—	10	—	15	—	ns
t_{ACE}	$\overline{CE}$ Access Time	—	55	—	70	—	100	ns
t_{DOE}	$\overline{OE}$ Access Time	—	30	—	35	—	50	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	—	20	—	25	—	30	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	5	—	5	—	5	—	ns
t_{HZCE}[2]	$\overline{CE}$ to High-Z Output	0	20	0	25	0	30	ns
t_{LZCE}[2]	$\overline{CE}$ to Low-Z Output	10	—	10	—	10	—	ns
t_{BA}	$\overline{LB}$, $\overline{UB}$ Access Time	—	55	—	70	—	100	ns
t_{HZB}	$\overline{LB}$, $\overline{UB}$ o High-Z Output	0	25	0	25	0	35	ns
t_{LZB}	$\overline{LB}$. $\overline{UB}$ to Low-Z Output	0	—	0	—	0	—	ns

Notes:
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.3V, input pulse levels of 0.4V to 2.2V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

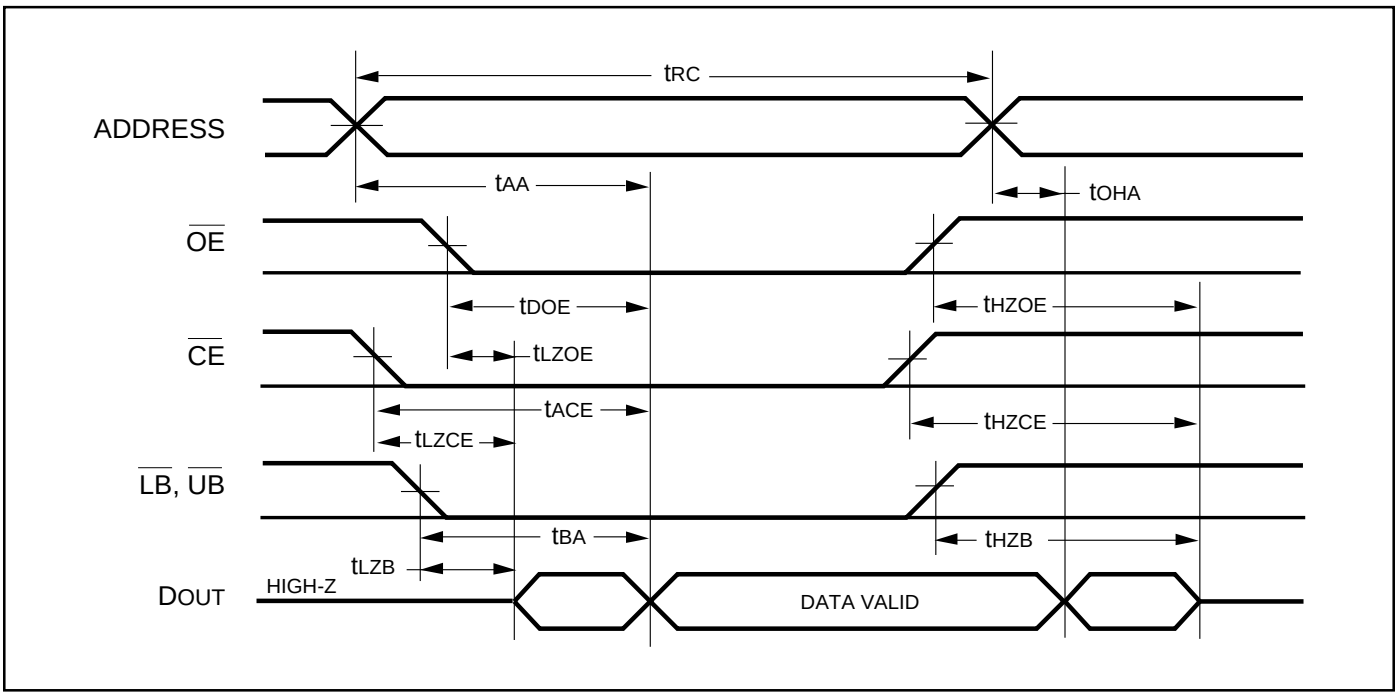
AC TEST LOADS

READ CYCLE NO.1[1,2] (Address Controlled) ($\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{UB}$ or $\overline{LB}$ = V_{IL})



AC WAVEFORMS

READ CYCLE NO. 2[1,3] ($\overline{CS}$, $\overline{OE}$, AND $\overline{UB}$/$\overline{LB}$ Controlled)



Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{UB}$, or $\overline{LB}$ = V_{IL}.
3. Address is valid prior to or coincident with $\overline{CE}$ LOW transitions.

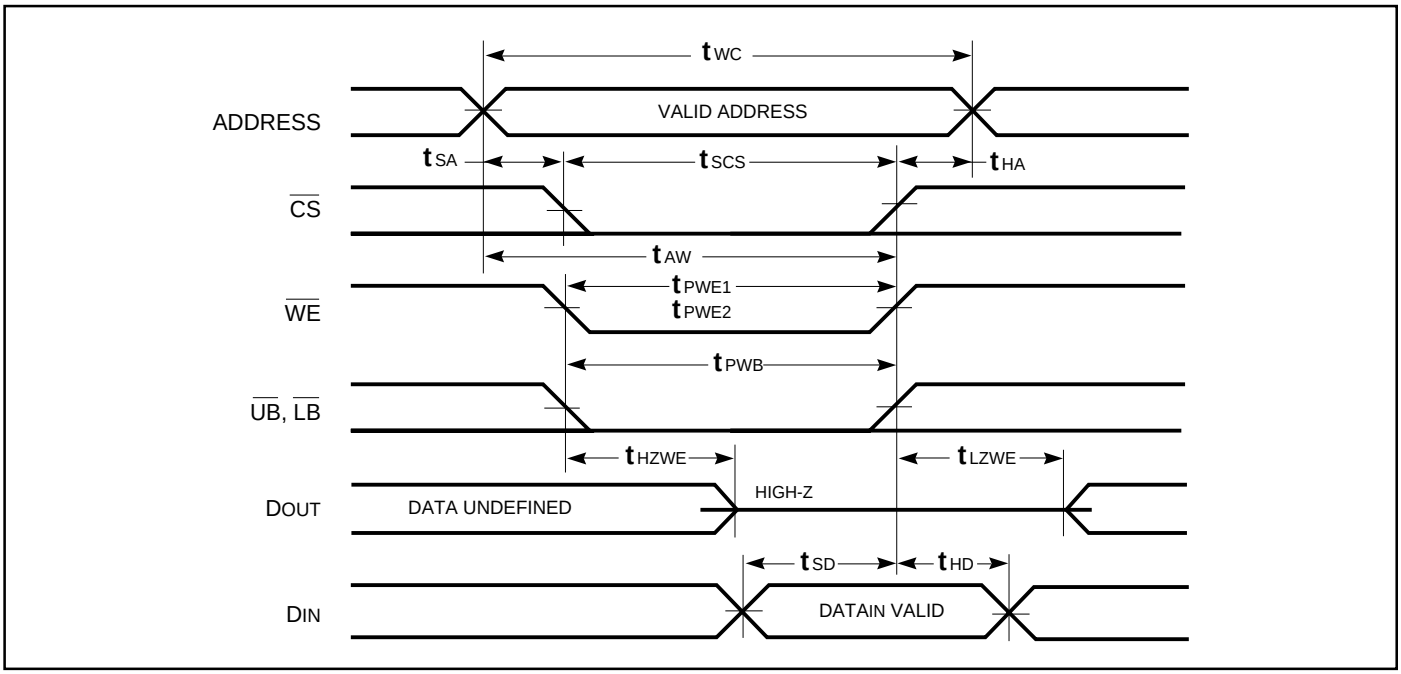
WRITE CYCLE SWITCHING CHARACTERISTICS[1,2] (Over Operating Range)

Symbol	Parameter	-55 Min.	-55 Max.	-70 Min.	-70 Max.	-100 Min.	-100 Max	Unit
t_{WC}	Write Cycle Time	55	—	70	—	100	—	ns
t_{SCE}	$\overline{CE}$ to Write End	50	—	65	—	80	—	ns
t_{AW}	Address Setup Time to Write End	50	—	65	—	80	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	0	—	ns
t_{PWB}	$\overline{LB}$, $\overline{UB}$ Valid to End of Write	45	—	60	—	80	—	ns
t_{PWE}	$\overline{WE}$ Pulse Width	45	—	60	—	80	—	ns
t_{SD}	Data Setup to Write End	25	—	30	—	40	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	0	—	ns
t_{HZWE}[3]	$\overline{WE}$ LOW to High-Z Output	—	30	—	30	—	40	ns
t_{LZWE}[3]	$\overline{WE}$ HIGH to Low-Z Output	5	—	5	—	5	—	ns

Notes:
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.3V, input pulse levels of 0.4V to 2.2V and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of $\overline{CE}$ LOW, and $\overline{UB}$ or $\overline{LB}$, and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
3. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

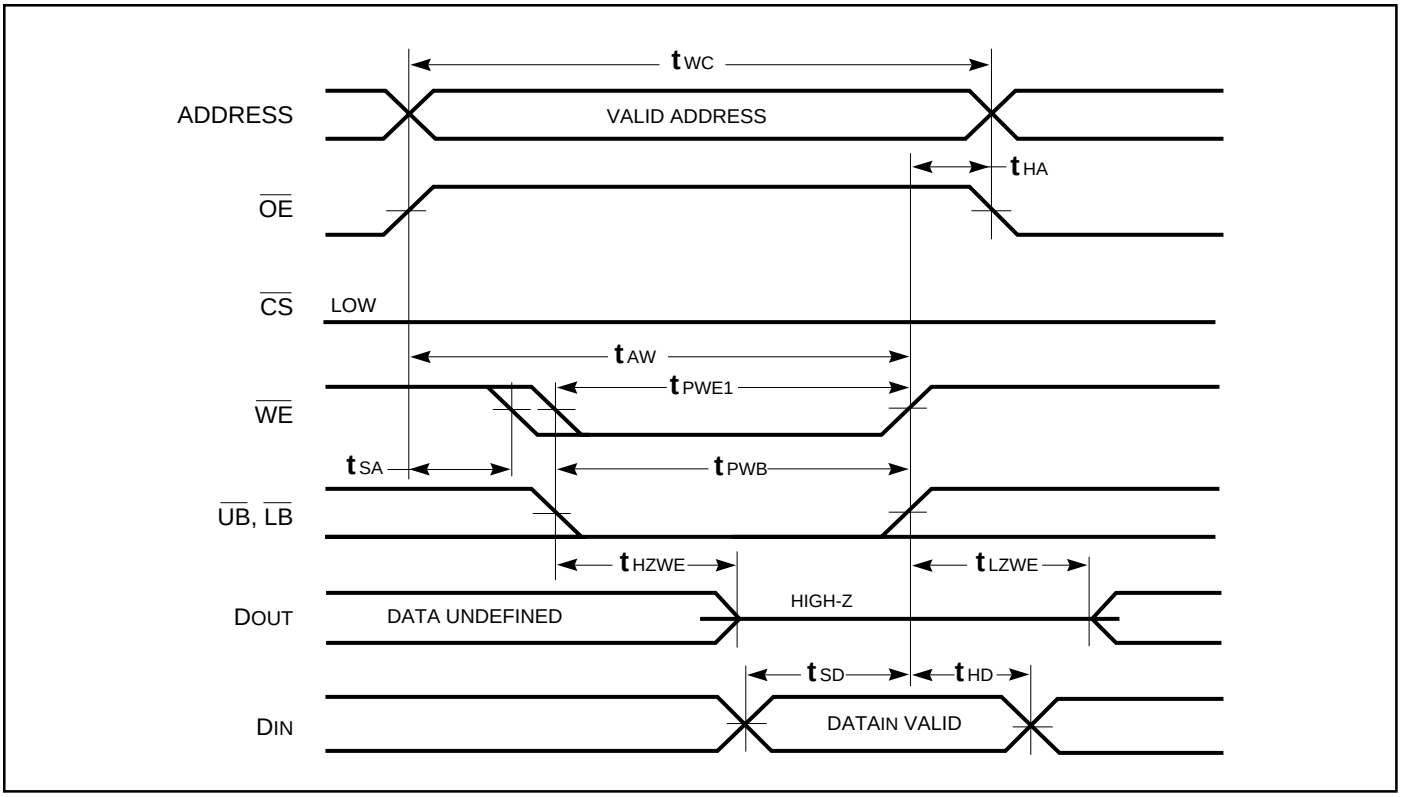
AC WAVEFORMS

WRITE CYCLE NO. 1[1,2] ($\overline{CS}$, Controlled, $\overline{OE}$ = HIGH or LOW)

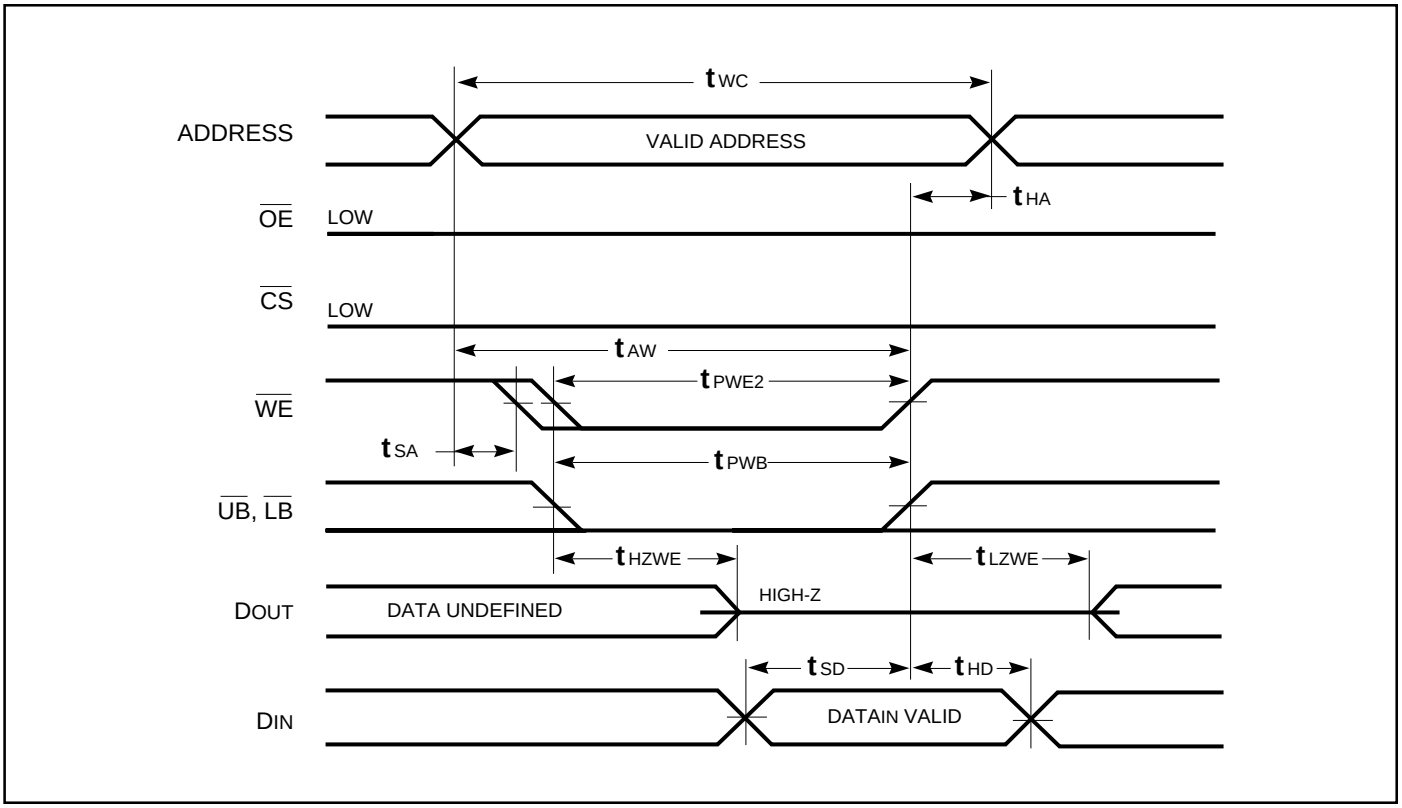


Notes:
1. WRITE is an internally generated signal asserted during an overlap of the LOW states on the $\overline{CS}$ and $\overline{WE}$ inputs and at least one of the $\overline{LB}$ and $\overline{UB}$ inputs being in the LOW state.
2. WRITE = ($\overline{CS}$) [($\overline{LB}$) = ($\overline{UB}$)] ($\overline{WE}$).

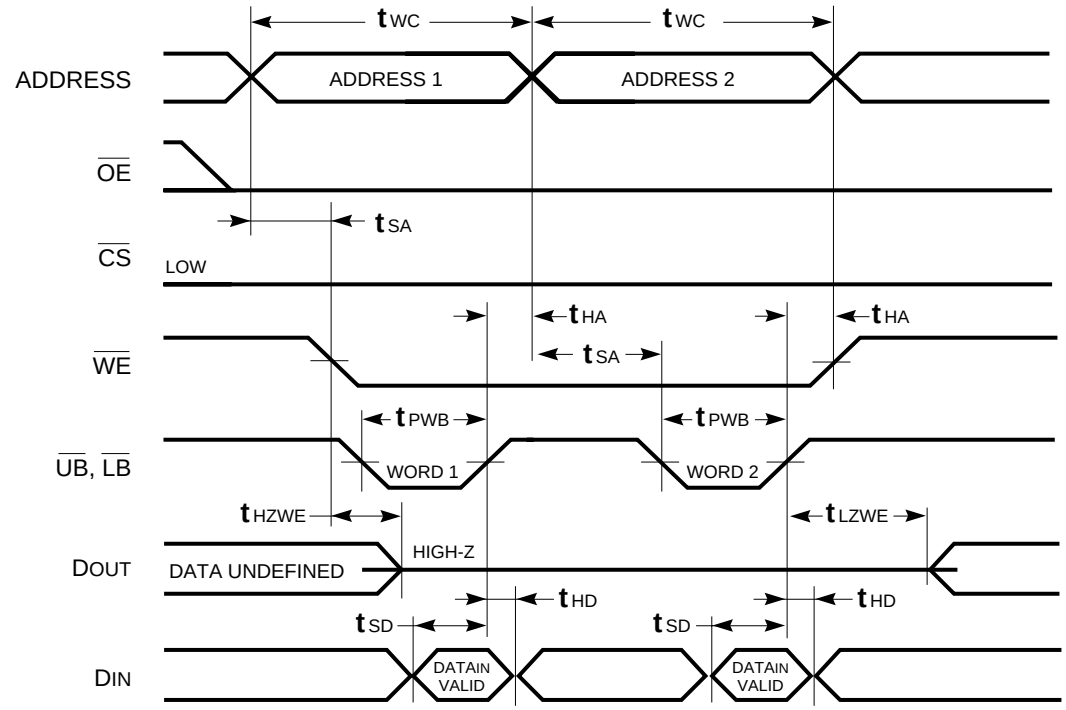
WRITE CYCLE NO. 2 ($\overline{WE}$ Controlled; $\overline{OE}$ is HIGH During Write Cycle)



WRITE CYCLE NO. 3 ($\overline{WE}$ Controlled; $\overline{OE}$ is LOW During Write Cycle)



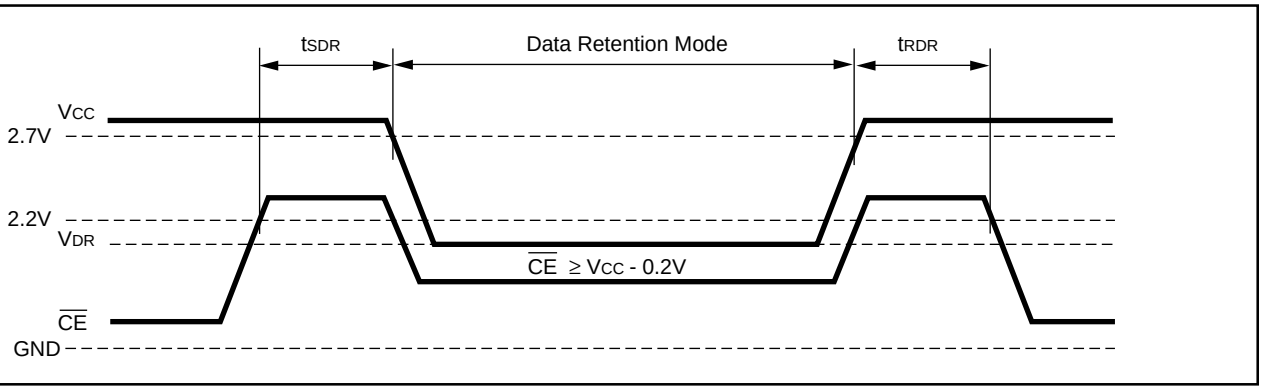
WRITE CYCLE NO. 4 ($\overline{UB}$ / $\overline{LB}$ Controlled)



DATA RETENTION SWITCHING CHARACTERISTICS (L/LL)

Symbol	Parameter	Test Condition		Min.	Max.	Unit
V_{DR}	Vcc for Data Retention	See Data Retention Waveform		1.5	3.6	V
I_{DR}	Data Retention Current	Vcc = 2.0V, $\overline{CE} \geq$ Vcc – 0.2V	Com. (-L)	—	20	µA
			Com. (-LL)	—	5	µA
			Ind. (-L)	—	25	µA
			Ind. (-LL)	—	7	µA
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0	—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		t_{RC}	—	ns

DATA RETENTION WAVEFORM ($\overline{CE}$ Controlled)



ORDERING INFORMATION
Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
55	IS62LV12816L-55T IS62LV12816L-55B	400mil TSOP-2 6*8mm TF-BGA
70	IS62LV12816L-70T IS62LV12816L-70B	400mil TSOP-2 6*8mm TF-BGA
100	IS62LV12816L-100T IS62LV12816L-100B	400mil TSOP-2 6*8mm TF-BGA

Industrial Range: -40°C to +85°C

Speed (ns)	Order Part No.	Package
55	IS62LV12816L-55TI IS62LV12816L-55BI	400mil TSOP-2 6*8mm TF-BGA
70	IS62LV12816L-70TI IS62LV12816L-70BI	400mil TSOP-2 6*8mm TF-BGA
100	IS62LV12816L-100TI IS62LV12816L-100BI	400mil TSOP-2 6*8mm TF-BGA

ORDERING INFORMATION
Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
55	IS62LV12816LL-55T IS62LV12816LL-55B	400mil TSOP-2 6*8mm TF-BGA
70	IS62LV12816LL-70T IS62LV12816LL-70B	400mil TSOP-2 6*8mm TF-BGA
100	IS62LV12816LL-100T IS62LV12816LL-100B	400mil TSOP-2 6*8mm TF-BGA

Industrial Range: -40°C to +85°C

Speed (ns)	Order Part No.	Package
55	IS62LV12816LL-55TI IS62LV12816LL-55BI	400mil TSOP-2 6*8mm TF-BGA
70	IS62LV12816LL-70TI IS62LV12816LL-70BI	400mil TSOP-2 6*8mm TF-BGA
100	IS62LV12816LL-100TI IS62LV12816LL-100BI	400mil TSOP-2 6*8mm TF-BGA

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