

# IS62LV1024L IS62LV1024LL



## 128K x 8 LOW POWER and LOW Vcc CMOS STATIC RAM

### FEATURES

- Access times of 45, 55, and 70 ns
- Low active power: 60 mW (typical)
- Low standby power: 15  $\mu$ W (typical) CMOS standby
- Low data retention voltage: 2V (min.)
- Available in Low Power (-L) and Ultra Low Power (-LL)
- Output Enable ( $\overline{OE}$ ) and two Chip Enable ( $\overline{CE1}$  and CE2) inputs for ease in applications
- TTL compatible inputs and outputs
- Single 2.7V to 3.6V power supply

### DESCRIPTION

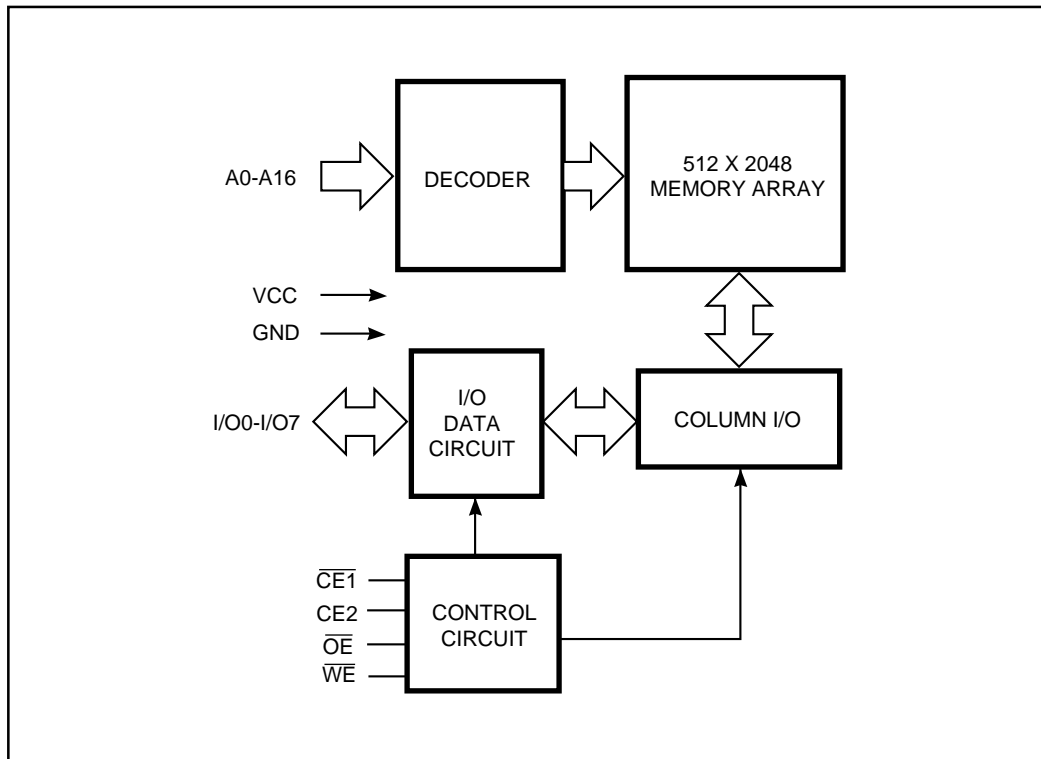
The *ICSI* IS62LV1024L and IS62LV1024LL are low power and low Vcc, 131,072-word by 8-bit CMOS static RAMs. They are fabricated using *ICSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields higher performance and low power consumption devices.

When  $\overline{CE1}$  is HIGH or CE2 is LOW (deselected), the device assumes a standby mode at which the power dissipation can be reduced by using CMOS input levels.

Easy memory expansion is provided by using two Chip Enable inputs,  $\overline{CE1}$  and CE2. The active LOW Write Enable ( $\overline{WE}$ ) controls both writing and reading of the memory.

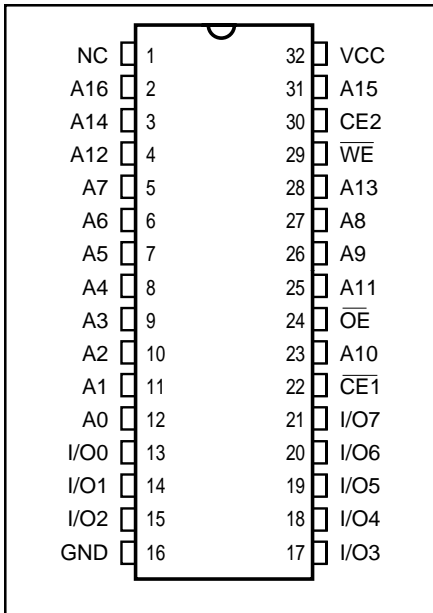
The IS62LV1024L and IS62LV1024LL are available in 32-pin 8\*20mm TSOP-1, 8\*13.4mm TSOP-1, 450mil SOP and 48-pin 6\*8mm TF-BGA.

### FUNCTIONAL BLOCK DIAGRAM

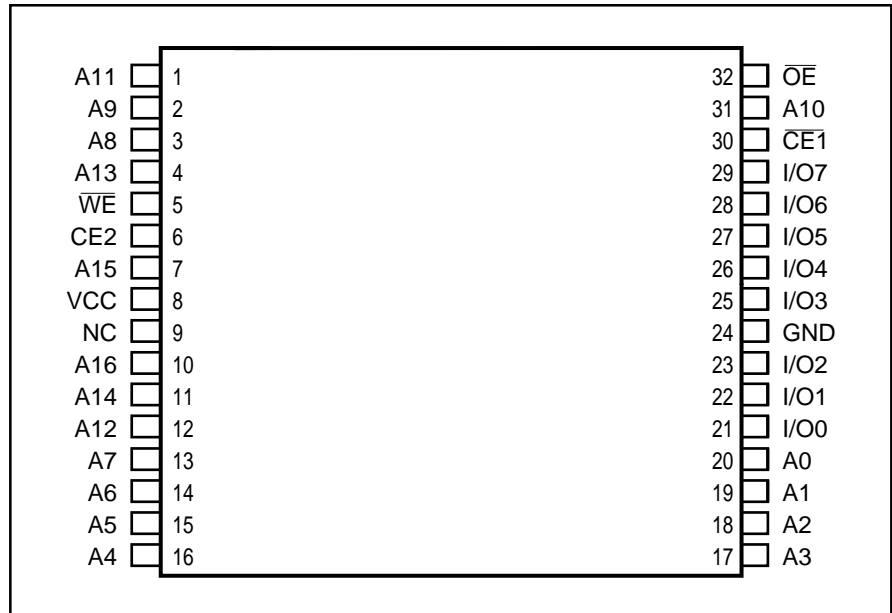


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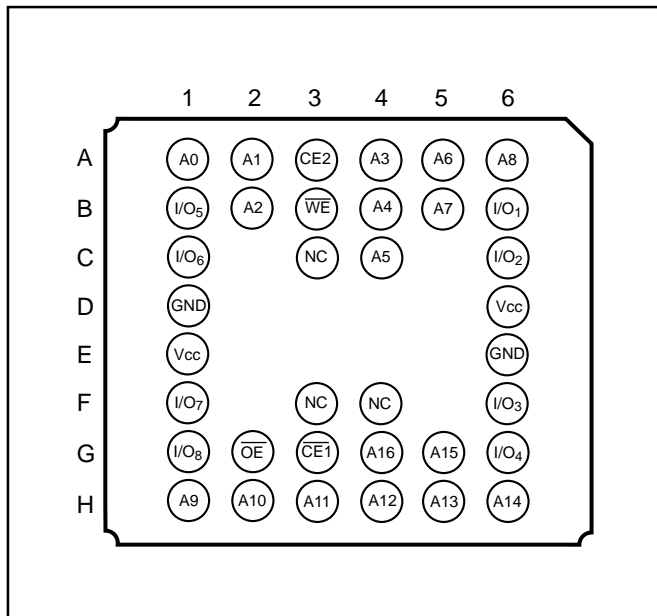
**PIN CONFIGURATION**  
32-Pin SOP



**PIN CONFIGURATION**  
32-Pin 8x20mm TSOP-1 and 8x13.4mm TSOP-1



**48-Pin 6x8mm TF-BGA**



**PIN DESCRIPTIONS**

A0-A16	Address Inputs
$\overline{CE1}$	Chip Enable 1 Input
CE2	Chip Enable 2 Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Input/Output
NC	No Connection
Vcc	Power
GND	Ground

**OPERATING RANGE**

Range	Ambient Temperature	Vcc
Commercial	0°C to +70°C	2.7V to 3.6V
Industrial	-40°C to +85°C	2.7V to 3.6V

## TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE1}$	CE2	$\overline{OE}$	I/O Operation	Vcc Current
Not Selected	X	H	X	X	High-Z	IsB1, IsB2
(Power-down)	X	X	L	X	High-Z	IsB1, IsB2
Output Disabled	H	L	H	H	High-Z	Icc
Read	H	L	H	L	DOUT	Icc
Write	L	L	H	X	DIN	Icc

ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Parameter	Value	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to Vcc + 0.5	V
VCC	Vcc related to GND	-0.3 to +4.6	V
TBIAS	Temperature Under Bias	-40 to +85	°C
TSTG	Storage Temperature	-65 to +150	°C
PT	Power Dissipation	0.7	W

## Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE<sup>(1,2)</sup>

Symbol	Parameter	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	6	pF
COUT	Output Capacitance	VOUT = 0V	8	pF

## Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: TA = 25°C, f = 1 MHz, Vcc = 3.0V.

## DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
VOH	Output HIGH Voltage	Vcc = Min., IOH = -1.0 mA	2.2	—	V
VOL	Output LOW Voltage	Vcc = Min., IOL = 2.1 mA	—	0.4	V
VIH	Input HIGH Voltage		2.2	Vcc + 0.3	V
VIL	Input LOW Voltage <sup>(1)</sup>		-0.3	0.4	V
ILI	Input Leakage	GND ≤ VIN ≤ Vcc	-1	1	μA
ILO	Output Leakage	GND ≤ VOUT ≤ Vcc	-1	1	μA

## Notes:

1. VIL = -3.0V for pulse width less than 10 ns.

IS62LV1024L POWER SUPPLY CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)

Symbol	Parameter	Test Conditions		-45L ns		-55L ns		-70L ns		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
I <sub>CC</sub>	V <sub>CC</sub> Dynamic Operating Supply Current	V <sub>CC</sub> = Max., $\overline{CE} = V_{IL}$ I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub>	Com.	–	40	–	35	–	30	mA
			Ind.	–	45	–	40	–	35	
I <sub>SB1</sub>	TTL Standby Current (TTL Inputs)	V <sub>CC</sub> = Max., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , $\overline{CE1} \geq V_{IH}$ or CE2 ≤ V <sub>IL</sub> , f = 0	Com.	–	0.3	–	0.3	–	0.3	mA
			Ind.	–	0.4	–	0.4	–	0.4	
I <sub>SB2</sub>	CMOS Standby Current (CMOS Inputs)	V <sub>CC</sub> = Max., f = 0 $\overline{CE1} \geq V_{CC} - 0.2V$ , CE2 ≤ 0.2V, or V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2V, V <sub>IN</sub> ≤ 0.2V	Com.	–	50	–	50	–	50	μA
			Ind.	–	75	–	75	–	75	

## Note:

1. At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

IS62LV1024LL POWER SUPPLY CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)

Symbol	Parameter	Test Conditions		-45LL ns		-55LL ns		-70LL ns		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
I <sub>CC</sub>	V <sub>CC</sub> Dynamic Operating Supply Current	V <sub>CC</sub> = Max., $\overline{CE} = V_{IL}$ I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub>	Com.	–	40	–	35	–	30	mA
			Ind.	–	45	–	40	–	35	
I <sub>SB1</sub>	TTL Standby Current (TTL Inputs)	V <sub>CC</sub> = Max., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , $\overline{CE1} \geq V_{IH}$ or CE2 ≤ V <sub>IL</sub> , f = 0	Com.	–	0.2	–	0.2	–	0.2	mA
			Ind.	–	0.3	–	0.3	–	0.3	
I <sub>SB2</sub>	CMOS Standby Current (CMOS Inputs)	V <sub>CC</sub> = Max., f = 0 $\overline{CE1} \geq V_{CC} - 0.2V$ , CE2 ≤ 0.2V, or V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2V, V <sub>IN</sub> ≤ 0.2V	Com.	–	5	–	5	–	5	μA
			Ind.	–	10	–	10	–	10	

## Note:

1. At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

**READ CYCLE SWITCHING CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)**

Symbol	Parameter	-45		-55		-70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>RC</sub>	Read Cycle Time	45	—	55	—	70	—	ns
t <sub>AA</sub>	Address Access Time	—	45	—	55	—	70	ns
t <sub>OH</sub>	Output Hold Time	10	—	10	—	10	—	ns
t <sub>ACE1</sub>	$\overline{CE1}$ Access Time	—	45	—	55	—	70	ns
t <sub>ACE2</sub>	CE2 Access Time	—	45	—	55	—	70	ns
t <sub>DOE</sub>	$\overline{OE}$ Access Time	—	20	—	25	—	35	ns
t <sub>LZOE<sup>(2)</sup></sub>	$\overline{OE}$ to Low-Z Output	0	—	5	—	5	—	ns
t <sub>HZOE<sup>(2)</sup></sub>	$\overline{OE}$ to High-Z Output	0	15	0	20	0	25	ns
t <sub>LZCE1<sup>(2)</sup></sub>	$\overline{CE1}$ to Low-Z Output	5	—	7	—	10	—	ns
t <sub>LZCE2<sup>(2)</sup></sub>	CE2 to Low-Z Output	5	—	7	—	10	—	ns
t <sub>HZCE<sup>(2)</sup></sub>	$\overline{CE1}$ or CE2 to High-Z Output	0	15	0	20	0	25	ns

**Notes:**

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0.4V to 2.2V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured  $\pm 500$  mV from steady-state voltage. Not 100% tested.

**AC TEST CONDITIONS**

Parameter	Unit
Input Pulse Level	0.4V to 2.2V
Input Rise and Fall Times	5 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1

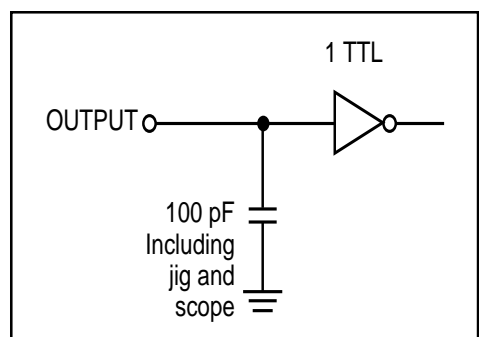
**AC TEST LOADS**


Figure 1.

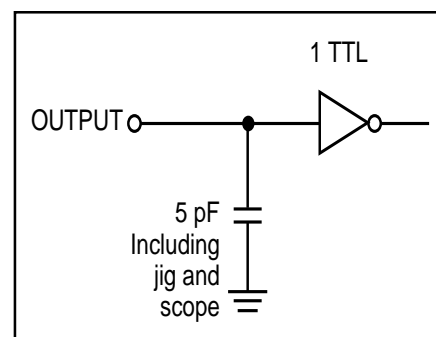
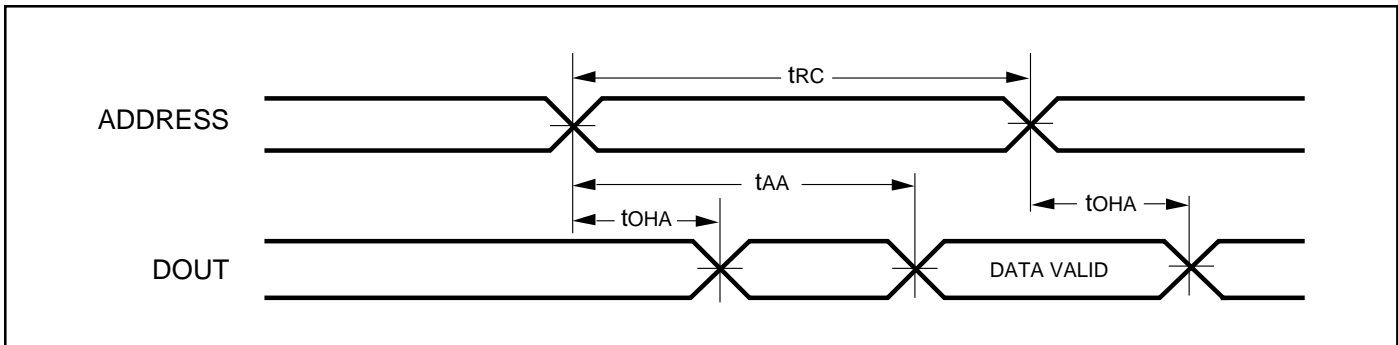
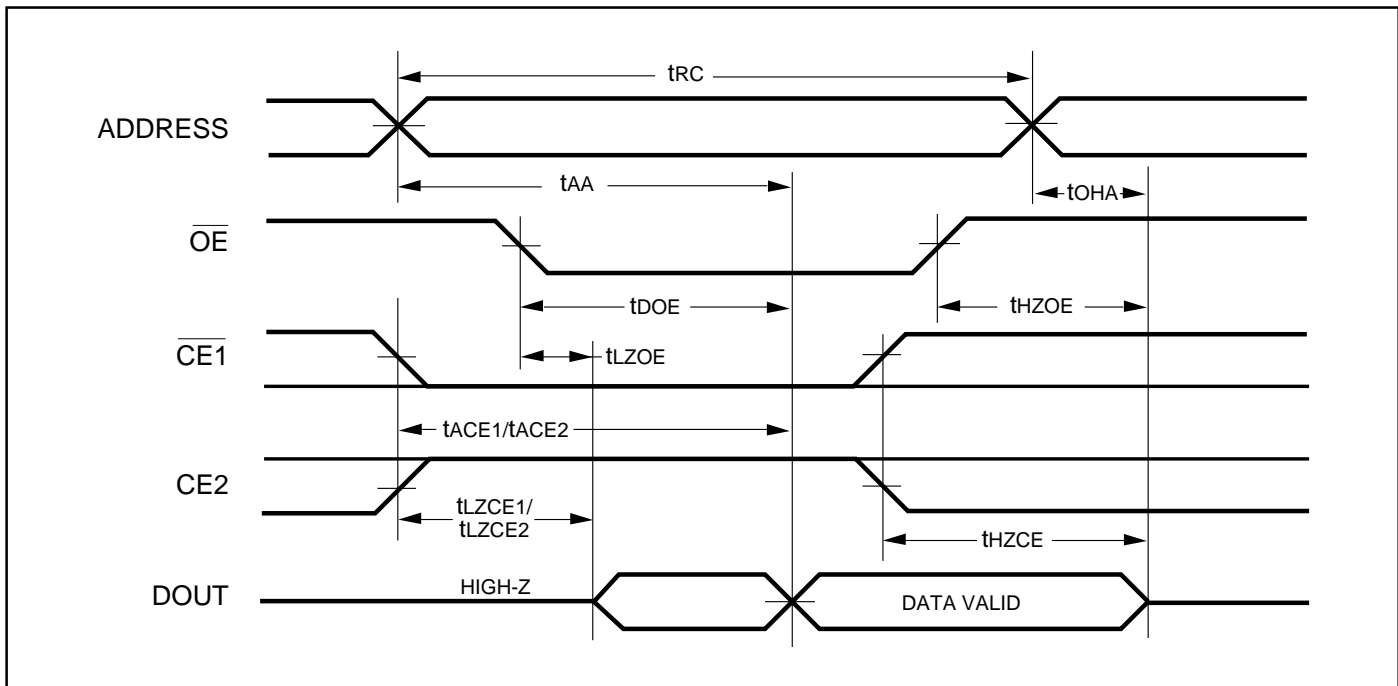


Figure 2.

## AC WAVEFORMS

READ CYCLE NO. 1<sup>(1,2)</sup>READ CYCLE NO. 2<sup>(1,3)</sup>

## Notes:

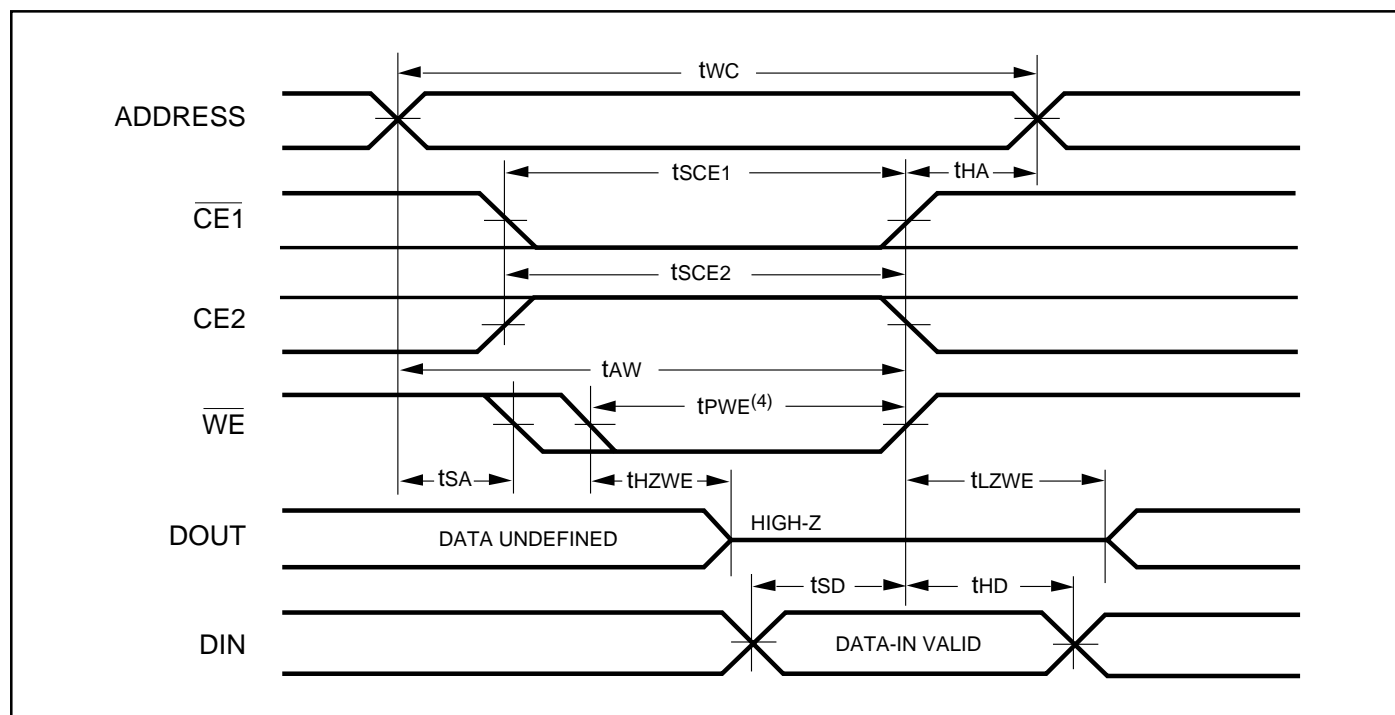
1.  $\overline{WE}$  is HIGH for a Read Cycle.
2. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE1} = V_{IL}$ ,  $CE2 = V_{IH}$ .
3. Address is valid prior to or coincident with  $\overline{CE1}$  LOW and  $CE2$  HIGH transitions.

**WRITE CYCLE SWITCHING CHARACTERISTICS<sup>(1,3)</sup> (Over Operating Range, Standard and Low Power)**

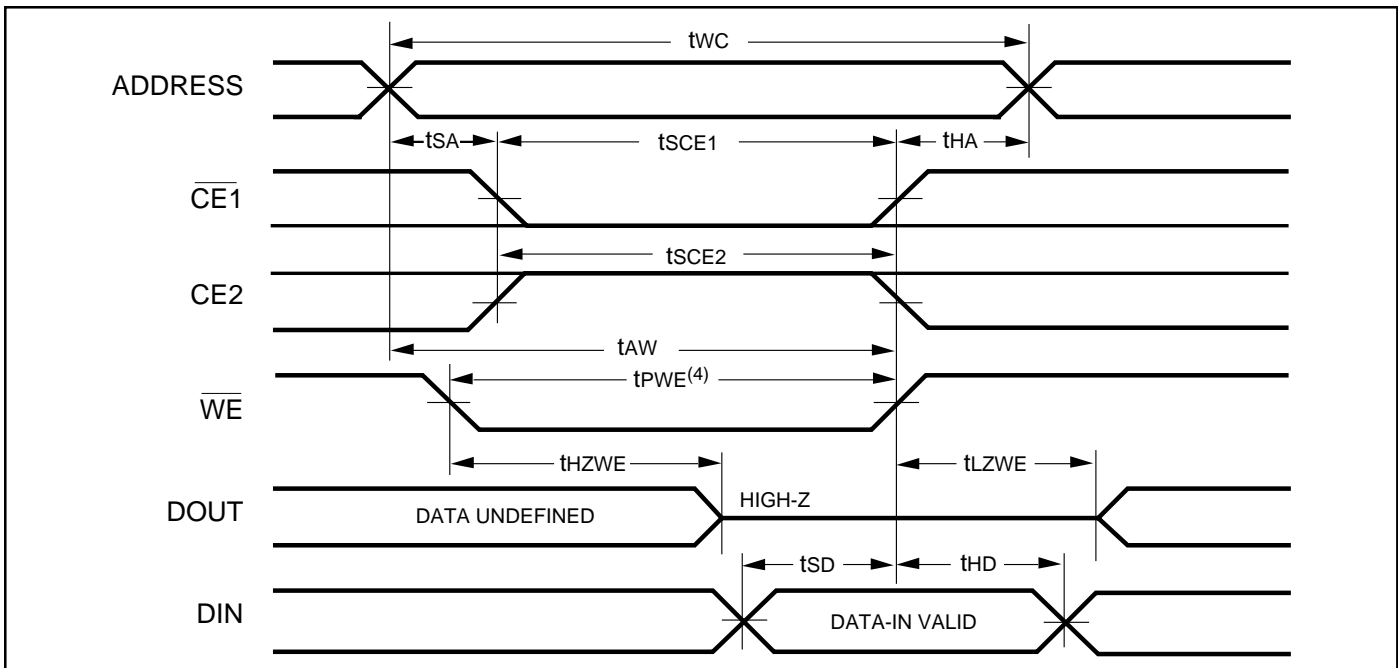
Symbol	Parameter	-45		-55		-70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{WC}$	Write Cycle Time	45	—	55	—	70	—	ns
$t_{SCE1}$	$\overline{CE1}$ to Write End	35	—	50	—	60	—	ns
$t_{SCE2}$	CE2 to Write End	35	—	50	—	60	—	ns
$t_{AW}$	Address Setup Time to Write End	35	—	50	—	60	—	ns
$t_{HA}$	Address Hold from Write End	0	—	0	—	0	—	ns
$t_{SA}$	Address Setup Time	0	—	0	—	0	—	ns
$t_{PWE}^{(4)}$	$\overline{WE}$ Pulse Width	35	—	40	—	55	—	ns
$t_{SD}$	Data Setup to Write End	25	—	25	—	30	—	ns
$t_{HD}$	Data Hold from Write End	0	—	0	—	0	—	ns
$t_{HZWE}^{(2)}$	$\overline{WE}$ LOW to High-Z Output	—	15	—	20	0	25	ns
$t_{LZWE}^{(2)}$	$\overline{WE}$ HIGH to Low-Z Output	5	—	5	—	5	—	ns

**Notes:**

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0.4V to 2.2V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured  $\pm 500$  mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of  $\overline{CE1}$  LOW, CE2 HIGH and  $\overline{WE}$  LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
4. Tested with  $\overline{OE}$  HIGH.

**AC WAVEFORMS**
**WRITE CYCLE NO. 1 ( $\overline{WE}$  Controlled)<sup>(1,2)</sup>**


WRITE CYCLE NO. 2 ( $\overline{CE1}$ , CE2 Controlled)<sup>(1,2)</sup>



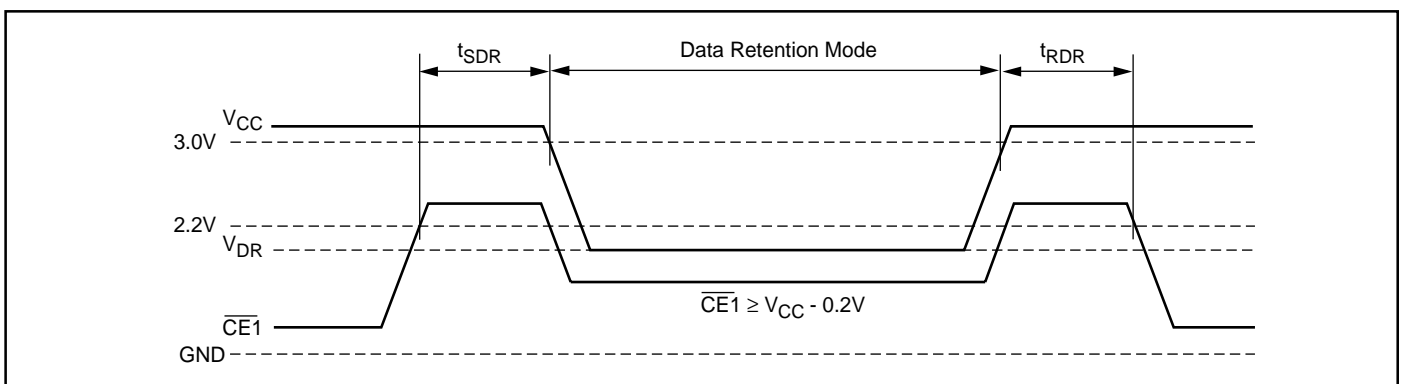
Notes:

1. The internal write time is defined by the overlap of  $\overline{CE1}$  LOW, CE2 HIGH and  $\overline{WE}$  LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if  $\overline{OE} = V_{IH}$ .

DATA RETENTION SWITCHING CHARACTERISTICS

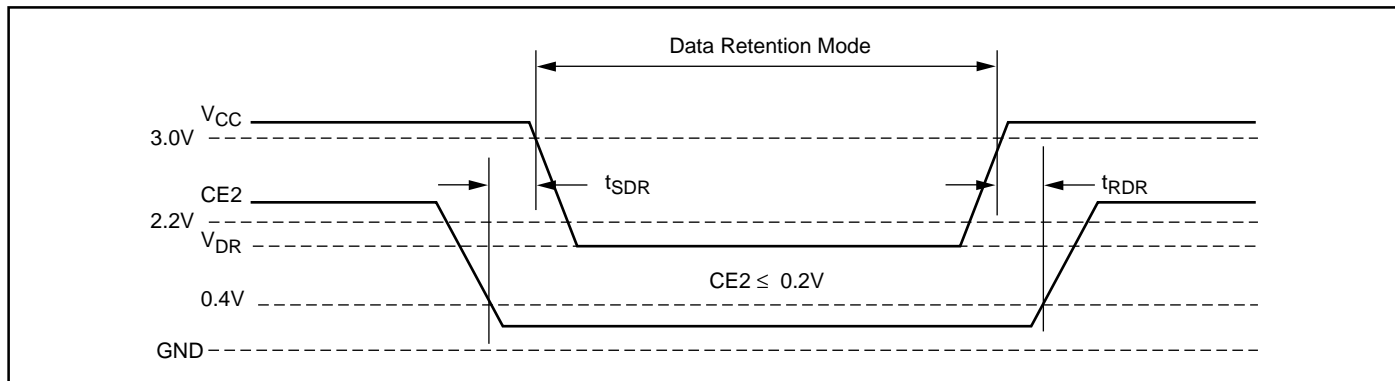
Symbol	Parameter	Test Condition	Min.	Max.	Unit	
$V_{DR}$	$V_{CC}$ for Data Retention	See Data Retention Waveform	2.0	3.6	V	
$I_{DR}$	Data Retention Current	$V_{CC} = 2.0V, \overline{CE1} \geq V_{CC} - 0.2V$	Com. (-L)	—	30	$\mu A$
		Com. (-LL)	—	5	$\mu A$	
		Ind. (-L)	—	50	$\mu A$	
		Ind. (-LL)	—	10	$\mu A$	
$t_{SDR}$	Data Retention Setup Time	See Data Retention Waveform	0	—	ns	
$t_{RDR}$	Recovery Time	See Data Retention Waveform	$t_{RC}$	—	ns	

DATA RETENTION WAVEFORM ( $\overline{CE1}$  Controlled)





## DATA RETENTION WAVEFORM (CE2 Controlled)



## IS62LV1024L

## ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
45	IS62LV1024L-45Q	450mil SOP
	IS62LV1024L-45T	8*20mm TSOP-1
	IS62LV1024L-45H	8*13.4mm TSOP-1
	IS62LV1024L-45B	6*8mm TF-BGA
55	IS62LV1024L-55Q	450mil SOP
	IS62LV1024L-55T	8*20mm TSOP-1
	IS62LV1024L-55H	8*13.4mm TSOP-1
	IS62LV1024L-55B	6*8mm TF-BGA
70	IS62LV1024L-70Q	450mil SOP
	IS62LV1024L-70T	8*20mm TSOP-1
	IS62LV1024L-70H	8*13.4mm TSOP-1
	IS62LV1024L-70B	6*8mm TF-BGA

## IS62LV1024L

## ORDERING INFORMATION

Industrial Range: -40°C to +85°C

Speed (ns)	Order Part No.	Package
45	IS62LV1024L-45QI	450mil SOP
	IS62LV1024L-45TI	8*20mm TSOP-1
	IS62LV1024L-45HI	8*13.4mm TSOP-1
	IS62LV1024L-45BI	6*8mm TF-BGA
55	IS62LV1024L-55QI	450mil SOP
	IS62LV1024L-55TI	8*20mm TSOP-1
	IS62LV1024L-55HI	8*13.4mm TSOP-1
	IS62LV1024L-55BI	6*8mm TF-BGA
70	IS62LV1024L-70QI	450mil SOP
	IS62LV1024L-70TI	8*20mm TSOP-1
	IS62LV1024L-70HI	8*13.4mm TSOP-1
	IS62LV1024L-70BI	6*8mm TF-BGA

## IS62LV1024LL

## ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
45	IS62LV1024LL-45Q	450mil SOP
	IS62LV1024LL-45T	8*20mm TSOP-1
	IS62LV1024LL-45H	8*13.4mm TSOP-1
	IS62LV1024LL-45B	6*8mm TF-BGA
55	IS62LV1024LL-55Q	450mil SOP
	IS62LV1024LL-55T	8*20mm TSOP-1
	IS62LV1024LL-55H	8*13.4mm TSOP-1
	IS62LV1024LL-55B	6*8mm TF-BGA
70	IS62LV1024LL-70Q	450mil SOP
	IS62LV1024LL-70T	8*20mm TSOP-1
	IS62LV1024LL-70H	8*13.4mm TSOP-1
	IS62LV1024LL-70B	6*8mm TF-BGA

## IS62LV1024LL

## ORDERING INFORMATION

Industrial Range: -40°C to +85°C

Speed (ns)	Order Part No.	Package
45	IS62LV1024LL-45QI	450mil SOP
	IS62LV1024LL-45TI	8*20mm TSOP-1
	IS62LV1024LL-45HI	8*13.4mm TSOP-1
	IS62LV1024LL-45BI	6*8mm TF-BGA
55	IS62LV1024LL-55QI	450mil SOP
	IS62LV1024LL-55TI	8*20mm TSOP-1
	IS62LV1024LL-55HI	8*13.4mm TSOP-1
	IS62LV1024LL-55BI	6*8mm TF-BGA
70	IS62LV1024LL-70QI	450mil SOP
	IS62LV1024LL-70TI	8*20mm TSOP-1
	IS62LV1024LL-70HI	8*13.4mm TSOP-1
	IS62LV1024LL-70BI	6*8mm TF-BGA



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